SF32LB58x

Datasheet

V1.6

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Revision History

Document Status

Document Status	Version Range	Description
Draft	0.0.0 ~0.9.9	Initial draft, informal release. The information is preliminary data, reflecting the specifications and performance of the product before mass production. No warranty is made as to the accuracy and the content is subject to change at any time without notice.
Release	1.0.0 ~1.9.9	Official release, and minor amendments might be made to the information to more accurately reflect the specifications and performance of mass-produced products; SiFli reserves the right to make changes to the document at any time without notice.

Revision History

Date	Version	Release Notes
2024-05-15	1.6	Updated GPADC specification; Added ordering information
2024-03-06	1.5	Added IO drive strength information
2024-02-23	1.4	Adjusted table formats
2024-01-26	1.3	Updated Tstorage temperature range
2023-12-29	1.2	Updated reliability data
2023-06-05	1.1	Updated power specification data
2023-03-13	1.0	Corrected typos
2023-03-03	0.9	Updated BLE Connection data
2023-02-28	0.8	Added power consumption calculation data
2023-02-27	0.7	Updated processor power consumption data
2023-02-24	0.6	Updated power consumption and audio data
2023-02-16	0.5	Updated Bluetooth data
2023-02-15	0.4	Updated RF data
2023-01-04	0.3	Updated power consumption data
2022-11-18	0.2	Added PSA Certified Level 1
2022-05-16	0.1	Initial draft

Overview

SF32LB58x is a family of highly integrated high-performance MCUs desgined for ultra-low power Artifical Intelligence of Things (AIoT) scenarios. SF32LB58x adopts the big.LITTLE architecture with Arm Cortex-M33 STAR-MC1 processors, and is embedded with 2D/2.5D GPU, neural network matrix accelerator, dual-mode BT5.3, and audio Codec. SF32LB58x can be used for a wide variety of applications such as wearables, smart HMI devices, and smart homes.

The dual-big core high performance processor of SF32LB58x can operate at up to 240MHz, delivering up to 984 CoreMark per core, and the energy efficiency reaches 8.29uA/CoreMark. The low-power processor ("LITTLE core") can operate at up to 96MHz for 394 CoreMark and serves as both sensor hub and Bluetooth controller at high energy efficiency of 3.88uA/CoreMark. This architecture delivers no-compromise user experience of both high computational performance required for feature-rich graphical HMI and always-on ultra-low power sensor control and wireless connectivity.

The dual-2D/2.5D GPU, at up to 240MHz, supports vector graphics and fonts, 4-layer alpha blending, hardware accelerated rotation and scaling, and conversion of various common graphic formats. eZip™2.0 supports lossless compressed graphics file, saving memory bandwidth and storage capacity. The dual-LCD controller can support interfaces of 8080/QSPI/MIPI-DSI/JDI at a full-screen refresh frame rate up to 60fps, and supports Always-On Display.

The dual-mode BT5.3 transceiver has a Max. Tx power of 13dBm at EDR2 mode, and 19dBm at BLE mode. The receiver consumes peak current of 2.2mA@3.3V at BR mode, and has a sensitivity of -100dBm (1Mbps) for BLE and -96.3dBm for BR and -95.5dBm for EDR2.

Functional Block Diagram

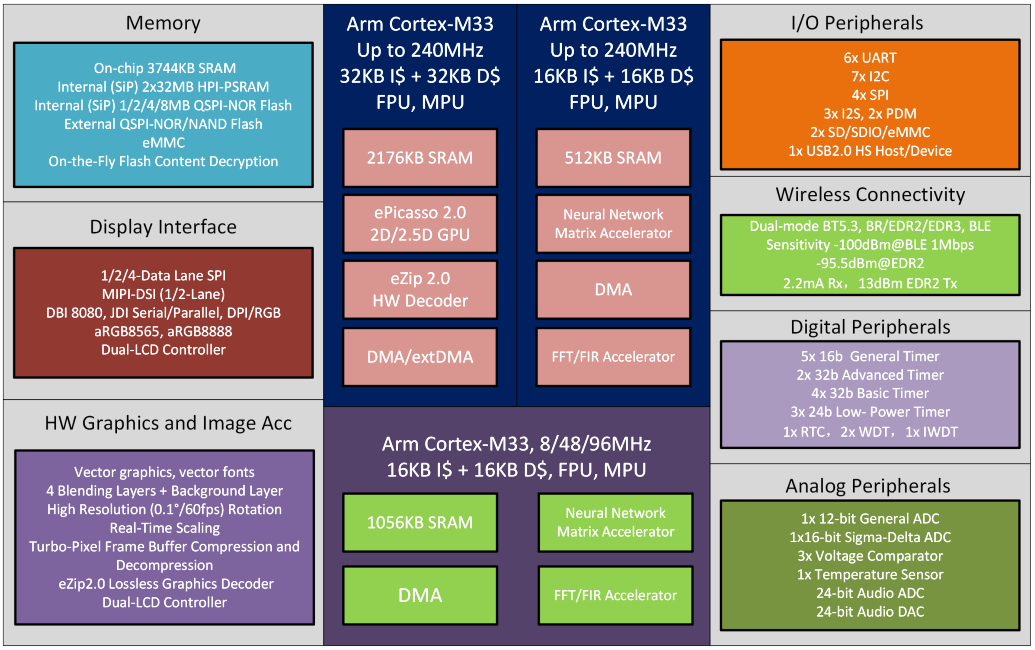

Figure 0-1: Functional Block Diagram

Features

CPU and Memory

- High Performance Processor (HCPU/ACPU)
  - Arm Cortex-M33 STAR-MC1
  - Up to 240MHz clock frequency, adjustable
  - Up to 370DMIPS, 984 EEMBC CoreMark
  - I-Cache + D-Cache
    - HCPU: 32KB(2-way)+32KB(4-way)
    - ACPU: 16KB(2-way)+16KB(4-way)
  - SRAM： 2176KB(HCPU)+512KB(ACPU)
  - CoreMark power (@3.3V)
    - 34uA/MHz
    - 8.29uA/CoreMark
    - 121CoreMark/mA
  - Floating Point Unit (FPU)
  - Memory Protection Unit (MPU)
- Ultra Low-Power Processor (LCPU)
  - Arm Cortex-M33 STAR-MC1
  - Up to 96MHz clock frequency, adjustable
  - Up to 148DMIPS, 394 EEMBC CoreMark
  - I/D-Cache: 16KB (2-way)+16KB (4-way)
  - SRAM: 1056KB (all Retention SRAM)
  - CoreMark power (48MHz, 3.3V):
    - 15.9uA/MHz
    - 3.88uA/CoreMark
    - 258CoreMark/mA
  - Floating Point Unit (FPU)
  - Memory Protection Unit (MPU)

Wireless Connectivity

- Dual-mode BT5.3, with BLE Audio support
- Sensitivity
  - BLE/1Mbps: -100dBm
  - BLE/2Mbps: -97dBm
  - BLE/LR 125kbps: -107.5dBm
  - BLE/LR 500bps: -104.5dBm
  - BT/BR 1Mbps: -96.3dBm
  - BT/EDR 2Mbps: -95.5dBm
  - BT/EDR 3Mbps: -88.5dBm
- Max. Tx power: 13dBm(EDR2/3), 19dBm(BR/BLE)
- Rx peak current (BR/EDR2/EDR3): 2.2mA@3.3V
- Average current (3.3V, 500ms, 0dBm Tx power)
  - BT Sniff: 20.0uA
  - BLE Connection: 15.0uA

Graphics and Display

- Dual-2D/2.5D GPU
  - 1×2D/2.5D GPU—ePicasso™2.0
  - 1×2D/2.5D GPU—Vivante GCNanoUltraV
  - Support vector graphics and fonts
  - Hardware-accelerated rotation, scaling, mirroring
  - Maximum resolution: 1024×1024
  - Support aRGB8565, aRGB8888, L8, A8, A4, alpha blending
- Lossless Decompression Accelerator – eZip™2.0
  - Lossless graphics decompression, support native animation
  - Concatenated operation with ePicasso™2.0
- JPEG Codec Accelerator
  - Support the encoding and decoding of hardware JPEG images
  - Support the cropping and scaling of hardware-accelerated JPEG images
  - Support MJPEG video playback
- LCD Controller
  - Support 8080, SPI, Dual-SPI, Quad-SPI, MIPI-DSI, JDI
  - 2-layer alpha blending + 1 background layer
  - TurboPixel™ Frame Buffer compression and decompression
  - Dual-LCD controller, support ultra-low power consumption Always-On Display mode

Audio

- 2×HiFi 24-bit Audio DAC
  - Sample rate: 8k/ 16k/ 11.025k/ 22.05k/ 24k/ 32k/ 44.1k/ 48kHz
  - SNR(with 10kOhm load and A-Weighted): 109dB
  - THD+N: -101dB, Dynamic Range: 109dB
  - Noise Floor: 3.3 μVrms
- 2×HiFi 24-bit Audio ADC
  - Sample rate: 8k/ 11.025k/ 12k/ 16k/ 22.05k/ 24k/ 32k/ 44.1k/ 48kHz

  - SNR(A-Weighted): 99dB
  - THD+N: -90dB, Dynamic Range: 99dB
- 3× I²S, 2× PDM
- Audio sample rate conversion accelerator
- Audio equalizer

Neural Network Matrix Accelerator

- Matrix convolution acceleration for TinyML scenarios
- Processing power up to 1.92GOPS
- Energy efficiency higher than 10TOPS/W

Hardware-Accelerated Digital Signal Processing

- One FFT accelerator in big core and one in LITTLE core
- One FIR filter accelerator in big core and one in LITTLE core
- One CORDIC trigonometric function co-processor for each processor

Memory Interface

- 5×MPI (Memory Peripheral Interface)
  - MPI1/2: dedicated SiP interface, support OPI/HPI-PSRAM, DDR, Max. frequency 144MHz, Max. throughput 576MB/s
  - MPI3/4: external interface, support QSPI-NOR, QSPI-NAND, QPI-PSRAM, Max. frequency 96MHz, Max. throughput 96MB/s
  - MPI5: dedicated SiP interface, support QSPI-NOR, DTR, Max. frequency 48MHz
  - MPI1/2/3/5: support real-time decryption of off-chip code
- 2×SD/SDIO/eMMC, one 4-bit and one 8-bit, support SD3.0, SDIO3.0 and eMMC4.51, Max. frequency 96MHz, support DDR

System Clock

- Oscillator
  - 48MHz crystal oscillator
  - Low power RC oscillator: 1MHz, 48MHz
  - Ultra-low powr RC oscillator: 10KHz
  - Ultra-low powr 32.768KHz crystal oscillator, optional
- PLL
  - Dedicated audio PLL
  - 3×PLL, Max. frequency 384MHz, in 24MHz steps

Security

- AES, HASH and CRC hardware accelerator
- True Random Number Generator (TRNG)
- Secure Boot
- 1024-bit eFuse to store Root of Trust and UID
- PSA Certified Level 1

Others

- DMA
  - General DMA: high efficiency data transfer between internal memory and peripherals
  - extDMA: high efficiency data transfer between internal memory and external memory
- Timers
  - 5×16b GPTIM, 2×32b ATIM, 4×32b BTIM, 3×24b LPTIM
  - 1×RTC
  - 2×24b WDT, 1×IWDT
- Analog Peripherals
  - 1×12-bit general purpose SAR ADC, 8 channels
  - 1×16-bit Sigma-Delta ADC, 5 channels
  - 1×Temperature sensor
  - 3×Low power voltage comparator
- I/O Peripherals
  - 6×UART, 7× I²C, 4×SPI
  - 3× I²S, 2× PDM
  - 1×USB2.0 HS Host/Device
  - SIM card controller
  - Peripheral Task Controller (PTC)
- Power Management
  - Power supply: 1.7 to 3.6V, -40 to 85°C
  - High-efficiency buck and low-power LDO
  - Sleep current with RTC wake-up: 700nA
  - Sleep current with pin wake-up: 300nA

Package

- BGA256, 154(HP94+LP60) GPIOs, 6.5×8.5×0.94mm

Applications

Smart Wearable

- High-end smart watch
- Smart wristband
- Wearable medical device
- Fitness equipment

Industrial Device

- Cost-effective display solution
- Graphical Human-Machine Interface (HMI) device
- Industrial sensor hub
- Industrial equipment monitoring
- Industrial instrumentation

Vehicle Device

- Electric vehicle control center
- Car key
- Wearable car remote controls

Home Automation

- Smart home appliance
- Smart door lock

Generic Scenario

- Low-power sensor hub
- Bluetooth mesh

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1 Introduction

1.1 System Architecture

SF32LB58x is a family of highly integrated high-performance SoC MCUs desgined for ultra-low-power Artifical Intelligence of Things (AIoT) scenarios. SF32LB58x adopts the big.LITTLE architecture with the Arm Cortex-M33 STAR-MC1 processor.

- High-Performance Processor/Big Core (HCPU/ACPU): Up to 240MHz clock frequency, HCPU has 32KB instruction cache (I-Cache) and 32KB data cache (D-Cache), ACPU has 16KB instruction cache (I-Cache) and 16KB data cache (D-Cache), 2688KB SRAM (HCPU 2176KB, ACPU 512KB); As the system master, it can efficiently access on-chip and off-chip storage. It is mainly used for system control, Human-Machine Interaction, and high-performance computing.
- Ultra-low Power Processor/LITTLE Core (LCPU): Up to 96MHz clock frequency, 16KB instruction cache (I-Cache) and 16KB data cache (D-Cache), 1056KB SRAM (all Retention SRAM); it is mainly used as the system's ultra-low power sensor hub and Bluetooth Low Energy connection controller to meet various data acquisition, processing, transmission and control requirements in ultra-low power scenarios.

1.2 Cortex-M33 STAR-MC1 Processor

Cortex-M33 STAR-MC1 processor is the first processor of the "Star" series from Arm China. It has the key features of Cortex-M33, supporting the full functionality of the existing Arm v8-M architecture, and with an in-order three-stage pipeline, it can significantly reduce the power consumption of the system. It also has partial dual-issue 16-bit instruction capability, and the coprocessor interface is further improved to support the Cache.

With the performance reaching 1.5DMIPS/MHz and 4.02Coremark/MHz, Cortex-M33 STAR-MC1 delivers a 20% performance improvement over previous-generation Arm processors at the same clock speed.

Cortex-M33 STAR-MC1 has a coprocessor interface which can further enhance the capability of customized calculation to meet the requirements of different scenarios. The MCR (Move from Coprocessor to Register) and MRC (Move from Register to Coprocessor) instructions enable the transfer of register data and computation results between Cortex-M33 STAR-MC1 and the coprocessor, making it ideal for operations with small data volumes, complex calculations but relatively fragmented and low latency. While the coprocessor computes, Cortex-M33 STAR-MC1 processor can still execute other instructions in parallel, thus significantly improving execution efficiency.

In addition, the processor supports Digital Signal Processing (DSP) instruction sets and Floating Point Unit (FPU).

Tightly Coupled Memory (TCM) and Cache technologies are adopted in Cortex-M33 STAR-MC1 processor to enhance flexibility in the use of internal and external memory systems with different characteristics, ensuring the real-time response and computational efficiency of the processor in a variety of scenarios.

1.3 High-Performance Processor (Big Core) System (HPSYS)

1.3.1 Bus Architecture

The HPSYS provides an internal bus matrix based on the AHB protocol, which supports multiple master devices to access the address spaces of multiple slave devices in parallel.

HCPU can access all address spaces of HPSYS, and can access all address spaces of LPSYS through HP2LP.

ACPU can access all address spaces of HPSYS except HPSYS_ITCM and Retention RAM, and can access all address spaces of LPSYS (except LPSYS_DTCM) through HP2LP.

DMAC1 and DMAC2 can access all address spaces of HPSYS except HPSYS_ITCM and Retention RAM, and can access all address spaces of LPSYS (except LPSYS_DTCM) through HP2LP.

Some master devices of LPSYS can access the address spaces of HPSYS (except HPSYS_ITCM and Retention RAM) through LP2HP.

The address space of HPSYS_ITCM and Retention RAM can only be accessed by HCPU. DTCM shares 128KB address spaces with HPSYS_RAM0, and can be accessed by HCPU and other master devices.

When multiple master devices access the address space of the same slave device at the same time, the access order will be determined based on the polling arbitration principle.

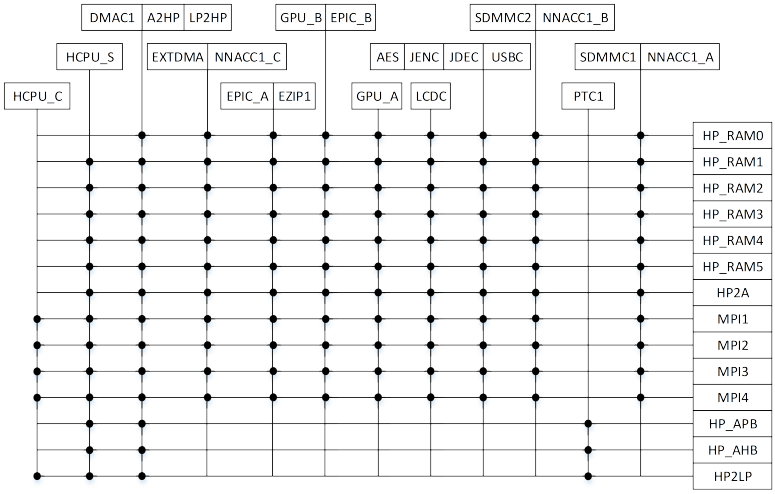


Figure 1-1: Bus Architecture of HCPU

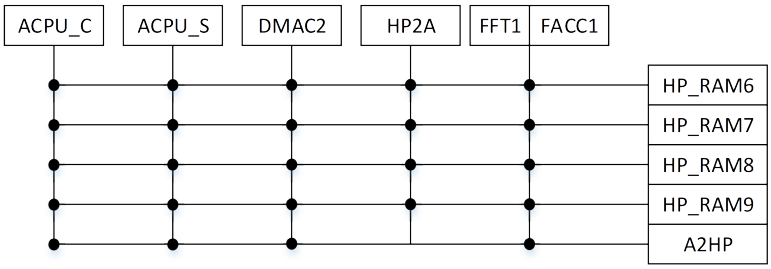


Figure 1-2: Bus Architecture of ACPU

1.3.2 Clock Architecture

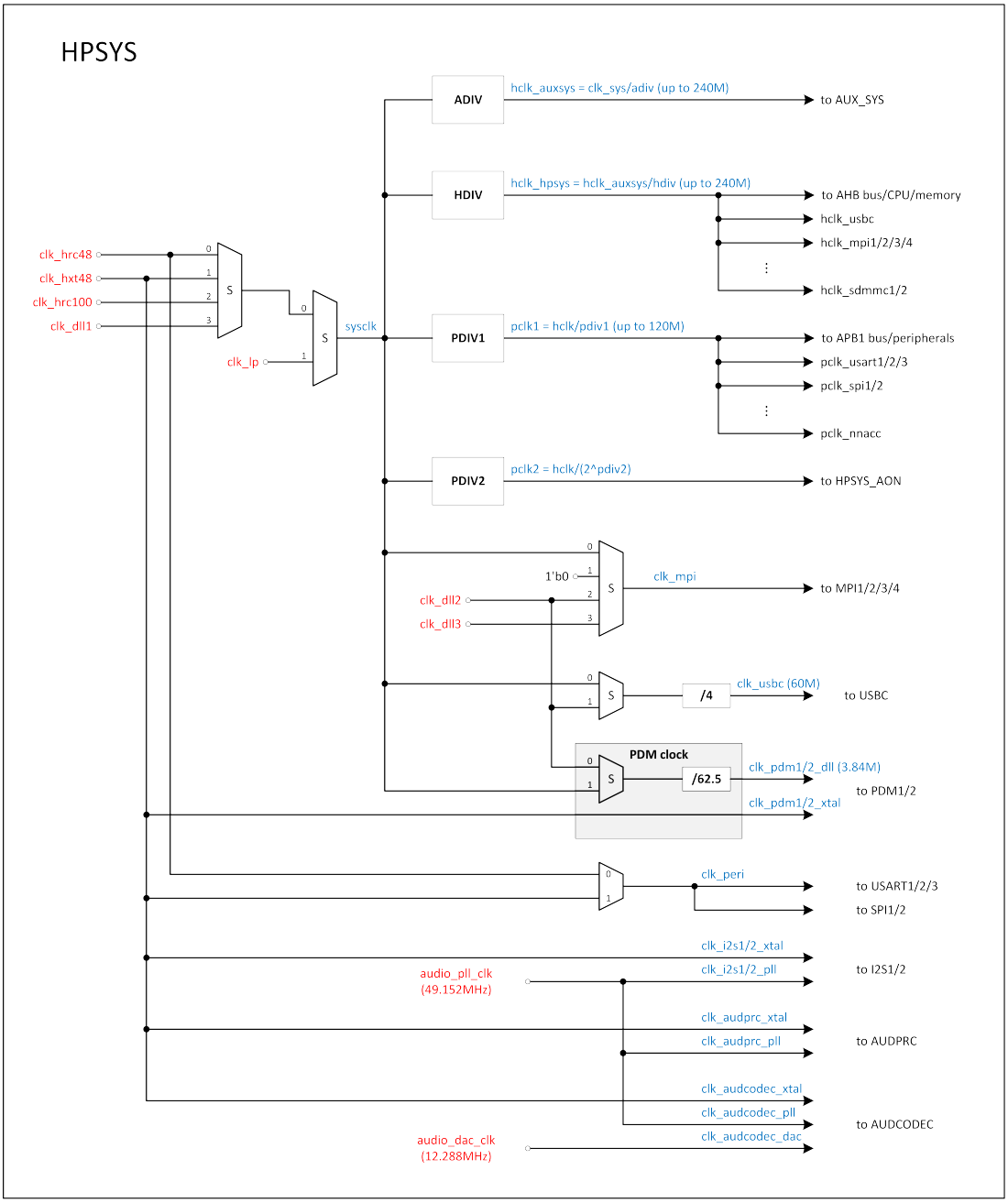


Figure 1-3: Clock Architecture of HPSYS

1.3.3 Memory Type

1.3.3.1 Cache

HCPU has 32KB 2-way I-Cache (Level 1 instruction cache) and 32KB 4-way D-Cache (Level 1 data cache), ACPU has 16KB 2-way I-Cache (Level 1 instruction cache) and 16KB 4-way D-Cache (Level 1 data cache), which can greatly improve CPU execution efficiency during XIP. The MPU (Memory Protection Unit) should be configured appropriately to set the cache address segment and non-cache address segment to balance efficiency and ease of use.

1.3.3.2 TCM

HCPU has 64KB zero-wait-cycle I-TCM with address space 0x0001_0000 –0x0001_FFFF. This TCM memory is exclusive to HCPU, and can't be accessed by other AHB masters. It can be used to place codes and data with high real-time requirements.

HCPU also has 128KB zero-wait-cycle D-TCM with address space 0x2000_0000 –0x2001_FFFF. This TCM memory is connected to the bus and can be accessed by other AHB masters.

1.3.3.3 SRAM

There is a total of 2624KB SRAM on the HPSYS bus, which includes:

- 2048KB HCPU zero-wait-cycle SRAM, address space 0x2000_0000 –0x201F_FFFF (shared with DTCM by 128KB), accessible to all AHB masters. Maximum frequency is 240MHz, which can maximize CPU performance.
- 512KB ACPU zero-wait-cycle SRAM, address space 0x2020_0000 –0x2027_FFFF.
- 64KB Retention SRAM, address space 0x0002_0000 –0x0002_FFFF, can be accessed by HCPU. Maximum frequency is 120MHz. When the system enters low power mode, this SRAM works to ensure no data loss.

1.3.3.4 Off-chip RAM

HPSYS supports external HPI/OPI DDR pSRAM with address space 0x6000_0000 –0x63FF_FFFF, the actual accessible address is determined by the capacity of the external particles. The maximum interface frequency is DDR 144MHz and the data bit width is 16-bit or 8-bit.

1.3.3.5 Off-chip Flash

HPSYS supports external NOR/NAND FLASHs, in which

- 0x6400_0000 –0x67FF_FFFF address segment can be connected to FLASH3, recommended frequency is 72MHz.
- 0x6800_0000 –0x9FFF_FFFF address segment can be connected to FLASH4, recommended frequency is 72MHz.

1.3.4 Address Mapping

Table 1-1: Address Mapping of HPSYS

Category	Memory /IP	Address space	HCPU				LCPU		ACPU			
			Starting Address		Ending Address		Starting Address	Ending Address	Starting Address		Ending Address	
HPSYS_ITCM		**256KB**	**0x0000_0000**		**0x0003_FFFF**		**NA**	**NA**	**NA**		**NA**	
	ROM	64KB	0x0000_0000		0x0000_FFFF		-	-	-		-	
	RAM	64KB	0x0001_0000		0x0001_FFFF		-	-	-		-	
	RAM (Retention)	64KB	0x0002_0000		0x0002_FFFF		-	-	-		-	
	Reserved	-	-		-		-	-	-		-	
External Memory		**1024MB**	**0x1000_0000**	**0x6000_0000**	**0x1BFF_FFFF**	**0x9FFF_FFFF**	**0x6000_0000**	**0x9FFF_FFFF**	**0x6000_0000**		**0x9FFF_FFFF**	
	MPI1 Memory	32MB	0x1000_0000	0x6000_0000	0x11FF_FFFF	0x61FF_FFFF	0x6000_0000	0x61FF_FFFF	0x6000_0000		0x61FF_FFFF	
	MPI2 Memory	32MB	0x1200_0000	0x6200_0000	0x13FF_FFFF	0x63FF_FFFF	0x6200_0000	0x63FF_FFFF	0x6200_0000		0x63FF_FFFF	
	MPI3 Memory	64MB	0x1400_0000	0x6400_0000	0x17FF_FFFF	0x67FF_FFFF	0x6400_0000	0x67FF_FFFF	0x6400_0000		0x67FF_FFFF	
	MPI4 Memory	64MB/896MB	0x1800_0000	0x6800_0000	0x1BFF_FFFF	0x9FFF_FFFF	0x6800_0000	0x9FFF_FFFF	0x6800_0000		0x9FFF_FFFF	
HPSYS_RAM		**2MB**	**0x2000_0000**		**0x2027_FFFF**		**0x2A00_0000**	**0x2A27_FFFF**	**0x0000_0000**	**0x2000_0000**	**0x0007_FFFF**	**0x2027_FFFF**
	RAM0	128KB	0x2000_0000		0x2001_FFFF		0x2A00_0000	0x2A01_FFFF	-	0x2000_0000	-	0x2001_FFFF
	RAM1	128KB	0x2002_0000		0x2003_FFFF		0x2A02_0000	0x2A03_FFFF	-	0x2002_0000	-	0x2003_FFFF
	RAM2	256KB	0x2004_0000		0x2007_FFFF		0x2A04_0000	0x2A07_FFFF	-	0x2004_0000	-	0x2007_FFFF
	RAM3	512KB	0x2008_0000		0x200F_FFFF		0x2A08_0000	0x2A0F_FFFF	-	0x2008_0000	-	0x200F_FFFF
	RAM4	512KB	0x2010_0000		0x2017_FFFF		0x2A10_0000	0x2A17_FFFF	-	0x2010_0000	-	0x2017_FFFF
	RAM5	512KB	0x2018_0000		0x201F_FFFF		0x2A18_0000	0x2A1F_FFFF	-	0x2018_0000	-	0x201F_FFFF
	RAM6 (ACPU)	128KB	0x2020_0000		0x2021_FFFF		0x2A20_0000	0x2A21_FFFF	0x0000_0000	0x2020_0000	0x0001_FFFF	0x2021_FFFF
	RAM7 (ACPU)	128KB	0x2022_0000		0x2023_FFFF		0x2A22_0000	0x2A23_FFFF	0x0002_0000	0x2022_0000	0x0003_FFFF	0x2023_FFFF
	RAM8 (ACPU)	128KB	0x2024_0000		0x2025_FFFF		0x2A24_0000	0x2A25_FFFF	0x0004_0000	0x2024_0000	0x0005_FFFF	0x2025_FFFF
	RAM9 (ACPU)	128KB	0x2026_0000		0x2027_FFFF		0x2A26_0000	0x2A27_FFFF	0x0006_0000	0x2026_0000	0x0007_FFFF	0x2027_FFFF
HPSYS_APB1		**256KB**	**0x4000_0000**		**0x4003_FFFF**		**0x4000_0000**	**0x4003_FFFF**	**0x4003_0000**		**0x4003_FFFF**	
	RCC1	4KB	0x4000_0000		0x4000_0FFF		0x4000_0000	0x4000_0FFF	0x4000_0000		0x4000_0FFF	
	DMAC1	4KB	0x4000_1000		0x4000_1FFF		0x4000_1000	0x4000_1FFF	0x4000_1000		0x4000_1FFF	
	MAILBOX1	4KB	0x4000_2000		0x4000_2FFF		0x4000_2000	0x4000_2FFF	0x4000_2000		0x4000_2FFF	
	PINMUX1	4KB	0x4000_3000		0x4000_3FFF		0x4000_3000	0x4000_3FFF	0x4000_3000		0x4000_3FFF	
	USART1	4KB	0x4000_4000		0x4000_4FFF		0x4000_4000	0x4000_4FFF	0x4000_4000		0x4000_4FFF	
	USART2	4KB	0x4000_5000		0x4000_5FFF		0x4000_5000	0x4000_5FFF	0x4000_5000		0x4000_5FFF	
	EZIP1	4KB	0x4000_6000		0x4000_6FFF		0x4000_6000	0x4000_6FFF	0x4000_6000		0x4000_6FFF	
	EPIC	4KB	0x4000_7000		0x4000_7FFF		0x4000_7000	0x4000_7FFF	0x4000_7000		0x4000_7FFF	
	LCDC1	4KB	0x4000_8000		0x4000_8FFF		0x4000_8000	0x4000_8FFF	0x4000_8000		0x4000_8FFF	
	I2S1	4KB	0x4000_9000		0x4000_9FFF		0x4000_9000	0x4000_9FFF	0x4000_9000		0x4000_9FFF	
	I2S2	4KB	0x4000_A000		0x4000_AFFF		0x4000_A000	0x4000_AFFF	0x4000_A000		0x4000_AFFF	
	SYSCFG1	4KB	0x4000_B000		0x4000_BFFF		0x4000_B000	0x4000_BFFF	0x4000_B000		0x4000_BFFF	
	EFUSEC	4KB	0x4000_C000		0x4000_CFFF		0x4000_C000	0x4000_CFFF	0x4000_C000		0x4000_CFFF	
	AES	4KB	0x4000_D000		0x4000_DFFF		0x4000_D000	0x4000_DFFF	0x4000_D000		0x4000_DFFF	
	Reserved	4KB	0x4000_E000		0x4000_EFFF		0x4000_E000	0x4000_EFFF	0x4000_E000		0x4000_EFFF	
	TRNG	4KB	0x4000_F000		0x4000_FFFF		0x4000_F000	0x4000_FFFF	0x4000_F000		0x4000_FFFF	
	GPTIM1	4KB	0x4001_0000		0x4001_0FFF		0x4001_0000	0x4001_0FFF	0x4001_0000		0x4001_0FFF	
	GPTIM2	4KB	0x4001_1000		0x4001_1FFF		0x4001_1000	0x4001_1FFF	0x4001_1000		0x4001_1FFF	
	BTIM1	4KB	0x4001_2000		0x4001_2FFF		0x4001_2000	0x4001_2FFF	0x4001_2000		0x4001_2FFF	
	BTIM2	4KB	0x4001_3000		0x4001_3FFF		0x4001_3000	0x4001_3FFF	0x4001_3000		0x4001_3FFF	
	WDT1	4KB	0x4001_4000		0x4001_4FFF		0x4001_4000	0x4001_4FFF	0x4001_4000		0x4001_4FFF	
	SPI1	4KB	0x4001_5000		0x4001_5FFF		0x4001_5000	0x4001_5FFF	0x4001_5000		0x4001_5FFF	
	SPI2	4KB	0x4001_6000		0x4001_6FFF		0x4001_6000	0x4001_6FFF	0x4001_6000		0x4001_6FFF	
	EXTDMA	4KB	0x4001_7000		0x4001_7FFF		0x4001_7000	0x4001_7FFF	0x4001_7000		0x4001_7FFF	
	DMAC2	4KB	0x4001_8000		0x4001_8FFF		0x4001_8000	0x4001_8FFF	0x4001_8000		0x4001_8FFF	
	NNACC1	4KB	0x4001_9000		0x4001_9FFF		0x4001_9000	0x4001_9FFF	0x4001_9000		0x4001_9FFF	
	PDM1	4KB	0x4001_A000		0x4001_AFFF		0x4001_A000	0x4001_AFFF	0x4001_A000		0x4001_AFFF	
	PDM2	4KB	0x4001_B000		0x4001_BFFF		0x4001_B000	0x4001_BFFF	0x4001_B000		0x4001_BFFF	
	I2C1	4KB	0x4001_C000		0x4001_CFFF		0x4001_C000	0x4001_CFFF	0x4001_C000		0x4001_CFFF	
	I2C2	4KB	0x4001_D000		0x4001_DFFF		0x4001_D000	0x4001_DFFF	0x4001_D000		0x4001_DFFF	
	DSIHOST	4KB	0x4001_E000		0x4001_EFFF		0x4001_E000	0x4001_EFFF	0x4001_E000		0x4001_EFFF	
	DSIPHY	4KB	0x4001_F000		0x4001_FFFF		0x4001_F000	0x4001_FFFF	0x4001_F000		0x4001_FFFF	
	PTC1	4KB	0x4002_0000		0x4002_0FFF		0x4002_0000	0x4002_0FFF	0x4002_0000		0x4002_0FFF	

Continued on the next page

Table 1-1: Address Mapping of HPSYS (continued)

Category	Memory /IP	Address space	HCPU		LCPU		ACPU	
			Starting Address	Ending Address	Starting Address	Ending Address	Starting Address	Ending Address
	BUSMON1	4KB	0x4002_1000	0x4002_1FFF	0x4002_1000	0x4002_1FFF	0x4002_1000	0x4002_1FFF
	I2C3	4KB	0x4002_2000	0x4002_2FFF	0x4002_2000	0x4002_2FFF	0x4002_2000	0x4002_2FFF
	ATIM1	4KB	0x4002_3000	0x4002_3FFF	0x4002_3000	0x4002_3FFF	0x4002_3000	0x4002_3FFF
	ATIM2	4KB	0x4002_4000	0x4002_4FFF	0x4002_4000	0x4002_4FFF	0x4002_4000	0x4002_4FFF
	AUDPRC	4KB	0x4002_5000	0x4002_5FFF	0x4002_5000	0x4002_5FFF	0x4002_5000	0x4002_5FFF
	AUDCODEC	4KB	0x4002_6000	0x4002_6FFF	0x4002_6000	0x4002_6FFF	0x4002_6000	0x4002_6FFF
	FFT1	4KB	0x4002_7000	0x4002_7FFF	0x4002_7000	0x4002_7FFF	0x4002_7000	0x4002_7FFF
	FACC1	4KB	0x4002_8000	0x4002_8FFF	0x4002_8000	0x4002_8FFF	0x4002_8000	0x4002_8FFF
	USART3	4KB	0x4002_9000	0x4002_9FFF	0x4002_9000	0x4002_9FFF	0x4002_9000	0x4002_9FFF
	EZIP2	4KB	0x4002_A000	0x4002_AFFF	0x4002_A000	0x4002_AFFF	0x4002_A000	0x4002_AFFF
	CAN1	4KB	0x4002_B000	0x4002_BFFF	0x4002_B000	0x4002_BFFF	0x4002_B000	0x4002_BFFF
	CAN2	4KB	0x4002_C000	0x4002_CFFF	0x4002_C000	0x4002_CFFF	0x4002_C000	0x4002_CFFF
	SCI	4KB	0x4002_D000	0x4002_DFFF	0x4002_D000	0x4002_DFFF	0x4002_D000	0x4002_DFFF
	BUSMON2	4KB	0x4002_E000	0x4002_EFFF	0x4002_E000	0x4002_EFFF	0x4002_E000	0x4002_EFFF
	I2C4	4KB	0x4002_F000	0x4002_FFFF	0x4002_E000	0x4002_FFFF	0x4002_E000	0x4002_FFFF
	Reserved	64KB	0x4003_0000	0x4003_FFFF	0x4003_0000	0x4003_FFFF	0x4003_0000	0x4003_FFFF
HPSYS_APB2		**256KB**	**0x4004_0000**	**0x4007_FFFF**	**0x4004_0000**	**0x4007_FFFF**	**0x4004_0000**	**0x4007_FFFF**
	HPSYS_AON	4KB	0x4004_0000	0x4004_0FFF	0x4004_0000	0x4004_0FFF	0x4004_0000	0x4004_0FFF
	LPTIM1	4KB	0x4004_1000	0x4004_1FFF	0x4004_1000	0x4004_1FFF	0x4004_1000	0x4004_1FFF
	Reserved	4KB	0x4004_2000	0x4004_2FFF	0x4004_2000	0x4004_2FFF	0x4004_2000	0x4004_2FFF
	Reserved	52KB	0x4004_3000	0x4004_FFFF	0x4004_3000	0x4004_FFFF	0x4004_3000	0x4004_FFFF
	Reserved	64KB	0x4005_0000	0x4005_FFFF	0x4005_0000	0x4005_FFFF	0x4005_0000	0x4005_FFFF
	Reserved	64KB	0x4006_0000	0x4006_FFFF	0x4006_0000	0x4006_FFFF	0x4006_0000	0x4006_FFFF
	Reserved	64KB	0x4007_0000	0x4007_FFFF	0x4007_0000	0x4007_FFFF	0x4007_0000	0x4007_FFFF
HPSYS_AHB		**256KB**	**0x4008_0000**	**0x400B_FFFF**	**0x4008_0000**	**0x400B_FFFF**	**0x4008_0000**	**0x400B_FFFF**
	GPIO1	4KB	0x4008_0000	0x4008_0FFF	0x4008_0000	0x4008_0FFF	0x4008_0000	0x4008_0FFF
	MPI1	4KB	0x4008_1000	0x4008_1FFF	0x4008_1000	0x4008_1FFF	0x4008_1000	0x4008_1FFF
	MPI2	4KB	0x4008_2000	0x4008_2FFF	0x4008_2000	0x4008_2FFF	0x4008_2000	0x4008_2FFF
	MPI3	4KB	0x4008_3000	0x4008_3FFF	0x4008_3000	0x4008_3FFF	0x4008_3000	0x4008_3FFF
	MPI4	4KB	0x4008_4000	0x4008_4FFF	0x4008_4000	0x4008_4FFF	0x4008_4000	0x4008_4FFF
	SDMMC1	4KB	0x4008_5000	0x4008_5FFF	0x4008_5000	0x4008_5FFF	0x4008_5000	0x4008_5FFF
	SDMMC2	4KB	0x4008_6000	0x4008_6FFF	0x4008_6000	0x4008_6FFF	0x4008_6000	0x4008_6FFF
	USBC	4KB	0x4008_7000	0x4008_7FFF	0x4008_7000	0x4008_7FFF	0x4008_7000	0x4008_7FFF
	V2D_GPU	4KB	0x4008_8000	0x4008_8FFF	0x4008_8000	0x4008_8FFF	0x4008_8000	0x4008_8FFF
	JPEG_ENC	4KB	0x4008_9000	0x4008_9FFF	0x4008_9000	0x4008_9FFF	0x4008_9000	0x4008_9FFF
	JPEG_DEC	4KB	0x4008_A000	0x4008_AFFF	0x4008_A000	0x4008_AFFF	0x4008_A000	0x4008_AFFF
	CRC1	4KB	0x4008_B000	0x4008_BFFF	0x4008_B000	0x4008_BFFF	0x4008_B000	0x4008_BFFF
	Reserved	16KB	0x4008_C000	0x4008_FFFF	0x4008_C000	0x4008_FFFF	0x4008_C000	0x4008_FFFF
	GFX_RAM	64KB	0x4009_0000	0x4009_FFFF	0x4009_0000	0x4009_FFFF	0x4009_0000	0x4009_FFFF
	Reserved	128KB	0x400A_0000	0x400B_FFFF	0x400A_0000	0x400B_FFFF	0x400A_0000	0x400B_FFFF

1.3.5 Interrupt List

Table 1-2: Interrupt List of HCPU

IRQ #	IRQ Source
NMI	WDT1
IRQ[0]	AON
IRQ[1]	LCPU_IRQ[1]
IRQ[2]	LCPU_IRQ[2]
IRQ[3]	LCPU_IRQ[3]
IRQ[4]	LCPU_IRQ[4]
IRQ[5]	LCPU_IRQ[5]
IRQ[6]	LCPU_IRQ[6]
IRQ[7]	LCPU_IRQ[7]
IRQ[8]	LCPU_IRQ[8]
IRQ[9]	LCPU_IRQ[9]
IRQ[10]	LCPU_IRQ[10]
IRQ[11]	LCPU_IRQ[11]
IRQ[12]	LCPU_IRQ[12]
IRQ[13]	LCPU_IRQ[13]
IRQ[14]	LCPU_IRQ[14]
IRQ[15]	LCPU_IRQ[15]
IRQ[16]	LCPU_IRQ[16]
IRQ[17]	LCPU_IRQ[17]
IRQ[18]	LCPU_IRQ[18]
IRQ[19]	LCPU_IRQ[19]
IRQ[20]	LCPU_IRQ[20]
IRQ[21]	LCPU_IRQ[21]
IRQ[22]	LCPU_IRQ[22]
IRQ[23]	LCPU_IRQ[23]
IRQ[24]	LCPU_IRQ[24]
IRQ[25]	LCPU_IRQ[25]
IRQ[26]	LCPU_IRQ[26]
IRQ[27]	LCPU_IRQ[27]
IRQ[28]	LCPU_IRQ[28]
IRQ[29]	LCPU_IRQ[29]
IRQ[30]	LCPU_IRQ[30]
IRQ[31]	LCPU_IRQ[31]
IRQ[32]	LCPU_IRQ[32]
IRQ[33]	LCPU_IRQ[33]
IRQ[34]	LCPU_IRQ[34]
IRQ[35]	LCPU_IRQ[35]
IRQ[36]	LCPU_IRQ[36]
IRQ[37]	LCPU_IRQ[37]
IRQ[38]	LCPU_IRQ[38]
IRQ[39]	LCPU_IRQ[39]
IRQ[40]	LCPU_IRQ[40]
IRQ[41]	LCPU_IRQ[41]
IRQ[42]	LCPU_IRQ[42]
IRQ[43]	LCPU_IRQ[43]
IRQ[44]	LCPU_IRQ[44]
IRQ[45]	LCPU_IRQ[45]
IRQ[46]	LPTIM1
IRQ[47]	rsvd

Continued on the next page

Table 1-2: Interrupt List of HCPU (continued)

IRQ #	IRQ Source
IRQ[48]	rsvd
IRQ[49]	RTC
IRQ[50]	DMAC1_CH1
IRQ[51]	DMAC1_CH2
IRQ[52]	DMAC1_CH3
IRQ[53]	DMAC1_CH4
IRQ[54]	DMAC1_CH5
IRQ[55]	DMAC1_CH6
IRQ[56]	DMAC1_CH7
IRQ[57]	DMAC1_CH8
IRQ[58]	LCPU2HCPU
IRQ[59]	USART1
IRQ[60]	SPI1
IRQ[61]	I2C1
IRQ[62]	EPIC
IRQ[63]	LCDC1
IRQ[64]	I2S1
IRQ[65]	I2S2
IRQ[66]	EFUSEC
IRQ[67]	AES
IRQ[68]	PTC1
IRQ[69]	TRNG
IRQ[70]	GPTIM1
IRQ[71]	GPTIM2
IRQ[72]	BTIM1
IRQ[73]	BTIM2
IRQ[74]	USART2
IRQ[75]	SPI2
IRQ[76]	I2C2
IRQ[77]	EXTDMA
IRQ[78]	ACPU2HCPU
IRQ[79]	SDMMC1
IRQ[80]	SDMMC2
IRQ[81]	NNACC1
IRQ[82]	PDM1
IRQ[83]	DSI
IRQ[84]	GPIO1
IRQ[85]	MPI1
IRQ[86]	MPI2
IRQ[87]	MPI3
IRQ[88]	MPI4
IRQ[89]	EZIP1
IRQ[90]	EZIP2
IRQ[91]	PDM2
IRQ[92]	USBC
IRQ[93]	I2C3
IRQ[94]	ATIM1
IRQ[95]	ATIM2
IRQ[96]	DMAC2_CH1
IRQ[97]	DMAC2_CH2
IRQ[98]	DMAC2_CH3
IRQ[99]	DMAC2_CH4

Continued on the next page

Table 1-2: Interrupt List of HCPU (continued)

IRQ #	IRQ Source
IRQ[100]	DMAC2_CH5
IRQ[101]	DMAC2_CH6
IRQ[102]	DMAC2_CH7
IRQ[103]	DMAC2_CH8
IRQ[104]	V2D_GPU
IRQ[105]	JPEG_ENC
IRQ[106]	JPEG_DEC
IRQ[107]	USART3
IRQ[108]	FFT1
IRQ[109]	FACC1
IRQ[110]	CAN1
IRQ[111]	CAN2
IRQ[112]	AUDPRC
IRQ[113]	AUD_HP
IRQ[114]	SCI
IRQ[115]	I2C4

Table 1-3: Interrupt List of ACPU

IRQ #	IRQ Source
NMI	WDT1
IRQ[0]	AON
IRQ[1]	LCPU_IRQ[1]
IRQ[2]	LCPU_IRQ[2]
IRQ[3]	LCPU_IRQ[3]
IRQ[4]	LCPU_IRQ[4]
IRQ[5]	LCPU_IRQ[5]
IRQ[6]	LCPU_IRQ[6]
IRQ[7]	LCPU_IRQ[7]
IRQ[8]	LCPU_IRQ[8]
IRQ[9]	LCPU_IRQ[9]
IRQ[10]	LCPU_IRQ[10]
IRQ[11]	LCPU_IRQ[11]
IRQ[12]	LCPU_IRQ[12]
IRQ[13]	LCPU_IRQ[13]
IRQ[14]	LCPU_IRQ[14]
IRQ[15]	LCPU_IRQ[15]
IRQ[16]	LCPU_IRQ[16]
IRQ[17]	LCPU_IRQ[17]
IRQ[18]	LCPU_IRQ[18]
IRQ[19]	LCPU_IRQ[19]
IRQ[20]	LCPU_IRQ[20]
IRQ[21]	LCPU_IRQ[21]
IRQ[22]	LCPU_IRQ[22]
IRQ[23]	LCPU_IRQ[23]
IRQ[24]	LCPU_IRQ[24]
IRQ[25]	LCPU_IRQ[25]
IRQ[26]	LCPU_IRQ[26]
IRQ[27]	LCPU_IRQ[27]
IRQ[28]	LCPU_IRQ[28]
IRQ[29]	LCPU_IRQ[29]
IRQ[30]	LCPU_IRQ[30]

Continued on the next page

Table 1-3: Interrupt List of ACPU (continued)

IRQ #	IRQ Source
IRQ[31]	LCPU_IRQ[31]
IRQ[32]	LCPU_IRQ[32]
IRQ[33]	LCPU_IRQ[33]
IRQ[34]	LCPU_IRQ[34]
IRQ[35]	LCPU_IRQ[35]
IRQ[36]	LCPU_IRQ[36]
IRQ[37]	LCPU_IRQ[37]
IRQ[38]	LCPU_IRQ[38]
IRQ[39]	LCPU_IRQ[39]
IRQ[40]	LCPU_IRQ[40]
IRQ[41]	LCPU_IRQ[41]
IRQ[42]	LCPU_IRQ[42]
IRQ[43]	LCPU_IRQ[43]
IRQ[44]	LCPU_IRQ[44]
IRQ[45]	LCPU_IRQ[45]
IRQ[46]	LPTIM1
IRQ[47]	rsvd
IRQ[48]	rsvd
IRQ[49]	RTC
IRQ[50]	DMAC1_CH1
IRQ[51]	DMAC1_CH2
IRQ[52]	DMAC1_CH3
IRQ[53]	DMAC1_CH4
IRQ[54]	DMAC1_CH5
IRQ[55]	DMAC1_CH6
IRQ[56]	DMAC1_CH7
IRQ[57]	DMAC1_CH8
IRQ[58]	LCPU2ACPU
IRQ[59]	USART1
IRQ[60]	SPI1
IRQ[61]	I2C1
IRQ[62]	EPIC
IRQ[63]	LCDC1
IRQ[64]	I2S1
IRQ[65]	I2S2
IRQ[66]	EFUSEC
IRQ[67]	AES
IRQ[68]	PTC1
IRQ[69]	TRNG
IRQ[70]	GPTIM1
IRQ[71]	GPTIM2
IRQ[72]	BTIM1
IRQ[73]	BTIM2
IRQ[74]	USART2
IRQ[75]	SPI2
IRQ[76]	I2C2
IRQ[77]	EXTDMA
IRQ[78]	HCPU2ACPU
IRQ[79]	SDMMC1
IRQ[80]	SDMMC2
IRQ[81]	NNACC1
IRQ[82]	PDM1

Continued on the next page

Table 1-3: Interrupt List of ACPU (continued)

IRQ #	IRQ Source
IRQ[83]	DSI
IRQ[84]	GPIO1
IRQ[85]	MPI1
IRQ[86]	MPI2
IRQ[87]	MPI3
IRQ[88]	MPI4
IRQ[89]	EZIP1
IRQ[90]	EZIP2
IRQ[91]	PDM2
IRQ[92]	USBC
IRQ[93]	I2C3
IRQ[94]	ATIM1
IRQ[95]	ATIM2
IRQ[96]	DMAC2_CH1
IRQ[97]	DMAC2_CH2
IRQ[98]	DMAC2_CH3
IRQ[99]	DMAC2_CH4
IRQ[100]	DMAC2_CH5
IRQ[101]	DMAC2_CH6
IRQ[102]	DMAC2_CH7
IRQ[103]	DMAC2_CH8
IRQ[104]	V2D_GPU
IRQ[105]	JPEG_ENC
IRQ[106]	JPEG_DEC
IRQ[107]	USART3
IRQ[108]	FFT1
IRQ[109]	FACC1
IRQ[110]	CAN1
IRQ[111]	CAN2
IRQ[112]	AUDPRC
IRQ[113]	AUD_HP
IRQ[114]	SCI
IRQ[115]	I2C4

1.4 Low-Power Processor (LITTLE Core) System (LPSYS)

1.4.1 Bus Architecture

The LPSYS provides an internal bus matrix based on the AHB protocol, which supports multiple master devices to access the address spaces of multiple slave devices in parallel.

LCPU and DMAC3 has access to all address spaces of LPSYS, and can access the address spaces of HPSYS (except HPSYS_ITCM and Retention RAM) via LP2HP.

Some master devices of HPSYS can access the address spaces of LPSYS through HP2LP.

LPSYS_ITCM and LPSYS_DTCM can be accessed by LCPU and DMAC3, and also by some master devices of the HPSYS.

When multiple master devices access the address space of the same slave device at the same time, the access order will be determined based on the polling arbitration principle.

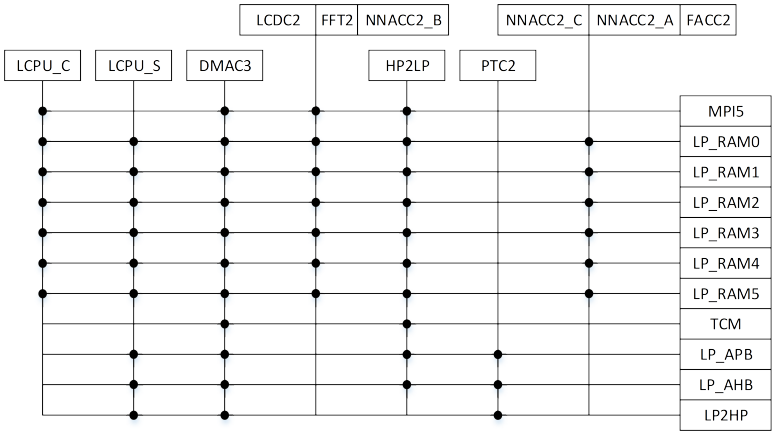


Figure 1-4: Bus Architecture of LPSYS

1.4.2 Clock Architecture

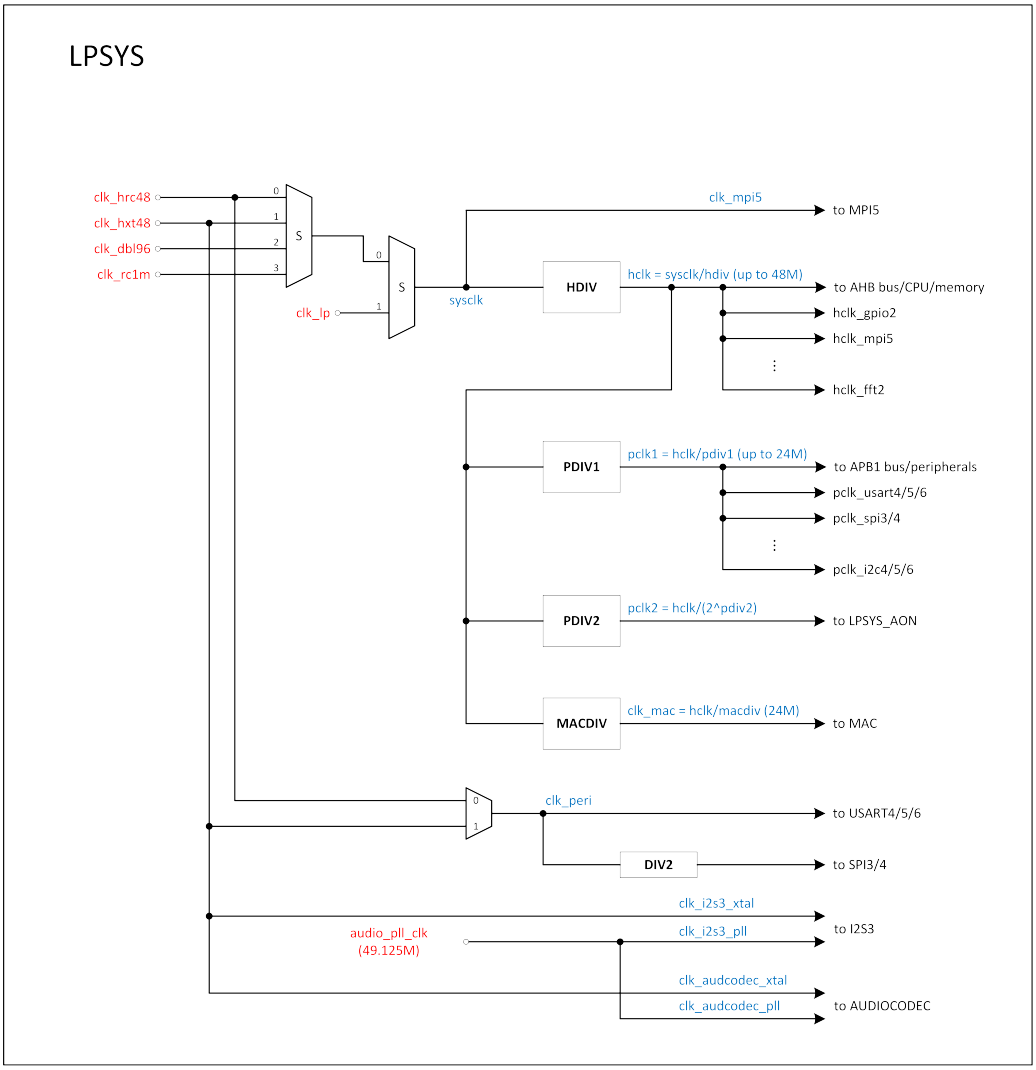


Figure 1-5: Clock Architecture of LPSYS

1.4.3 Memory Type

1.4.3.1 Cache

LCPU has 16KB 2-way I-Cache (Level 1 instruction cache) and 16KB 4-way D-Cache (Level 1 data cache).

1.4.3.2 TCM

LCPU has 16KB zero-wait-cycle I-TCM with address space 0x003F_C000 –0x003F_FFFF. This TCM memory is exclusive to LCPU and can be initialized by HCPU via address segments 0x20BF_C000 –0x20BF_FFFF. It is recommended to place codes and data with high real-time (or delay determinism) requirements.

LCPU also has 16KB zero-wait-cycle D-TCM with address space 0x203F_C000 –0x203F_FFFF. This TCM memory is exclusive to LCPU and can be initialized by HCPU via the same address segment.

1.4.3.3 SRAM

There is a total of 1024KB one-wait-cycle SRAM on LPSYS bus, and the address space is 0x2040_0000–0x204F_FFFF.

1.4.3.4 Off-chip Flash

LPSYS supports external NOR FLASH for system startup, with address space 0x1C00_0000 –0x1FFF_FFFF.

1.4.4 Address Mapping

Table 1-4: Address Mapping of LPSYS

Category	Memory /IP	Address space	HCPU				LCPU				ACPU			
			Starting Address		Ending Address		Starting Address		Ending Address		Starting Address		Ending Address	
LPSYS_ITCM		**4MB**	**0x2080_0000**		**0x20BF_FFFF**		**0x0000_0000**		**0x003F_FFFF**		**0x2080_0000**		**0x20BF_FFFF**	
	ROM	1MB	0x2080_0000		0x208F_FFFF		0x0000_0000		0x000F_FFFF		0x2080_0000		0x208F_FFFF	
	Reserved	-	-		-		-		-		-		-	
	RAM	16KB	0x20BF_C000		0x20BF_FFFF		0x003F_C000		0x003F_FFFF		0x20BF_C000		0x20BF_FFFF	
LPSYS_DTCM		**4MB**	**0x2000_0000**		**0x203F_FFFF**		**0x2000_0000**		**0x203F_FFFF**		**0x2000_0000**		**0x203F_FFFF**	
	Reserved	-	-		-		-		-		-		-	
	RAM	16KB	0x203F_C000		0x203F_FFFF		0x203F_C000		0x203F_FFFF		0x203F_C000		0x203F_FFFF	
External Memory		**64MB**	**0x1C00_0000**		**0x1FFF_FFFF**		**0x1C00_0000**		**0x1FFF_FFFF**		**0x1C00_0000**		**0x1FFF_FFFF**	
	MPI5 Memory	64MB	0x1C00_0000		0x1FFF_FFFF		0x1C00_0000		0x1FFF_FFFF		0x1C00_0000		0x1FFF_FFFF	
LPSYS_RAM		**1MB**	**0x20C0_0000**	**0x2040_0000**	**0x20CF_FFFF**	**0x204F_FFFF**	**0x0040_0000**	**0x2040_0000**	**0x004F_FFFF**	**0x204F_FFFF**	**0x20C0_0000**	**0x2040_0000**	**0x20CF_FFFF**	**0x204F_FFFF**
	RAM0	128KB	0x20C0_0000	0x2040_0000	0x20C1_FFFF	0x2041_FFFF	0x0040_0000	0x2040_0000	0x0041_FFFF	0x2041_FFFF	0x20C0_0000	0x2040_0000	0x20C1_FFFF	0x2041_FFFF
	RAM1	128KB	0x20C2_0000	0x2042_0000	0x20C3_FFFF	0x2043_FFFF	0x0042_0000	0x2042_0000	0x0043_FFFF	0x2043_FFFF	0x20C2_0000	0x2042_0000	0x20C3_FFFF	0x2043_FFFF
	RAM2	256KB	0x20C4_0000	0x2044_0000	0x20C7_FFFF	0x2047_FFFF	0x0044_0000	0x2044_0000	0x0047_FFFF	0x2047_FFFF	0x20C4_0000	0x2044_0000	0x20C7_FFFF	0x2047_FFFF
	RAM3	256KB	0x20C8_0000	0x2048_0000	0x20CB_FFFF	0x204B_FFFF	0x0048_0000	0x2048_0000	0x004B_FFFF	0x204B_FFFF	0x20C8_0000	0x2048_0000	0x20CB_FFFF	0x204B_FFFF
	RAM4	128KB	0x20CC_0000	0x204C_0000	0x20CD_FFFF	0x204D_FFFF	0x004C_0000	0x204C_0000	0x004D_FFFF	0x204D_FFFF	0x20CC_0000	0x204C_0000	0x20CD_FFFF	0x204D_FFFF
	RAM5 (EM)	128KB	0x20CE_0000	0x204E_0000	0x20CF_FFFF	0x204F_FFFF	0x004E_0000	0x204E_0000	0x004F_FFFF	0x204F_FFFF	0x20CE_0000	0x204E_0000	0x20CF_FFFF	0x204F_FFFF
LPSYS_APB1		**192KB**	**0x5000_0000**		**0x5003_FFFF**		**0x5000_0000**		**0x5003_FFFF**		**0x5000_0000**		**0x5003_FFFF**	
	RCC2	4KB	0x5000_0000		0x5000_0FFF		0x5000_0000		0x5000_0FFF		0x5000_0000		0x5000_0FFF	
	DMAC3	4KB	0x5000_1000		0x5000_1FFF		0x5000_1000		0x5000_1FFF		0x5000_1000		0x5000_1FFF	
	MAILBOX2	4KB	0x5000_2000		0x5000_2FFF		0x5000_2000		0x5000_2FFF		0x5000_2000		0x5000_2FFF	
	PINMUX2	4KB	0x5000_3000		0x5000_3FFF		0x5000_3000		0x5000_3FFF		0x5000_3000		0x5000_3FFF	
	PATCH	4KB	0x5000_4000		0x5000_4FFF		0x5000_4000		0x5000_4FFF		0x5000_4000		0x5000_4FFF	
	USART4	4KB	0x5000_5000		0x5000_5FFF		0x5000_5000		0x5000_5FFF		0x5000_5000		0x5000_5FFF	
	USART5	4KB	0x5000_6000		0x5000_6FFF		0x5000_6000		0x5000_6FFF		0x5000_6000		0x5000_6FFF	
	USART6	4KB	0x5000_7000		0x5000_7FFF		0x5000_7000		0x5000_7FFF		0x5000_7000		0x5000_7FFF	
	I2S3	4KB	0x5000_8000		0x5000_8FFF		0x5000_8000		0x5000_8FFF		0x5000_8000		0x5000_8FFF	
	SPI3	4KB	0x5000_9000		0x5000_9FFF		0x5000_9000		0x5000_9FFF		0x5000_9000		0x5000_9FFF	
	SPI4	4KB	0x5000_A000		0x5000_AFFF		0x5000_A000		0x5000_AFFF		0x5000_A000		0x5000_AFFF	
	WDT2	4KB	0x5000_B000		0x5000_BFFF		0x5000_B000		0x5000_BFFF		0x5000_B000		0x5000_BFFF	
	I2C5	4KB	0x5000_C000		0x5000_CFFF		0x5000_C000		0x5000_CFFF		0x5000_C000		0x5000_CFFF	
	I2C6	4KB	0x5000_D000		0x5000_DFFF		0x5000_D000		0x5000_DFFF		0x5000_D000		0x5000_DFFF	
	I2C7	4KB	0x5000_E000		0x5000_EFFF		0x5000_E000		0x5000_EFFF		0x5000_E000		0x5000_EFFF	
	SYSCFG2	4KB	0x5000_F000		0x5000_FFFF		0x5000_F000		0x5000_FFFF		0x5000_F000		0x5000_FFFF	
	GPTIM3	4KB	0x5001_0000		0x5001_0FFF		0x5001_0000		0x5001_0FFF		0x5001_0000		0x5001_0FFF	
	GPTIM4	4KB	0x5001_1000		0x5001_1FFF		0x5001_1000		0x5001_1FFF		0x5001_1000		0x5001_1FFF	
	GPTIM5	4KB	0x5001_2000		0x5001_2FFF		0x5001_2000		0x5001_2FFF		0x5001_2000		0x5001_2FFF	
	BTIM3	4KB	0x5001_3000		0x5001_3FFF		0x5001_3000		0x5001_3FFF		0x5001_3000		0x5001_3FFF	
	BTIM4	4KB	0x5001_4000		0x5001_4FFF		0x5001_4000		0x5001_4FFF		0x5001_4000		0x5001_4FFF	
	NNACC2	4KB	0x5001_5000		0x5001_5FFF		0x5001_5000		0x5001_5FFF		0x5001_5000		0x5001_5FFF	
	GPADC	4KB	0x5001_6000		0x5001_6FFF		0x5001_6000		0x5001_6FFF		0x5001_6000		0x5001_6FFF	
	SDADC	4KB	0x5001_7000		0x5001_7FFF		0x5001_7000		0x5001_7FFF		0x5001_7000		0x5001_7FFF	
	AUDADC	4KB	0x5001_8000		0x5001_8FFF		0x5001_8000		0x5001_8FFF		0x5001_8000		0x5001_8FFF	
	LPCOMP	4KB	0x5001_9000		0x5001_9FFF		0x5001_9000		0x5001_9FFF		0x5001_9000		0x5001_9FFF	
	TSEN	4KB	0x5001_A000		0x5001_AFFF		0x5001_A000		0x5001_AFFF		0x5001_A000		0x5001_AFFF	
	PTC2	4KB	0x5001_B000		0x5001_BFFF		0x5001_B000		0x5001_BFFF		0x5001_B000		0x5001_BFFF	
	LCDC2	4KB	0x5001_C000		0x5001_CFFF		0x5001_C000		0x5001_CFFF		0x5001_C000		0x5001_CFFF	
	BUSMON3	4KB	0x5001_D000		0x5001_DFFF		0x5001_D000		0x5001_DFFF		0x5001_D000		0x5001_DFFF	
	FFT2	4KB	0x5001_E000		0x5001_EFFF		0x5001_E000		0x5001_EFFF		0x5001_E000		0x5001_EFFF	
	FACC2	4KB	0x5001_F000		0x5001_FFFF		0x5001_F000		0x5001_FFFF		0x5001_F000		0x5001_FFFF	
	Reserved	64KB	0x5002_0000		0x5002_FFFF		0x5002_0000		0x5002_FFFF		0x5002_0000		0x5002_FFFF	
	Reserved	64KB	0x5003_0000		0x5003_FFFF		0x5003_0000		0x5003_FFFF		0x5003_0000		0x5003_FFFF	
LPSYS_APB2		**64KB**	**0x5004_0000**		**0x5007_FFFF**		**0x5004_0000**		**0x5007_FFFF**		**0x5004_0000**		**0x5007_FFFF**	
	LPSYS_AON	4KB	0x5004_0000		0x5004_0FFF		0x5004_0000		0x5004_0FFF		0x5004_0000		0x5004_0FFF	
	LPTIM2	4KB	0x5004_1000		0x5004_1FFF		0x5004_1000		0x5004_1FFF		0x5004_1000		0x5004_1FFF	
	LPTIM3	4KB	0x5004_2000		0x5004_2FFF		0x5004_2000		0x5004_2FFF		0x5004_2000		0x5004_2FFF	

Continued on the next page

Table 1-4: Address Mapping of LPSYS (continued)

Category	Memory /IP	Address space	HCPU		LCPU		ACPU	
			Starting Address	Ending Address	Starting Address	Ending Address	Starting Address	Ending Address
	Reserved	4KB	0x5004_3000	0x5004_3FFF	0x5004_3000	0x5004_3FFF	0x5004_3000	0x5004_3FFF
	Reserved	24KB	0x5004_4000	0x5004_9FFF	0x5004_4000	0x5004_9FFF	0x5004_4000	0x5004_9FFF
	PMUC	4KB	0x5004_A000	0x5004_AFFF	0x5004_A000	0x5004_AFFF	0x5004_A000	0x5004_AFFF
	RTC	4KB	0x5004_B000	0x5004_BFFF	0x5004_B000	0x5004_BFFF	0x5004_B000	0x5004_BFFF
	IWDT	4KB	0x5004_C000	0x5004_CFFF	0x5004_C000	0x5004_CFFF	0x5004_C000	0x5004_CFFF
	Reserved	12KB	0x5004_D000	0x5004_FFFF	0x5004_D000	0x5004_FFFF	0x5004_D000	0x5004_FFFF
	Reserved	64KB	0x5005_0000	0x5005_FFFF	0x5005_0000	0x5005_FFFF	0x5005_0000	0x5005_FFFF
	Reserved	64KB	0x5006_0000	0x5006_FFFF	0x5006_0000	0x5006_FFFF	0x5006_0000	0x5006_FFFF
	EUROPA	4KB	0x5007_0000	0x5007_0FFF	0x5007_0000	0x5007_0FFF	0x5007_0000	0x5007_0FFF
	Reserved	60KB	0x5007_1000	0x5007_FFFF	0x5007_1000	0x5007_FFFF	0x5007_1000	0x5007_FFFF
LPSYS_AHB		**256KB**	**0x5008_0000**	**0x500B_FFFF**	**0x5008_0000**	**0x500B_FFFF**	**0x5008_0000**	**0x500B_FFFF**
	GPIO2	4KB	0x5008_0000	0x5008_0FFF	0x5008_0000	0x5008_0FFF	0x5008_0000	0x5008_0FFF
	MPI5	4KB	0x5008_1000	0x5008_1FFF	0x5008_1000	0x5008_1FFF	0x5008_1000	0x5008_1FFF
	RFC	8KB	0x5008_2000	0x5008_3FFF	0x5008_2000	0x5008_3FFF	0x5008_2000	0x5008_3FFF
	PHY	4KB	0x5008_4000	0x5008_4FFF	0x5008_4000	0x5008_4FFF	0x5008_4000	0x5008_4FFF
	CRC2	4KB	0x5008_5000	0x5008_5FFF	0x5008_5000	0x5008_5FFF	0x5008_5000	0x5008_5FFF
	Reserved	40KB	0x5008_6000	0x5008_FFFF	0x5008_6000	0x5008_FFFF	0x5008_6000	0x5008_FFFF
	MAC	64KB	0x5009_0000	0x5009_FFFF	0x5009_0000	0x5009_FFFF	0x5009_0000	0x5009_FFFF
	Reserved	128KB	0x500A_0000	0x500B_FFFF	0x500A_0000	0x500B_FFFF	0x500A_0000	0x500B_FFFF
PHY_DUMP		**64KB**	**0x500C_0000**	**0x500C_FFFF**	**0x500C_0000**	**0x500C_FFFF**	**0x500C_0000**	**0x500C_FFFF**

1.4.5 Interrupt List

Table 1-5: Interrupt List of LCPU

IRQ #	IRQ Source
NMI	WDT2
IRQ[0]	AON
IRQ[1]	BLE
IRQ[2]	DMAC3_CH1
IRQ[3]	DMAC3_CH2
IRQ[4]	DMAC3_CH3
IRQ[5]	DMAC3_CH4
IRQ[6]	DMAC3_CH5
IRQ[7]	DMAC3_CH6
IRQ[8]	DMAC3_CH7
IRQ[9]	DMAC3_CH8
IRQ[10]	PATCH
IRQ[11]	DM
IRQ[12]	USART4
IRQ[13]	USART5
IRQ[14]	USART6
IRQ[15]	BT
IRQ[16]	SPI3
IRQ[17]	SPI4
IRQ[18]	I2S3
IRQ[19]	I2C5
IRQ[20]	I2C6
IRQ[21]	I2C7
IRQ[22]	GPTIM3
IRQ[23]	GPTIM4
IRQ[24]	GPTIM5
IRQ[25]	BTIM3
IRQ[26]	BTIM4
IRQ[27]	AUD_LP
IRQ[28]	GPADC
IRQ[29]	SDADC
IRQ[30]	HPSYS0
IRQ[31]	HPSYS1
IRQ[32]	TSEN
IRQ[33]	PTC2
IRQ[34]	LCDC2
IRQ[35]	GPIO2
IRQ[36]	MPI5
IRQ[37]	NNACC2
IRQ[38]	FFT2
IRQ[39]	FACC2
IRQ[40]	ACPU2LCPU
IRQ[41]	LPCOMP
IRQ[42]	LPTIM2
IRQ[43]	LPTIM3
IRQ[44]	HPSYS2
IRQ[45]	HPSYS3
IRQ[46]	HCPU2LCPU
IRQ[47]	RTC

1.5 Power Management

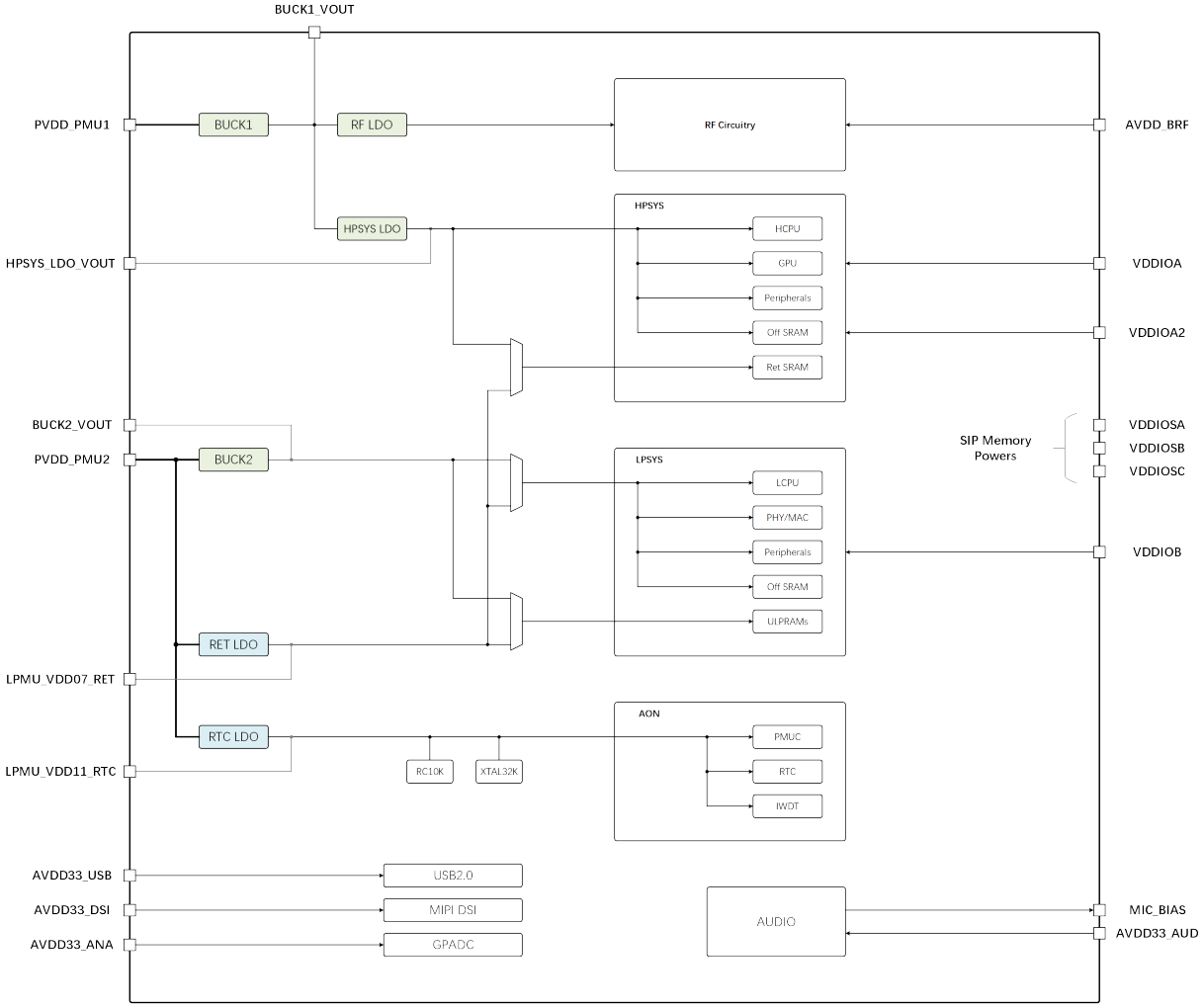


Figure 1-6: Power Management Architecture

2 High-Performance Dedicated Computing

2.1 ePicasso™ High-Performance 2.5D GPU

In 2.5D image processing, many common image operations will consume a lot of CPU computing resources. ePicasso™ is an acceleration GPU designed specifically for 2.5D image operations. It can provide exponential speed improvements for common 2.5D image operations such as layer overlay, scaling, and rotation. In addition, ePicasso™ is compatible with various common RGB image formats, simplifying the conversion of different image formats in the system.

2.1.1 Layer Overlay

ePicasso™ supports four foreground layers, one dedicated mask layer, and one monochrome background layer. The input and output formats include commonly used RGB565, RGB888, ARGB8565, ARGB8888, L8, A8 and A4. Each foreground layer has a separate overlay mode and overlay area, and the mask layer is mainly used to extract specific shapes of the image. In addition, each layer also has a separate filter configuration option, which can make the layer filter out a specific color. This function can be used for simple image capture.

2.1.2 Graphics Scaling

ePicasso™ has a layer called functional layer, which, in addition to supporting overlays, enables the scaling of graphics up to 1024 times, with an accuracy of 1/65536. The scaling can be configured separately in the X and Y directions to suit different requirements.

2.1.3 Graphics Rotation

In addition to scaling, the functional layer of ePicasso™ can support high-precision rotation of images. Users can customize the sin/cos values of the rotation angle to meet the rotation requirements of any angle. Rotation and scaling can be enabled at the same time to complete two operations of the image at one time, which improves the performance of image processing.

2.2 Vivante GCNanoUltraV High-Performance Vector Graphics GPU

GCNanoUltraV is a vector graphics GPU for the MCU platform. Compared with the GPU on the traditional platform, GCNanoUltraV has the features of low power consumption, small area and low memory requirements. Its supporting graphics library has also been optimized to better match the MCU platform.

2.2.1 Coordinate System Transformation

GCNanoUltraV supports coordinate system transformation based on 3×3 matrix. Relying on coordinate transformation, it can generate the corresponding deformation of graphics.

2.2.2 Layer Stacking

GCNanoUltraV supports up to 14 different pixel formats and 8 layer stacking methods based on the Porter-Duff rule.

2.2.3 Filling

GCNanoUltraV supports non-zero filling and odd/even filling.

2.2.4 Drawing

GCNanoUltraV can draw straight lines and curved paths with monochrome and gradient filling in color.

2.2.5 Layer Compression

GCNanoUltraV support compression format of etc2 and it can directly read the image of etc2 format when reading the layer. As a lossy compression, etc2 has a compression ratio of 1:4. Using compressed materials can save space of resource storage.

2.3 JPEG Codec Accelerator

In the MCU platform, the storage of images has been consuming a lot of memory space. Common compression such as JPEG can greatly save image storage space, but it also consumes a lot of computing resources. The hardware JPEG codec accelerator can rely on the powerful JPEG codec ability to efficiently implement the operation of JPEG images, which not only saves storage spcae, but also greatly shortens the operation time.

2.3.1 JPEG Encoder

The encoder supports JPEG Baseline mode, input formats of YUV420, YUV422, RGB444, RGB555, RGB565, and RGB888, output formats of JFIF format 1.02 and Non-Progressive JPEG. The resolution is up to 4K $\times$ 4K.

2.3.2 JPEG Decoder

The decoder supports JPEG Baseline mode, input formats of JFIF format 1.02, YUV420, YUV422 and YUV444. The output format supports YUV to RGB conversion, which is compatible with BT.601 and BT.709 standards, and the conversion standard can also be customized. The output post-processing supports image scaling and cropping, and the maximum resolution is 4K$\times$4K.

2.4 LCD Controller

The LCD controller is mainly used to output data from the Framebuffer to the external display, and the existing LCD controller can support common screen interfaces, including DBI and DPI. In addition, the LCD controller also supports images of compressed format, which can significantly reduce the memory usage bandwidth and improve system performance.

2.4.1 TurboPixel™ Frame Buffer Compression

To improve the frame rate of the image and the smoothness of the display, multiple (two or three) frame buffers are frequently used. Typically, in order to parallelize image output and image processing, dedicated frame buffers are required to output image data to the screen. To reduce the memory space and reading bandwidth of these frame buffers, the MCU system provides a TurboPixel™ image frame compression module based on proprietary algorithm. When reading the image data, the decompression module in the LCD controller can directly read the compressed data and output the decompressed data to the screen. In this way, the memory space of the frame buffer and the bandwidth resources consumed by reading can be saved.

2.4.2 Display Interface

The LCD controller is mainly used for the adaptation between the data for display and the mainstream display interfaces, and the following display interfaces are supported by this chip.

2.4.2.1 MIPI-DBI

The LCD controller can support serial SPI mode and parallel 8080 mode in the DBI interface. For SPI mode, the LCD controller can support both 3-wire and 4-wire modes, as well as dual/quad data line operations. It supports 8-bit RGB332, 16-bit RGB565 and 24-bit RGB888 in color format. For the 8080 mode, the LCD controller supports bus widths of 8-bit, 16-bit and 24-bit, and also supports color formats of RGB332, RGB444, RGB565, RGB666 and RGB888.

2.4.2.2 MIPI-DPI

To support screens without built-in cache, the LCD controller has also added support for the DPI interface, which has a 24-bit data width and supports color formats of RGB565 and RGB888. In addition, the LCD controller provides flexible VBP, VFP, HBP and HFP controls to meet the needs of different screen types.

2.4.2.3 MIPI-DSI

As a serial high-speed bus, DSI is mainly designed for high-resolution and highly integrated screen usage scenarios, such as wearable devices. The LCD controller also adds support for the DSI interface. In high-speed mode, it can support up to 2 bi-directional data lines, each with a maximum transfer rate of 480Mbps. In low-speed mode, the LCD controller can also support one bi-directional data line. This configuration can meet the needs of most wearable devices.

2.4.2.4 JDI Reflective Display

To meet the low-power requirements of wearable products, JDI has developed an ultra-low-power reflective display that uses the sun's rays to present images. Compared with the traditional LCD screen, the power consumption can be reduced by more than 95%. It can be used in wearable products to achieve long battery life. The LCD controller also added support for JDI reflective display interface, including serial interface and parallel interface. The two interfaces can support up to 64-color display, and support partial refresh and full-screen refresh, thereby further reducing the power consumption of screen refresh and meeting the needs of long battery life.

2.5 eZip™ Lossless Compression Decoder

The eZip™ decoder is a real-time lossless decompression module based on proprietary algorithm, with a compression rate equivalent to that of the Zip format. It can be used to decode the general data before saving it, which will improve the real-time loading capability of the data. If the data is transferred from outside the chip, the transfer after compression will help shorten the transfer time and reduce the power consumption.

In addition, eZip™ also supports image compression of proprietary formats, with a compression rate equivalent to that of the PNG format, and supports independent DMA operations or reading linked with ePicasso™. When operating independently, eZip™ can flexibly decompress and transport the compressed pictures stored in Flash or RAM to the target cache through the DMA mechanism. In the linkage mode, ePicasso™ reads pictures from the memory in real time and decompresses them in real time through the eZip™ module, and then performs the required 2.5D calculations according to the general graphics process, thereby saving the cache for temporary storage of decompressed pictures.

Through the above mechanism, eZip™ can effectively reduce the demand for storage capacity of image materials, maximize the richness of materials in limited storage, and reduce the bandwidth requirements for off-chip storage, thereby greatly improving the overall operating efficiency of the system.

The eZip™ module is a module for decoding the eZip™ compressed images and outputting them. The module reads compressed data through the AHB bus, and the decoded image data can be configured to be output through the AHB bus or directly sent to the epic module for subsequent processing.

The module has the following characteristics:

- The data address input/output via the AHB bus can be configured
- Output image data can be sent directly to the epic module
- Can output image data for a specified area
- Support decoding parameter cache function, which can shorten decoding time in case of cache hit

2.6 Neural Network Accelerator

2.6.1 Neural Network Matrix Convolution Accelerator (NNACC)

The matrix convolution accelerator is designed to meet the needs for the underlying matrix computing power in machine learning, and can be widely applied to various neural network frameworks. The accelerator has rich memory and access interfaces and provides flexible data address configuration. It supports a maximum input matrix of 255×255 and a maximum number of input and output channels of 128. It supports 8bit integer operations, which can meet most of the edge-end AI computing requirements, such as voice command recognition, heart rate, pedometer, electrocardiogram and other sensor calculations.

2.6.2 Neural Network Co-Processor (NN Co-Processor)

The neural network coprocessor is connected to the hpcpu/lpcpu through the coprocessor interface. The software calls the processor through special coprocessor instructions.

The coprocessor has the following characteristics:

- Data bus width of 64Bit

- Support MAC operations with 8Bit width
- Support 4 independent MAC operations for a single instruction

2.7 Digital Signal Processing Accelerators

2.7.1 FFT Accelerator

FFT operation requires high computing power. Using FFT accelerator can reduce CPU load and improve system performance. There is one FFT accelerator integrated in each of AUXSYS and HPSYS to meet the FFT computing power requirements in more scenarios.

Features of FFT accelerator:

- Support maximum 4096-point minimum 16-point FFT (AUXSYS FFT)
- Support maximum 1024-point minimum 16-point FFT (LPSYS FFT)
- Support 24-point, 16-point and 8-point fixed-point signed number inputs and outputs, and the bit widths are independently configurable
- Support real number FFT operation
- Support IFFT

2.7.2 Cordic Coprocessor

The Cordic coprocessor is used to compute trigonometric and hyperbolic functions and some arithmetic operations derived from them. There is one Cordic coprocessor integrated in each of HPSYS, AUXSYS and LPSYS.

Features of Cordic coprocessor:

- Support ARM coprocessor instructions
- Support ARM Custom Datapath Extention instructions (only HPSYS)
- Support trigonometric function operations: cos, sin, ang, mod, atan, rot
- Support hyperbolic function operations: cosh, sinh, atanh, angh, modh, mul, div, ln, exp, sqrt
- Support 32-bit fixed-point inputs and outputs

3 Peripherals

3.1 Dual-mode Bluetooth 5.3

3.1.1 RF and Baseband

BLE RF and baseband include the transmitter and the receiver. The transmitter modulates the baseband signal to the 2.4G BLE frequency band and transmits it, and the receiver receives the over-the-air 2.4G BLE frequency band signal and demodulates it to the baseband signal.

The main features are:

- Support Bluetooth 5.2 protocol: 1M PHY (1Mbps), 2M PHY (2Mbps), Coded PHY (125Kbps, 500Kbps)
- Integrated AGC
- Support RSSI
- The receiver supports automatic frequency offset correction
- Adjustable transmit power, 10dBm max
- Integrated Balun and antenna matching network, no off-chip matching required

3.1.2 BT MAC

The BT MAC is a dual-mode baseband controller that fully supports Bluetooth protocol v5.3 and is compatible with v4.2, v4.1, and 4.0. It is mainly used for packet encoding and decoding as well as event scheduling.

The main functions are as follows:

- BLE mode:
  1. Support rate (1M/2M);
  2. Support all packet formats (broadcast packet/expanded broadcast packet/data packet, etc.);
  3. Support data encryption and decryption;
  4. Support data stream processing (redundancy checking, whitening);
  5. Support two frequency hopping modes;
- Classic Bluetooth mode:
  1. Support all packet types of ACL, CSB, SCO and eSCO;
  2. Support data encryption and decryption (E0 encryption and AES-CCM encryption);
  3. Support data stream processing (HEC, CRC, Whitening, FEC2/3, FEC1/3);
  4. Support coding and decoding of audio data (CVSD and a/μ-Law);
  5. Support adaptive frequency hopping;
- And
  - Support AMBA AHB bus access;
  - Support WLAN/MWS coexistence mechanism.

3.2 Analog Peripherals

3.2.1 12Bit Analog/Digital Converter

GPADC contains a SARADC, and the basic function is to convert the external input voltages into digital signals.

The main features of GPADC are:

- 12-bit resolution
- Maximum sampling rate 4MS/s
- Single-ended input voltage: 0 ~ 3.3V
- Differential input voltage: -2.1V ~ +2.1V
- Support 8 single-ended analog inputs or 4 pairs of differential analog inputs
- Support single measurement mode and cyclic measurement mode
- Each measurement can be divided into 4 time slots, and each time slot can be individually configured with analog input channels
- Support software (write register) and hardware (e.g. timer) triggering
- Support DMA channels
- Sampling frequency can be configured

Table 3-1: 12-bit GPADC Specifications

	Min.	Typ.	Max.	Unit	Comments
Resolution		12		bit	
T_{sample} (Differential)	125n		2/3	s	fs=1/(T_{sample}+$T_{conversion}$)
T_{sample} (Single-Ended)	166.66n		2/3	s	
$T_{conversion}$	125n		10.67u	s	
Sample rate (fs)			4	Msps	
ENOB (Differential)		10.6		bit	V_{in}=-1dBFs, no averaging
ENOB (Single-Ended)		10		bit	V_{in}=-3dBFs, no averaging
SNDR (Differential)		65.6		dB	V_{in}=-1dBFs, no averaging
SNDR (Single-Ended)		61.96		dB	V_{in}=-3dBFs, no averaging
Current Consumption		466		uA	fs=4Msps
		130		uA	fs=500ksps
		90		uA	fs=100ksps

The relationship between GPADC source resistance R_{AIN} and the sampling time is as follows:

Resolution (bit)	Number of T_{PCLK} Cycle @24MHz	T_{sample} (ns)	Maximum source resistance R_{AIN} (kOhm)
12	4	166	1
	15	625	5
	30	1250	10
	150	6250	50
	300	12500	100
	1500	62500	500
	15000	625000	5000

3.2.2 16Bit Analog/Digital Converter

The SDADC is mainly used for the measurement of signals, and supports continuous sampling as well as single sampling. The reference voltage is 0~2V, and the gain is 0.25 to 4 times. The measurement range that can be achieved by single-ended is 0V~(0.65×reference voltage/gain), the measurement range that can be achieved by differential is -(0.65×reference voltage/gain)~(0.65×reference voltage/gain), but the measurement range can't exceed 0~AVDD, with a minimum measurement error of ±60uV, and a sampling rate of 4kHz for single sampling and 8kHz for continuous sampling.

Main functions:

- Support 16bit data accuracy
- Support up to 2 differential or 5 single-ended channel sampling
- Support multiple sampling of multiple channels which can be configured by the software

3.2.3 Temperature Sensor

The temperature sensor converts the temperature into a voltage that changes with the temperature, and then converts the voltage into a number through the ADC. The system calls the temperature sensor through the software.

The main features are as follows:

- Temperature sensor resolution 0.2°C
- Support temperature range from -40°C to 125°C
- Temperature sensor accuracy -3°C to 3°C
- Support polling or interrupt mode reading

3.2.4 Low-Power Comparator

The LPCOMP (Low-Power Comparator) contains two independent voltage comparators which can compare the voltage of an external input analog signal to the reference voltage value to produce the comparison result. The two comparators can measure different signals separately or measure the same signal and produce a combined output. The reference voltage value can be input from an external source or generated internally by the chip. The comparator results can be read via IO output or via registers, and can also generate interrupt/ PTC event triggers or wake-up signals.

The LPCOMP is also capable of real-time monitoring when the system enters certain low-power modes, and waking the system up when a specific comparison result is detected.

Main features of LPCOMP:

- Two comparators, which can be used independently or in combination for window comparison
- Reference voltage selection
  - Internally generated 4 levels of reference voltage
  - External input
- Configurable hysteresis comparison
- Configurable power/speed gear
- Polarity reversal of the comparison results
- Post-processing of the comparison results
  - High/Low level
  - Rising edge/falling edge/any edge

- Multiple outputs
  - IO
  - Register
  - Interrupt
  - PTC trigger
  - LPTIM clock
  - Low-power sleep wakeup
- The system can also work under low-power mode (light sleep/deep sleep) and can be woken up

3.2.5 Audio DAC

Audio DAC is a module that converts digital audio signals into analog voltage output. The chip integrates two 24-bit DACs, supporting audio sampling rates from 8KHz to 48KHz, and supports differential output.

3.2.6 Audio PLL

The main function of audio PLL is to provide high-precision clock for the audio system. It supports the fractional frequency division function with an adjustment accuracy of 48MHz/2^18, and can meet the needs of different sampling rates such as 48KHz, 32KHz and 44.1KHz.

3.2.7 Audio ADC

Audio ADC is a module that converts external analog singals into internal digital audio signals. The chip integrates two 24-bit ADCs, supporting audio sampling rates from 8KHz to 48KHz, and each ADC has separate gain adjustments.

3.3 DMA

3.3.1 ExtDMA

The ExtDMA (Extended Direct Memory Access) enables efficient data transfer between two different address ranges on the bus, and integrates the TurboPixel™image frame compression module for image compression while transferring. ExtDMA can also be used as a general-purpose DMA when compression is not enabled. Compared to DMAC, ExtDMA is more efficient in accessing external memory (e.g. FLASH, PSRAM), but it has only one channel, supports only 4-byte aligned handling, and does not respond to peripheral requests.

Main features of ExtDMA:

- Single transmission channel, built-in FIFO with a depth of 16 and a bit width of 32 bits
- Both the source address and the destination address are accessed in 4 bytes, and support automatic address increment
- The maximum number of transmission units in a single configuration is 2^20-1, with a fixed 4-byte transmission per unit, i.e., a maximum of 4M bytes in a single transmission
- Each channel supports transmission completion, half transmission, and transmission error event flags, and can generate interrupt requests independently
- Integrated TurboPixel™image frame compression function, support RGB565/ RGB888/ ARGB8888 format input, supports up to 1024×1024 resolution

3.3.2 DMAC

The DMAC (Direct Memory Access Controller) is used to carry out data transfer between two different address ranges on the bus. DMAC has a total of 8 independent channels. Each channel can be configured with a source address range and a target address range, which are respectively mapped to the address range of each memory or peripheral, so as to achieve high-efficiency transmission between memory-memory, memory-peripheral, peripheral-memory, and peripheral-peripheral, which can effectively alleviate the workload of the CPU.

The DMAC supports peripheral response mode and memory handling mode: In the peripheral response mode, the DMAC performs handling based on the DMA request of the peripheral, thereby adapting the bandwidth of the peripheral; In the memory handling mode, the DMAC does not wait for the DMA request of the peripheral, and will complete data transfer as soon as possible. When multiple channels are enabled at the same time, the DMAC will transport in order of priority from high to low; and in the process of transporting lower priority channels, the higher priority channels can carry out the preemption handling. Each channel can generate an interrupt or PTC trigger when the transmission is halfway or complete.

DMAC1 and DMAC2 is located in HPSYS and can respond to DMA requests from HPSYS peripherals. DMAC3 is located in LPSYS and can respond to DMA requests from LPSYS peripherals.

Main features of DMAC:

- 8 independent configurable channels
- The DMA request for each channel can be selected from up to 64 peripheral DMA requests, or can be requested by software
- Each channel supports 4 levels of priority configuration, when the priority is the same, it is judged according to the channel number
- Support memory-memory, memory-peripheral, peripheral-memory, peripheral-peripheral transfer
- Support single-byte/ double-byte/ 4-byte access to both source and destination addresses independently, and support automatic address increment
- Support cyclic buffering mode, which will automatically restart after a single transfer is completed
- Each channel supports 3 types of event flags,i.e. transmission completed, half-transmission, transmission error, and can independently generate interrupts or PTC triggers
- The maximum number of transmission units in a single configuration is 65536, and each unit has single-byte/ double-byte/ 4-byte transmission according to different configurations
- Each channel supports block transfer mode with configurable block size

3.4 AUDPRC

The audio processing module performs sampling rate conversion, mixing and equalization for audio data from different sources, and sends the processed audio data to the corresponding playback or storage device. It mainly includes two main data paths, the DAC path for processing playback data and the ADC path for processing audio acquisition data.

3.4.1 DAC Path

DAC path audio data comes from memory, and AUDPRC supports up to four channels of 24bit audio data. The DAC path in AUDPRC supports sampling rate conversion for two channels of data. The sampling rate conversion range is 1/8~8 times, and the singal-to-noise ratio is not less than 96dB. After the converted data is mixed with data of the other two channels,

it enters the 10-level audio equalizer, the parameters of which can be configured by users according to needs. Finally, the two-channel audio data passing through the equalizer can be sent to the analog DAC module or the I2S interface as output.

3.4.2 ADC Path

ADC path audio data comes from analog ADC or the I2S interface, and supports up to two channels of 24bit audio data. The data through the sampling rate conversion module can be stored in memory by DMA.

3.5 I/O Peripherals

3.5.1 General Purpose Input/ Output (GPIO)

The system supports up to 154 GPIOs (HPSYS: 94, LPSYS: 60). Different functions can be assigned to these pins by configuring the corresponding registers.

When configured as an output function, the output value can be configured through the register.

When configured as an input function, the input value can be queried through the corresponding register, and support the input signal interrupt trigger at the same time. The interrupt trigger mode can be set to level trigger and edge trigger, which includes upper and lower dual-edge trigger.

3.5.2 Universal Asynchronous Receiver/Transmitter (UART)

The Universal Asynchronous Receiver/Transmitter (UART) supports full-duplex mode and offers baud rates up to 6Mbps and a variety of configurable data formats, providing a flexible and efficient means of data interaction for communication with external standardized devices. It also supports DMA for multi-packet transceiving.

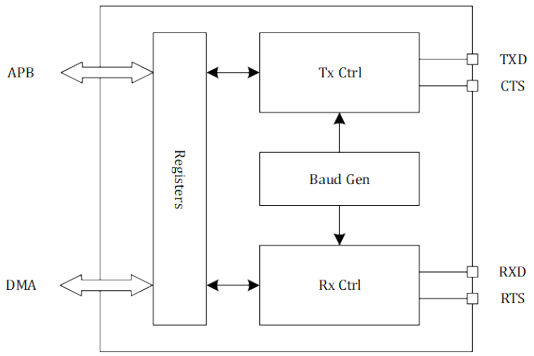


Figure 3-1: UART

Main features of UART:

- Full-duplex asynchronous communication
- Configurable 16 times oversampling or 8 times oversampling, select frequency priority or clock tolerance priority
- Flexible baud rate configuration, when the input clock is 48MHz and the oversampling rate is 16, the baud rate is 3Mbps
- Configurable packet length (7/8/9 bits)

- Configurable stop bit (1/2 bits)
- Hardware flow control (CTS/RTS)
- DMA multi-packet sending and receiving
- Receiving parity check and sending parity generation
- Receiving and sending interrupts, and other error interrupts

Baud rate calculation instructions

Assuming that the input clock is fixed at 48MHz, the baud rate calculation formula is as follows:

$$Baud\ Rate = \frac{48MHz}{(BRR_{INT} + \frac{BRR_{FRAC}}{16})(16\ or\ 8)} \tag{3.1}$$

3.5.3 I2C

The I2C (Inter-Integrated Circuit) interface supports both the roles of master and slave. It can be used as a master to communicate with I2C slave peripherals, or as a slave to respond to an external I2C master. I2C has a built-in 8-byte FIFO, which can perform single read and write, or batch data read and write through DMA. I2C supports standard mode, fast mode, fast mode plus, and high-speed mode, with a maximum speed of 3.4Mbps.

I2C1, I2C2, I2C3 and I2C4 are located in HPSYS. I2C5, I2C65 and I2C7 are located in LPSYS.

Main features of I2C:

- Can be used as master and slave at the same time
- Support bus multi-master
- Support standard mode (up to 100kbps)
- Support fast mode (up to 400kbps)
- Support fast mode + (up to 1Mbps)
- Support high-speed mode (up to 3.4Mbps)
- As a master, it supports access to 7-bit or 10-bit addressing
- As a slave, it supports access to 7-bit addressing
- Configurable bus timing
- Support clock stretching
- 8-byte FIFO, support DMA
- Configurable digital anti-jitter circuit
- Independent functional clock, support system clock dynamic adjustment

3.5.4 PDM

The PDM (Pulse Density Modulation) interface is mainly used to convert the PDM audio signal captured by the PDM microphone into PCM (Pulse Code Modulation) signal for subsequent audio processing.

Main features of PDM:

- Support left and right stereo signals at the same time, and can also collect mono signals separately
- Available PDM microphone clock rates: 3.072MHz, 1.536MHz, 0.768MHz, 1.024MHz, 2.4MHz, 1.6MHz, 0.8MHz
- Support PCM data rates: 48kHz, 32kHz, 24kHz, 16kHz, 12kHz, 8kHz
- Support 32bit, 24bit, 16bit and 8bit PCM signals

- Support resolution of 0.5dB and gain adjustable from -15dB to 45dB

3.5.5 I2S

The I2S interface is used for audio input and output, and can be used to connect external audio chips, digital microphones and other devices. Compared with the analog audio interface, the I2S digital audio interface has a better anti-interference ability and a more streamlined interface protocol.

Main features of I2S:

- Support both master and slave modes
- Support full duplex mode
- Configurable I2S data format, including left-justified, right-justified and standard format
- Support multiple audio data formats, including 8-bit and 16-bit mono and stereo formats
- Configurable I2S PCM signal bit width, up to 24-bit

3.5.6 Serial Peripheral Interface (SPI)

The SPI supports 3 communication formats: SSP/ SPI/ Microwire. SSP/ SPI is a full-duplex communication protocol, and the controller can be configured in Master or Slave mode. Microwire is a half-duplex communication protocol, and the controller can only be configured in Master mode. The SPI controller has a built-in transmit/receive FIFO. The transmit FIFO and the receive FIFO share the same address. The receive FIFO is accessed when the address is read, and the transmit FIFO is accessed when the address is written. SPI1/ SPI2 are located in HPSYS, and SPI3/ SPI4 are located in LPSYS.

The features of SPI are as follows:

- Support 4 to 32Bit data width
- In SPI format, the clock polarity and phase can be set by register SPO and SPH
- Chip select signal polarity can be configured
- FIFO depth can be set to 32Bits×16Entry or 4Bits/ 8Bits×32Entry
- Both receive and transmit support DMA mode
- The maximum clock frequency of SPI in HPSYS is 48MHz; the maximum clock frequency of SPI in LPSYS is 24MHz

The working sequences of various communication formats are as follows:

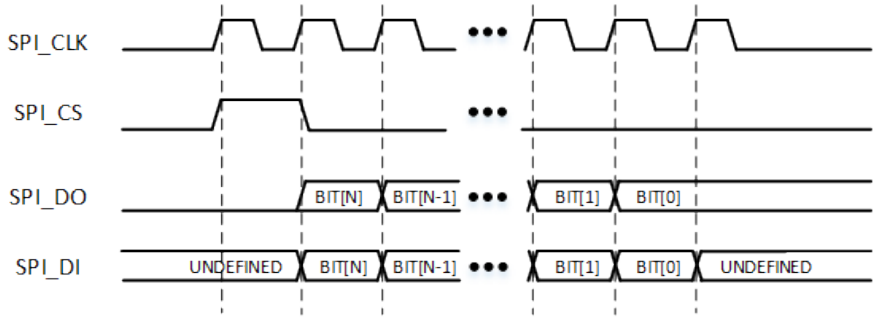


Figure 3-2: Single Transmit and Receive Sequence of SSP Format

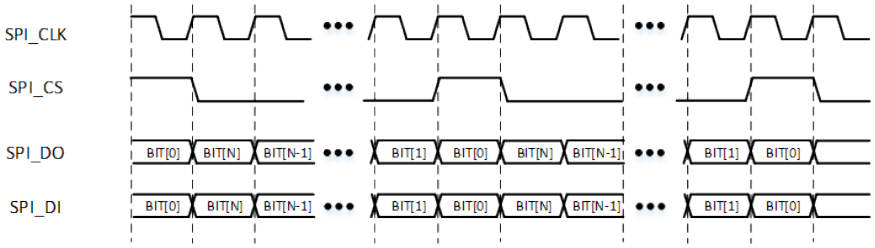


Figure 3-3: Continuous Transmit and Receive Sequence of SSP Format

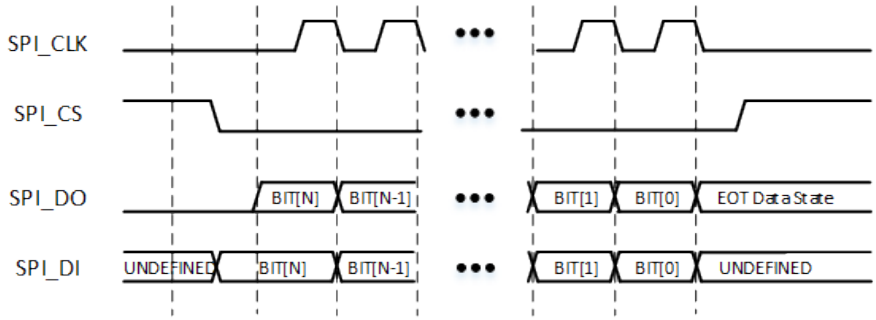


Figure 3-4: Single Transmit and Receive Sequence of SPI Format

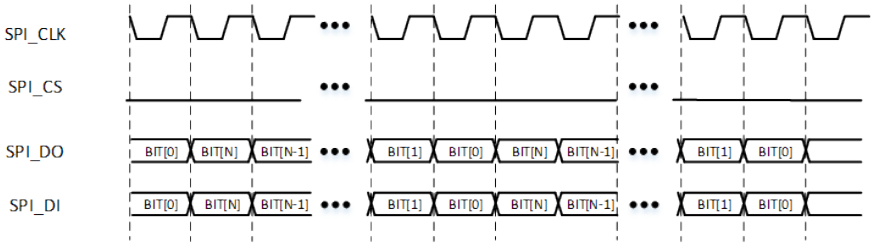


Figure 3-5: Continuous Transmit and Receive Sequence of SPI Format

The following figures illustrate the effect of SPH/SPO settings in SPI format:

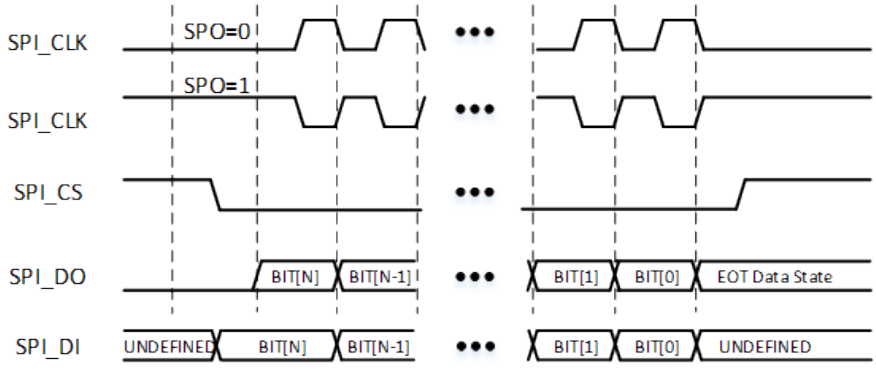


Figure 3-6: SPI Sequence at SPH=0

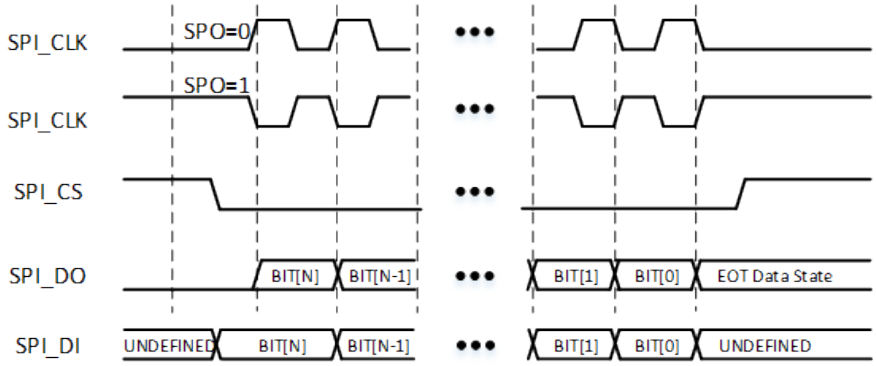


Figure 3-7: SPI Sequence at SPH=1

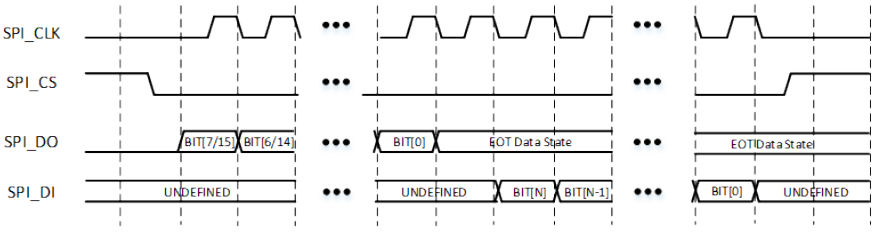


Figure 3-8: Single Transmit and Receive Sequence of Microwire Format

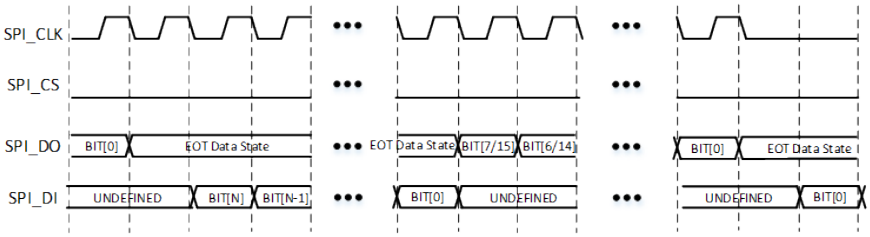


Figure 3-9: Multiple Transmit and Receive Sequence of Microwire Format

3.5.7 Peripheral Task Controller (PTC)

The PTC (Peripheral Task Controller) is a stand-alone peripheral controller, which can automatically complete the mutual scheduling and control tasks of each peripheral without waking up the CPU. Based on the event triggering of the selected peripherals, the PTC can automatically rewrite the working mode or working state of each peripheral, and can chain these tasks together to form an automatically triggered task sequence, thus completing a complex and fast response task chain. In the process of the task chain, the CPU can stay asleep all the time, thereby effectively saving power.

The PTC has a total of 8 channels, independent trigger source can be selected for each channel and independent task can be can be configured. The tasks that can be performed include two types: write the specified data directly to the specified address; read out the contents of the specified address, perform XOR/ and/ or/ addition with the specified data and then write it back. When the task of each channel is completed, a trigger signal can be generated to trigger the tasks of other channels. The number of triggers can be configured for each channel. Some channel support a configurable delay before executing the task after triggering.

PTC1 is located in HPSYS, and PTC2 is located in LPSYS. Both of them can control the peripherals on HPSYS bus and LPSYS bus.

Main features of PTC:

- 8 independently configured channels can work at the same time
- Each channel trigger can be selected from 128 trigger sources, including PTC's own trigger sources
- Access to AHB and APB peripheral address space, word-aligned access only
- Support directly writing data, or rewriting after reading
- Support 32-bit XOR/ and/ or/ addition operations
- Configurable trigger times 1 ~ 1023, or unlimited trigger times
- Configurable trigger delay 0 ~ 65535 HCLK cycles
- Fixed priority arbitration, the smaller the channel number, the higher the priority
- The register space of 4 words is used for data cache

3.5.8 USB2.0 FS

This chip integrates a high-speed (HS) USB 2.0 Host/Device interface with the following functions.

- Software configurable endpoint settings, support suspend/ resume
- Support session request protocol and host negotiation protocol
- Support high speed and full speed modes

3.5.9 SIM Card Controller

The SIM card interface is a half-duplex serial interface. The SIM card controller in this chip supports the sending and receiving of SIM card data packet. The controller can support polling mode and DMA mode. Combined with the upper software, the protocol layer communication function of SIM card can be realized.

3.6 Timers

3.6.1 General-Purpose Timer

The GPTIM (General-Purpose Timer) is based on a 16-bit counter, and can realize functions such as timing, measuring the pulse length of the input signal (input capture) or generating output waveforms (output comparison and PWM). The counter itself can count up, down or up/down. The counting clock can be the system PCLK, IO input signal or cascaded input signal, and can be prescaled from 1 to 65536 times. The GPTIM has 4 channels in total, which can be independently configured as input capture or output mode. The results of counting, input capture and output comparison can generate interrupts, DMA requests or PTC events. The GPTIM has a Master-Slave Mode interface, which can be multi-level cascaded to realize functions such as multi-level counting or synchronous triggering.

GPTIM1 and GPTIM2 are located in HPSYS. GPTIM3, GPTIM4 and GPTIM5 are located in LPSYS.

Main features of GPTIM:

- 16-bit increment, decrement, increment/ decrement auto-reload counter, the maximum count is 65535
- 16-bit programmable (can be modified in real time) prescaler, the clock division is any value between 1~65536
- 8-bit configurable repeat count
- Support One Pulse Mode (OPM), the counter will stop automatically when the repeated counting is completed
- 4 independent channels, which can be configured as input or output modes respectively

- Input mode
  - Rising edge/ falling edge capture
  - PWM pulse width and period capture (requires two channels)
  - Optional one of 4 input ports or 1 external trigger port, supporting anti-jitter filtering and pre-frequency reduction
- Output mode
  - Forced output high/ low level
  - Output high/ low/ toggle level when counting to the comparison value
  - PWM output, pulse width and period can be configured
  - Multi-channel PWM combined output to generate multiple PWMs with interrelationships
  - Single pulse/ retrigger single pulse mode output
- Master-Slave Mode
  - Support multi-counter interconnection, which can be used as a slave device to be controlled by external input or other master devices while generating control signals as a master device
  - Control modes include reset, trigger, gate control, etc.
  - Support synchronous start and reset of multiple counters
- Encoding mode input, control the incremental/ decremental counting of the counter
- An interrupt/ DMA request/ PTC trigger is generated when the following events occur:
  - Update: Counter increment overflow /decrement overflow, counter initialization (by software or internal/external trigger)
  - Trigger event (counter start, stop, initialization or counting triggered internally/ externally)
  - Input capture
  - Output comparison

3.6.2 Advanced Timer

The ATIM (Advanced Timer) is based on a 32-bit counter, and can realize functions such as timing, measuring the pulse length of the input signal (input capture) or generating output waveforms (output comparison and PWM). ATIM supports 6 complementary PWM outputs with dead zone protection, multiple PWMs with simultaneous phase change, and 2 brake inputs to quickly switch the outputs to a safe state. The counter itself can count up, down or up/down. The counting clock can be the system PCLK, IO input signal or cascaded input signal, and can be prescaled from 1 to 65536 times. The ATIM has 6 channels in total, which can be independently configured as input capture or output mode. The results of counting, input capture and output comparison can generate interrupts, DMA requests or PTC events. The ATIM has a Master-Slave Mode interface, which can be multi-level cascaded to realize functions such as multi-level counting or synchronous triggering.

Both ATIM1 and ATIM2 are located in HPSYS.

Main features of ATIM:

- 32-bit increment, decrement, increment/ decrement auto-reload counter
- 16-bit programmable (can be modified in real time) prescaler, the clock division is any value between 1~65536
- 16-bit configurable repeat count
- Support One Pulse Mode (OPM), the counter will stop automatically when the repeated counting is completed
- 6 independent channels
  - Channel 1~3 can be configured as input or output modes respectively, each channel can output 2 complementary PWMs with dead zone protection

  - Channel 4 can be configured to input or output mode, it can output single PWM
  - Channel 5 and 6 can be configured to output comparison mode
- Input mode
  - Rising edge/ falling edge capture
  - PWM pulse width and period capture (requires two channels)
  - Optional one of 4 input ports or 1 external trigger port, supporting anti-jitter filtering and pre-frequency reduction
- Output mode
  - Forced output high/ low level
  - Output high/ low/ toggle level when counting to the comparison value
  - PWM output, pulse width and period can be configured
  - Multi-channel PWM combined output to generate multiple PWMs with interrelationships
  - Single pulse/ retrigger single pulse mode output
- Master-Slave Mode
  - Support multi-counter interconnection, which can be used as a slave device to be controlled by external input or other master devices while generating control signals as a master device
  - Control modes include reset, trigger, gate control, etc.
  - Support synchronous start and reset of multiple counters
- Encoding mode input, control the incremental/ decremental counting of the counter
- Support Hall sensor circuit for positioning
- 2 brake inputs with anti-jilter filter to quickly place the outputs in a safe state. The brake singal sources include
  - CPU anomaly
  - Comparator
  - External input
  - Software trigger
- An interrupt/ DMA request/ PTC trigger is generated when the following events occur:
  - Update: Counter increment overflow /decrement overflow, counter initialization (by software or internal/external trigger)
  - Trigger event (counter start, stop, initialization or counting triggered internally/ externally)
  - Input capture
  - Output comparison
  - Brake
  - Phase change

3.6.3 Basic Timer

The BTIM (Basic Timer) is based on a 32-bit incremental counter and can realize the timing function. The counter clock can be the system PCLK or cascaded input signal, and can be prescaled from 1 to 65536 times. The timing results can generate interrupts, DMA requests, or PTC events. The BTIM has a Master-Slave Mode interface, which can be multi-level cascaded to realize functions such as multi-level counting or synchronous triggering.

BTIM1 and BTIM2 are located in HPSYS. BTIM3 and BTIM4 are located in LPSYS.

Main features of BTIM:

- 32-bit incremental auto-reload counter
- 16-bit programmable prescaler, the clock division is any value between 1~65536

- Support One Pulse Mode (OPM), the counter will stop automatically when the counting is completed
- Master-Slave Mode
  - Support interconnection with BTIM and GPTIM, which can be used as a slave device to be controlled by external input or other master devices while generating control signals as a master device
  - Control modes include reset, trigger, gate control, etc.
  - Support multiple timers to start and reset simultaneously
- Interrupt/ DMA will be generated in case of counter overflow or initialization

3.6.4 Low-Power Timer

The LPTIM (Low-Power Timer) is based on a 24-bit incremental counter, and can realize functions such as timing, generating output waveform (output comparison and PWM), and waking up the system. The counter clock can be the system PCLK2, low-power clock, IO input signal or comparator output, and can be prescaled up to 128 times and cycle counting up to 256 times. Depending on the counting results, the PWM output as well as the interrupt can be generated,or the wake-up signal can be generated to wake up the system from the low-power mode. When the IO input signal is used as the count clock, it supports counting independent of the internal clock and generates the wake-up signal, allowing the system to turn off the internal clock.

LPTIM1 is located in HPSYS. LPTIM2 and LPTIM3 are located in LPSYS. only LPTIM2 and LPTIM3 support using IO input signals or comparator outputs as count clocks. Only LPTIM3 supports outputing PWM.

Main features of LPTIM:

- 24-bit upward automatic reload counter, the maximum count is 16777215 (2^24-1)
- Counting clock selection
  - Internal clock, PCLK2 or low-power clock
  - IO input signal or comparator output with selectable edges, can use the internal clock for anti-jitter, and can also count independently without relying on the internal clock
- 8-level prescaling, clock division is 0 to the 7th power of 2
- 1~256 cycles
- Counting mode
  - Continuous counting mode
  - One Pulse Mode, counting ends after the number of cycles is completed
- Configurable polarity output mode
  - PWM output, can be configured with pulse width and period
  - Single toggle output
  - Single pulse or specified number of pulse output
- Trigger mode
  - Software trigger
  - IO input signal edge trigger, support anti-jitter filtering
- Timeout detection, the counter will be reset on each external trigger
- The interrupt or wake-up signal will be generated when the following events occur:
  - Update
  - Counter overflow
  - Output comparison
  - External trigger

3.6.5 Watchdog

The watchdog timer, as a counter, is mainly used to reset the system after the set time is reached to prevent the software from hanging up.

Basic functions of watchdog timer:

- Support two working modes:
  - Mode0
    - wdt will not generate interruption, and will reset the system directly after the set time is reached
    - Support up to 24-bit counter
  - Mode1
    - Divided into two periods. After reaching the set time of the first period, the interrupt will be generated. After reaching the set time of the second period, the system will be reset
    - Support up to 24-bit counter for each period
- Support write protection to prevent software from misoperation of wdt

3.7 Encryption

3.7.1 AES

The AES accelerator is an arithmetic accelerator for symmetric encryption algorithms. Users can configure the encryption and decryption algorithm keys and initial vectors to perform encryption and decryption operations on the data in the memory, and store the results in the designated memory area.

Compared with software encryption and decryption, the AES accelerator has higher computing speed, more flexible configuration, and better access efficiency to peripheral storage devices. In addition, in bypass mode, the AES accelerator can also be used as a DMA for data transmission.

Features of AES:

- Support AES-128, AES-192, AES-256 and State Secrets SM4 algorithm standard
- Support ECB, CTR and CBC modes
- RootKey can be called to perform encryption and decryption operations, while ensuring that RootKey cannot be read by external programs

3.7.2 HASH

HASH is an operational accelerator for hash sequence algorithms. User can choose different hash algorithms to calculate the hash values of specific data in memory. HASH is faster than the software algorithm, and the configuration is also flexible. Users can also customize the initial vector to achieve multi-threaded HASH operations. The algorithms supported by HASH include SHA1, SHA224, SHA256 and SM3.

3.7.3 CRC

The CRC (Cyclic Redundancy Check) can perform CRC calculations with a specific bit width, any generated polynomial, and any initial value. Data can be input via CPU or DMA with a minimum input unit of a single byte and no maximum

byte limit. A single HCLK cycle is sufficient for a single byte input calculation. The check result will be obtained instantly after all data inputs are completed. It supports input data high/ low bit reversal and output data high/ low bit reversal. It supports input data with different valid bit widths.

CRC1 is located in HPSYS, and CRC2 is located in LPSYS.

Features of CRC:

- 7/8/16/32-bit CRC calculation
- Any custom polynomial
- Any initial value
- Supports single byte/ double byte/ triple byte/ quadruple byte valid bit width for input data
- Supports byte/ double byte/ quadruple byte high and low bit reversal for input data
- Supports high and low bit reversal for output data
- Calculation speed is 1 byte per HCLK cycle

3.7.4 True Random Number Generator (TRNG)

The TRNG (True Random Number Generator) is a module that generates random numbers based on the instability of oscillation circuits. No external random entropy source is required for this module, and the random numbers can be generated by activating multiple internal oscillation circuits with a certain entropy source processing logic.

Features of TRNG:

- Independent internal entropy source
- Generate 256-bit seeds and 256-bit random numbers in a single pass
- Deadlock check against entropy source

3.8 Memory Interfaces

3.8.1 MPI

MPI (Memory Peripheral Interface) controller is a dedicated memory communication interface which supports a variety of off-chip memory particles, including:

- SPI NOR Flash, support 1-wire/ 2-wire/ 4-wire, support DTR mode
- SPI NAND Flash, support 1-wire/ 2-wire/ 4-wire
- pSRAM, support x8 and x16 data width, support Xccela standard interface, compatible with Legacy interface
- HyperRAM, support x8 and x16 data width, support HyperBus standard interface

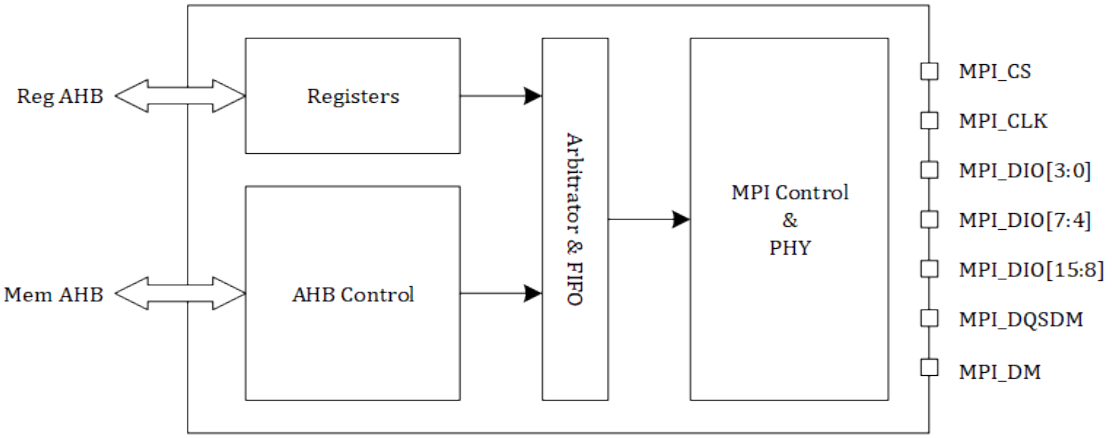


Figure 3-10: MPI Controller Block Diagram

The MPI controller supports two modes of operation: (1) register mode and (2) address-mappping mode. The switching between the two modes is automatically completed by the hardware and can be dynamically interspersed for execution. In either mode, highly customizable interface timing is supported for compatibility with various memory particles.

Register Mode:

- Send a command timing via register operation. The command can also be set as a status query command to be sent repeatedly until the read back data meets a preset status
- Support sending a sequence of two command timings, the second of which can be set as a status query command to be sent repeatedly until the read back data meets a preset status
- Support DMA channels, data handling is completed through the register FIFO interface

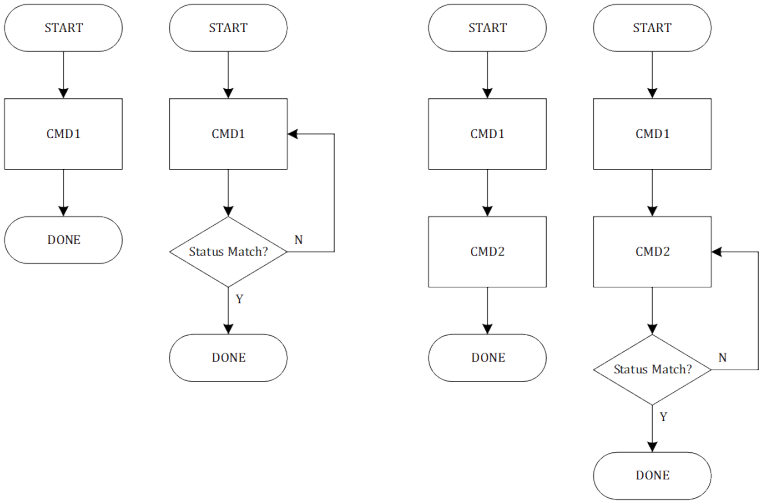


Figure 3-11: Sequence of Single and Multiple Command Timings in Register Mode

Address mapping mode:

- Map the external memory to the AHB address space, and convert the bus read and write to the preset Memory interface timing, realize XIP function
- Support Byte (8-bit), Half-word (16-bit) and Word (32-bit) AHB access
- Efficient conversion of AHB Wrap operations, independent of whether the particles support Wrap or not

- Support XIP real-time (On-The-Fly) decryption, the mode is AES128-CTR or AES256-CTR
- Support continuous read and write function, if the read and write address of the current AHB is continuous with the previous one, the data transmission will be started directly, and the command and address part will be omitted. This feature can greatly increase the effective bandwidth when handling large blocks of data.
- For the internal dynamic refresh feature of pSRAM and HyperRAM, the maximum CS pull-down time of particles, the nearest CS access interval, the maximum burst data length and other restrictions are automatically processed without software processing.

3.8.2 SD/SDIO/eMMC

SDMMC supports SD protocol 3.0 and eMMC standard 4.51, and can be used as a HOST controller to interact with SD/SDIO/eMMC devices. SDMMC has a built-in chained DMA controller and 1K byte FIFO, which can read and write data independently, supporting block data handling. SDMMC supports SDR single-wire, 4-wire and 8-wire modes, and supports DDR 4-wire and 8-wire modes.

Both SDMMC1 and SDMMC2 are located in HPSYS, SDMMC2 doesn't support 8-wire mode.

Features of SDMMC:

- Compatible with SD Host Controller Standard Specification Version 3.0
- Compatible with SD 3.0 Physical Layer Specification Version 3.01
- Compatible with SDIO Specification Version 3.0
- Compatible with JEDEC JESD84-B451 eMMC 4.51 Specification
- Support SDSC/SDHC/SDXC/SDHS card
- Support UHS-1: SDR12/SDR25/SDR50/SDR104/DDR50
- Support SDR single-wire, 4-wire and 8-wire modes
- Support DDR 4-wire and 8-wire modes
- Built-in 1K byte FIFO, support up to 512 bytes in a single block
- Configurable clock
- Support chained DMA

3.9 CAN

CAN (Controller Area Network) is compatible with CAN protocol 2.0b, and can be extended to support CAN FD. CAN can configure the base transmission rate,and support the rate switching function of CAN FD. CAN has internal receiving FIFO and transmitting FIFO, supporting multi-frame auto-transmitting/receiving, auto-retransmission, preemptive transmission and other functions. CAN includes configurable receiving ID auto-filters that retain filtered frames only in the receiving FIFO. When abnormal bus and transmitting/receiving are detected, CAN has a complete error notification mechanism.

CAN1 and CAN2 are located in HPSYS.

Features of CAN:

- Compatible with CAN 2.0b, support CAN FD
- Configurable data rate, CAN2.0b up to 1Mbps
- CAN FD frame data length up to 64byte, and support rate switching
- Receiving FIFO depth 16, transmitting FIFO depth 16+1
- 16 configurable ID filters

- Support frame preemptive transmitting
- Error detection and notification mechanism

3.10 Summary of Peripheral Interface Rates

Table 3-2: Common Interface Rates

Controller	Max. Rate	Unit	Remarks
MPI1	144	MHz	SiP OPI/HPI-PSRAM
MPI2	144	MHz	SiP OPI/HPI-PSRAM
MPI3	96	MHz	External QSPI-NOR, QSPI-NAND Flash
MPI4	96	MHz	External QSPI-NOR, QSPI-NAND Flash
MPI5	48	MHz	SiP QSPI-NOR, DTR
SDMMC	96	MHz	External eMMC
I2C	3.4	MHz	
SPI1/2	48	MHz	
SPI3/4	8	MHz	
UART	3	Mbaud	
I2S	48	KHz	Sampling rate 48KHz, 32-bit×2 channel
PDM	3.072	MHz	
CAN	1	MHz	
GPADC	4	Msps	
SDADC	4	Ksps	

4 Electrical Characteristics

4.1 Basic Electrical Characteristics

Table 4-1: Operating Conditions

Symbol	Description	Min	Typ	Max	Unit
VDD	Power supply voltage from external source	1.7	3.3	3.6	V
T_{amb}	Ambient temperature	-30		+80	°C
V_{IL}	CMOS low level input voltage	0		$0.3\times V_{IO}$	V
V_{IH}	CMOS high level input voltage	$0.7\times V_{IO}$		V_{IO}	V
V_{TH}	CMOS threshold voltage		$0.5\times V_{IO}$		V

Table 4-2: Absolute Max. Ratings

Symbol	Description	Min	Typ	Max	Unit
VDD	Power supply voltage from external source			3.6	V
$T_{Storage}$	Storage temperature	-40		125	°C
V_{IN}	Input voltage	0		V_{IO}+0.3	V
V_{LNA}	LNA input level			0	dBm
I_{IN}	Input current			20	mA

Table 4-3: PMU Power Supply Specifications

PMU Power Pin	Min. Voltage(V)	Typ. Voltage(V)	Max. Voltage(V)	Max. Current(mA)	Description
PVDD1	1.71	1.8	3.6	100	PVDD1 power input
PVDD2	1.71	1.8	3.6	50	PVDD2 power input
BUCK1_LX BUCK1_FB	-	1.25	-	100	BUCK1_LX output, connected to inductor Internal power input 1, connected to the other end of the inductor, and the external capacitor
BUCK2_LX BUCK2_FB	-	0.9	-	50	BUCK2_LX output, connected to inductor Internal power input 2, connected to the other end of the inductor, and external capacitor
LDO_VOUT1	-	1.1	-	100	LDO output, external capacitor
VDD_RET	-	0.9	-	1	RET LDO output, external capacitor
VDD_RTC	-	1.1	-	1	RTC LDO output, external capacitor

Table 4-4: Other Power Supply Specifications

Other Power Pin	Min. Voltage(V)	Typ. Voltage(V)	Max. Voltage(V)	Max. Current(mA)	Description
AVDD_BRF	1.71	1.8	3.3	1	RF power input
AVDD18_DSI	1.71	1.8	2.5	20	MIPI DSI power input
AVDD33_ANA	3.15	3.3	3.45	50	Analog power supply+RF PA power input
AVDD33_AUD	3.15	3.3	3.45	50	Analog audio power input
AVDD33_USB	3.15	3.3	3.45	50	USB power input
MIC_BIAS	1.4	-	2.8	-	MIC power output
VDDIOA	1.71	1.8	3.45	-	PA12-PA93 I/O power input
VDDIOA2	1.71	1.8	3.45	-	PA0-PA11 I/O power input
VDDIOB	1.71	1.8	3.45	-	PB I/O power input
VDDIOSA	1.71	1.8	1.8	-	SIPA power input
VDDIOSB	1.71	1.8	1.8	-	SIPB power input
VDDIOSC	1.71	1.8	1.8	-	SIPC power input

4.2 Reliability

Table 4-5: Reliability Test

Test Item	Test Condition	Applicable Product	Test Criteria
HTOL	Tj=125°C, 1000 hours	SF32LB58x	JESD22-A108
ESD	HBM（Human Body Mode）± 3000 V	SF32LB58x	JS-001-2017
	CDM（Charge Device Mode）±1000V	SF32LB58x	JS-002-2018
Latch-up	I-Test: ± 200mA	SF32LB58x	JESD78E
	OVT: +1.5×Vdd_{MAX}	SF32LB58x	
MSL3	Baking: 125°C, 24 hours Soaking: 30°C, 60% RH, 192 hours Reflow Soldering: 260 + 0°C, 20 seconds, 3 times	SF32LB58x	JESD22-A113
TCT	-65°C~150°C, Dwell=15min, 1000 cycles	SF32LB58x	JESD22-A104
uHAST	130°C, 85% RH, 33.3psig, 96 hours	SF32LB58x	JESD22-A118
HTSL	Ta=150°C, 1000 hours	SF32LB58x	JESD22-A103

4.3 Power Consumption Characteristics

4.3.1 Power Consumption at Shutdown

Table 4-6: Power Consumption at Shutdown

Symbol	1.8V Power Supply (Typical Value)	Unit
$I_{POWER\ OFF\ (RTC\ wake\text{-}up)}$	683.3	nA
$I_{POWER\ OFF\ (Key\ wake\text{-}up)}$	429.3	nA

4.3.2 Processor Power Consumption

Table 4-7: Processor Power Consumption

Symbol	Condition		@1.8V Current (mA)	@1.8V Current Increment (uA/MHz)	@3.8V Current (mA)	@3.8V Current Increment (uA/MHz)
$I_{CoreMark}$	HPSYS	240MHz	19.652	59.479	10.34	31.305
		192MHz	16.797		8.84	
	LPSYS	48MHz	1.695	27.583	0.89	14.518
		24MHz	1.033		0.54	
$I_{WhileLoop}$	HPSYS	240MHz	15.168	40.375	7.98	21.250
		192MHz	13.23		6.96	
	LPSYS	48MHz	1.265	18.708	0.67	9.846
		24MHz	0.816		0.43	

* 1. The above power consumption of 3.8V supply voltage is calculated based on the test data of 1.8V and 3.3V power supply according to the efficiency (calculation formula: $I_{3.8V} = I_{1.8V} \times 1.8/90\%/3.8+I_{3.3V}$).

4.3.3 BLE Power Consumption

Table 4-8: BLE Power Consumption

Symbol	Condition	1.8V Power Supply (Typical Value)	3.8V Power Supply (Typical Value)	Unit
$I_{\triangle TX}$	TX_{POWER}=0dBm	4.19	2.21	mA
$I_{\triangle RX}$		4.03	2.12	mA

4.3.4 Average Power Consumption of BLE and Classic Bluetooth in Various States

Table 4-9: Average Power Consumption of BLE and Classic Bluetooth in Various States

Mode	Condition	3.8V @TXpower=0dBm Typical Value	3.8V @TXpower=10dBm* Typical Value	Unit
ΔBT Sniff Mode	50ms (attempt=1)	146.4	178.6	uA
	100ms (attempt=1)	73.2	89.3	uA
	200ms (attempt=1)	36.6	44.7	uA
	500ms (attempt=1)	14.6	17.9	uA
	1s (attempt=1)	7.3	8.9	uA
ΔBLE ADV	50ms	166.9	251.8	uA
	100ms	83.4	125.9	uA
	200ms	41.7	63.0	uA
	500ms	16.7	25.2	uA
	1s	8.3	12.6	uA
ΔBLE Connection	50ms	128.8	148.4	uA
	100ms	64.4	74.2	uA
	200ms	32.2	37.1	uA
	500ms	12.9	14.8	uA
	1s	6.4	7.4	uA
ΔScan	Inquiry Scan or Page Scan	53.0		uA
ΔBoth Scan	Inquiry Scan and Page Scan	106.1		uA
Standby		4.2		uA

* 1. Scan receives 28.4ms per 1.28s, Both Scan receives 56.8ms per 1.28s.

2. Power supply: PVDD_PMU1+PVDD_PMU2+AVDDBRF+DSI+ANA_3V3

3. The above power consumption of 3.8V supply voltage is calculated based on the test data of 1.8V and 3.3V power supply according to the efficiency (calculation formula: $I_{3.8V} = I_{1.8V} \times 1.8/90\%/3.8+I_{3.3V}$).

4. Calculation example:

bt 500ms sniff @TXpower10dBm: =17.9+4.2=22.1uA

bt 500ms sniff + ble 500ms connection @TXpower10dBm: =17.9+28.7+4.2=50.8uA

4.4 Bluetooth RF

4.4.1 BLE RF

4.4.1.1 BLE Transmitter Characteristics

Table 4-10: BLE Transmitter Characteristics – 1Mbps

Parameter	Condition	Min	Typ	Max	Unit
Maximum RF transmit power			19		dBm
RF power control range		-20		19	dBm
Adjacent channel transmit power (@+19dBm)	F = F_0+2MHz		-27	-20	dBm
	F = F_0-2MHz		-27	-20	dBm
	F = F_0+3MHz		-31	-30	dBm
	F = F_0-3MHz		-31	-30	dBm
	F = F_0+>3MHz		-38	-30	dBm
	F = F_0->3MHz		-38	-30	dBm
Δf_{1avg} Maximum modulation		225	250	275	kHz
Δf_{2max} Minimum modulation		185	210		kHz
$\Delta f_{2avg}/\Delta f_{1avg}$		0.8	0.89		
ICFT		-150	±20	150	kHz
Drift rate		-20	±4	20	kHz/50us
Drift		-50	±4	50	kHz
Harmonic spur (@+19dBm transmit power)	Second harmonic		-50*		dBm
	Third harmonic		-40*		dBm

* With external π type matching network

Table 4-11: BLE Transmitter Characteristics – 2Mbps

Parameter	Condition	Min	Typ	Max	Unit
Maximum RF transmit power			19		dBm
RF power control range		-20		19	dBm
Adjacent channel transmit power (@+19dBm)	F = F_0+4MHz		-37	-20	dBm
	F = F_0-4MHz		-37	-20	dBm
	F = F_0+5MHz		-38	-20	dBm
	F = F_0-5MHz		-38	-20	dBm
	F = F_0+>5MHz		-42	-30	dBm
	F = F_0->5MHz		-42	-30	dBm
Δf_{1avg} Maximum modulation		450	500	550	kHz
Δf_{2max} Minimum modulation		370	420		kHz
$\Delta f_{2avg}/\Delta f_{1avg}$		0.8	0.89		
ICFT		-150	±20	150	kHz
Drift rate		-20	±4	20	kHz/50us
Drift		-50	±4	50	kHz
Harmonic Spur (@+19dBm transmit power)	Second harmonic		-50*		dBm
	Third harmonic		-40*		dBm

* With external π type matching network

4.4.1.2 BLE Receiver Characteristics

Table 4-12: BLE Receiver Characteristics – 1Mbps

Parameter	Condition	Min	Typ	Max	Unit
Sensitivity with dirty off@30.8% PER & 37bytes		/	-100	/	dBm
Sensitivity with dirty on@30.8% PER & 37bytes		/	-99.3	/	dBm
Maximum received signal@30.8% PER		/	0	/	dBm
C/I co-channel			7		dB
Adjacent channel selectivity C/I	F = F_0+1MHz		-10		dB
	F = F_0-1MHz		-7		dB
	F = F_0+2MHz		-43		dB
	F = F_0-2MHz		-40		dB
	F = F_0+3MHz		-50		dB
	F = F_0-3MHz		-40		dB
	F = F_{image}(F_0-4MHz)		-24		dB
Out of band blocking performance	30MHz~2000MHz		-11		dBm
	2000MHz~2400MHz		-25		dBm
	2500~3000MHz		-25		dBm
	3000MHz~12.5GHz		-10		dBm
Intermodulation			-24		dBm

Table 4-13: BLE Receiver Characteristics – 2Mbps

Parameter	Condition	Min	Typ	Max	Unit
Sensitivity with dirty off@30.8% PER & 37bytes		/	-97	/	dBm
Sensitivity with dirty on@30.8% PER & 37bytes		/	-96.5	/	dBm
Maximum received signal@30.8% PER		/	0	/	dBm
C/I co-channel			7		dB
Adjacent channel selectivity C/I	F = F_0+2MHz		-10		dB
	F = F_0-2MHz		-8		dB
	F = F_0+4MHz		-44		dB
	F = F_0-4MHz		-34		dB
	F = F_0+6MHz		-50		dB
	F = F_0-6MHz		-24		dB
	F = F_{image}(F_0-6MHz)		-24		dB
Out of band blocking performance	30MHz 2000MHz		-11		dBm
	2000MHz-2400MHz		-25		dBm
	2500-3000MHz		-25		dBm
	3000MHz-12.5GHz		-10		dBm
Intermodulation			-25		dBm

Table 4-14: BLE Receiver Characteristics – S2 Mode

Parameter	Condition	Min	Typ	Max	Unit
Sensitivity with dirty transmit off@30.8% PER & 37bytes		/	-104.5	/	dBm
Sensitivity with dirty transmit on@30.8% PER & 37bytes		/	-104	/	dBm
Maximum received signal@30.8% PER		/	0	/	dBm
C/I co-channel			2		dB
Adjacent channel selectivity C/I	F = F0+1MHz		-12		dB
	F = F0-1MHz		-9		dB
	F = F0+2MHz		-48		dB
	F = F0-2MHz		-43		dB
	F = F0+3MHz		-58		dB
	F = F0-3MHz		-43		dB
Adjacent channel selectivity C/I	F = Fimage(F0-4MHz)		-31		dB

Table 4-15: BLE Receiver Characteristics – S8 Mode

Parameter	Condition	Min	Typ	Max	Unit
Sensitivity with dirty transmit off@30.8% PER & 37bytes		/	-107.5	/	dBm
Sensitivity with dirty transmit on@30.8% PER & 37bytes		/	-107	/	dBm
Maximum received signal@30.8% PER		/	0	/	dBm
C/I co-channel			1		dB
Adjacent channel selectivity C/I	F = F0+1MHz		-12		dB
	F = F0-1MHz		-9		dB
	F = F0+2MHz		-48		dB
	F = F0-2MHz		-44		dB
	F = F0+3MHz		-58		dB
	F = F0-3MHz		-44		dB
Adjacent channel selectivity C/I	F = Fimage(F0-4MHz)		-32		dB

4.4.2 Classic Bluetooth

4.4.2.1 Transmitter Characteristics

Table 4-16: Transmitter Characteristics – Basic Data Rate

Parameter	Condition	Min	Typ	Max	Unit
Maximum RF transmit power			19		dBm
RF power control step		2	4	8	dB
Adjacent channel transmit power	F = F_0+2MHz		-37	-20	dBm
	F = F_0-2MHz		-37	-20	dBm
	F = F_0+3MHz		-41	-40	dBm
	F = F_0-3MHz		-41	-40	dBm
	F = F_0+>3MHz		-44	-40	dBm
	F = F_0->3MHz		-44	-40	dBm
Δf_{1avg} modulation		140	160	175	kHz
Δf_{2max} modulation		120	150	175	kHz
$\Delta f_{2avg}/\Delta f_{1avg}$		0.8	0.9		
ICFT		-75	0	75	kHz
Drift (1 slot packet)		-25	0	25	kHz
Drift (5 slot packet)		-40	0	40	kHz
Harmonic spur	3G-20GHz		-35		dBm

Table 4-17: Transmitter Characteristics – Enhanced Data Rate

Parameter	Condition	Min	Typ	Max	Unit
Maximum RF transimit power			13		dBm
DPSK Power - GFSK Power	2-DH5		0		dB
π/4 DQPSK max w_0		-10	0	10	kHz
π/4 DQPSK max w_i		-75	0	+75	kHz
π/4 DQPSK max $\|w_i + w_0\|$		-75	0	+75	kHz
8DPSK max w_0		-10	0	10	kHz
8DPSK max w_i		-75	0	+75	kHz
8DPSK max $\|w_i + w_0\|$		-75	0	+75	kHz
π/4 DQPSK modulation accuracy	RMS DEVM		6	20	%
	99% DEVM		11	30	%
	Peak DEVM		16	35	%
8DPSK modulation accuracy	RMS DEVM		6	13	%
	99% DEVM		11	20	%
	Peak DEVM		16	25	%
In-band spurious emissions	F=F_0+1MHz		-39	-26	dB
	F=F_0-1MHz		-41	-26	dB
	F=F_0+2MHz		-28	-20	dBm
	F=F_0-2MHz		-29	-20	dBm
	F=F_0+3MHz		-39*		dBm
	F=F_0-3MHz		-39*		dBm
	F=F_0+>3MHz		-40	-40	dBm
	F=F_0->3MHz		-40	-40	dBm
EDR differential phase encoding			99	100	%

* Exceptions in up to 3 bands are allowed. For exceptions, PTX $\leq$ -20dBm.

4.4.2.2 Receiver Characteristics

Table 4-18: Receiver Characteristics – Basic Data Rate

Parameter	Condition	Min	Typ	Max	Unit
Sensitivity with dirty transmit off@0.1% BER		/	-96.3	/	dBm
Sensitivity with dirty transmit on@0.1% BER		/	-94	/	dBm
Maximum received signal@0.1% BER		0	/	/	dBm
C/I co-channel			10		dB
Adjacent channel selectivity C/I	F = F_0+1MHz		-13		dB
	F = F_0-1MHz		-10		dB
	F = F_0+2MHz		-42		dB
	F = F_0-2MHz		-43		dB
	F = F_0+3MHz		-48		dB
	F = F_0-3MHz		-45		dB
	F = F_{image}(F_0-5MHz)		-31		dB
Out of band blocking performance	30MHz~2000MHz	-10	-10		dBm
	2000MHz~2400MHz	-27	-10		dBm
	2500~3000MHz	-27	-10		dBm
	3000MHz~12.5GHz	-10	-10		dBm
Intermodulation			-22		dBm

Table 4-19: Receiver Characteristics – Enhanced Data Rate-π/4 DQPSK

Parameter	Condition	Min	Typ	Max	Unit
Sensitivity with dirty transmit off@0.01% BER		/	-95.5	/	dBm
Sensitivity with dirty transmit on@0.01% BER		/	-95	/	dBm
Maximum received signal@0.01% BER		/	0	/	dBm
C/I co-channel			11		dB
Adjacent channel selectivity C/I	F = F_0+1MHz		-13		dB
	F = F_0-1MHz		-9		dB
	F = F_0+2MHz		-35		dB
	F = F_0-2MHz		-31		dB
	F = F_0+3MHz		-41		dB
	F = F_0-3MHz		-41		dB
	F = F_{image}(F_0-5MHz)		-30		dB

Table 4-20: Receiver Characteristics – Enhanced Data Rate-8DPSK

Parameter	Condition	Min	Typ	Max	Unit
Sensitivity with dirty transmit off@0.01% BER		/	-88.5	/	dBm
Sensitivity with dirty transmit on@0.01% BER		/	-87	/	dBm
Maximum received signal@0.01% BER		/	0	/	dBm
C/I co-channel			17		dB
Adjacent channel selectivity C/I	F = F_0+1MHz		-4		dB
	F = F_0-1MHz		-5		dB
	F = F_0+2MHz		-29		dB
	F = F_0-2MHz		-29		dB
	F = F_0+3MHz		-39		dB
	F = F_0-3MHz		-39		dB
	F = F_{image}(F_0-5MHz)		-28		dB

4.5 Audio Characteristics

Table 4-21: Audio ADC Characteristics

Analogue to Digital Converter under 3.3V

Parameter	Test Condition	Min	Typ	Max	Unit
Resolution		/	/	24	Bits
Sample Frequency		8	/	48	kHz
Analog Gain Range	1dB/Step	-20		10	dB
Input Resistance	Analog Gain = 0dB, @48kHz Sample Frequency	/	23	/	KΩ
Dynamic Range	1kHz -60dBFS Input, @48kHz Sample Frequency, Output A-Weighted	/	99	/	dB
Signal to Noise Ratio	1kHz Input, @48kHz Sample Frequency, Output A-Weighted	/	99	/	dB
Total Harmonic Distortion+Noise	Analog Gain = 0dB, 1kHz Input, @48kHz Sample Frequency	/	-90	/	dB

Table 4-22: Audio DAC Characteristics

Digital to Analogue Converter under 3.3V

Parameter	Test Condition	Min	Typ	Max	Unit
Resolution		/	/	24	Bits
Output Swing			0.9		Vrms
Sample Frequency		8	/	48	kHz
Total Harmonic Distortion+Noise	1kHz Output, 0dBFS, with 10kOhm Loading, @48kHz Sample Frequency, Output A-Weighted	/	-101	/	dB
Dynamic Range	1kHz Output, -60dBFS, with 10kOhm Loading, @48kHz Sample Frequency, Output A-Weighted	/	109	/	dB
Noise Floor		/	3.3	/	μV rms
Signal to Noise Ratio	1kHz Output, 0dBFS, with 10kOhm Loading, @48kHz Sample Frequency, Output A-Weighted	/	109	/	dB

4.6 IO Drive Strength

Table 4-23: IO Drive Strength

DS0	DS1	Driving Capability
0	0	2mA
0	1	4mA
1	0	8mA
1	1	12mA

5 Packaging and Hardware

5.1 Pin Layout

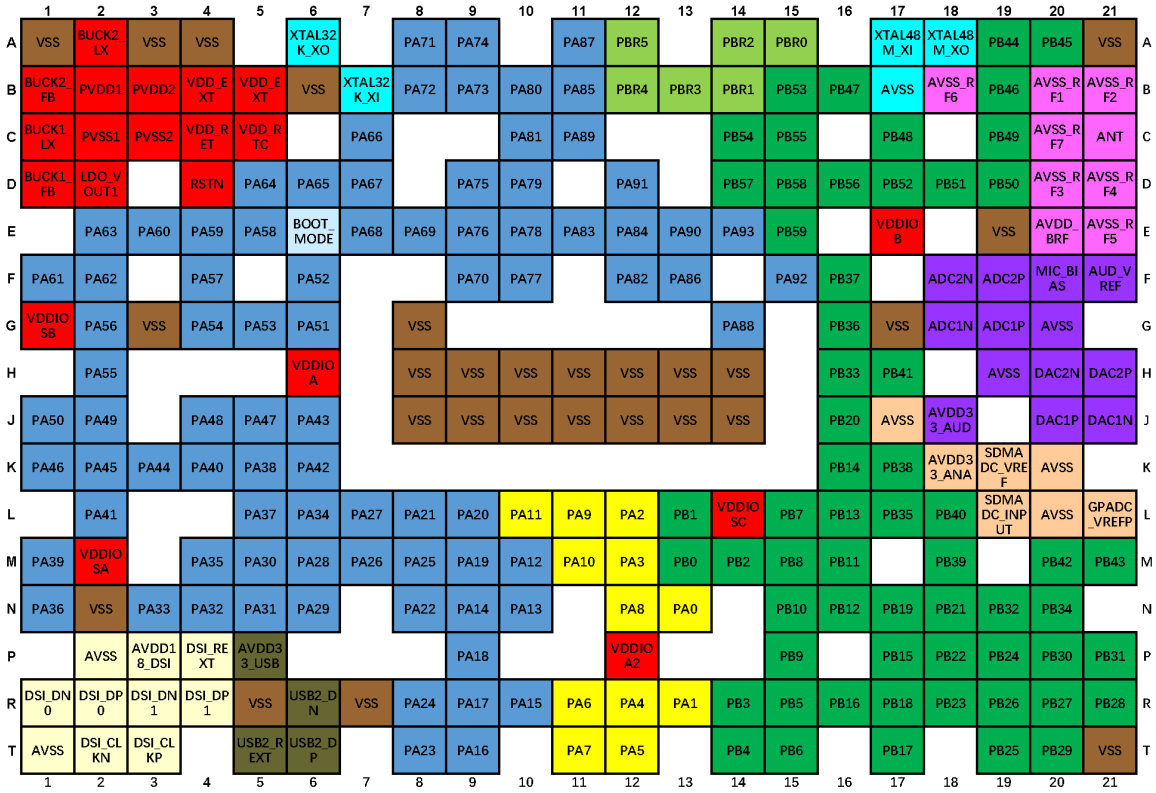


Figure 5-1: SF32LB58x (BGA256) Pin Layout (Top View)

5.2 Pin Description

The pin types of this chip are shown in Table 5-1, and the following text will describe the big core domain GPIO, LITTLE core domain GPIO and other dedicated pins respectively.

Table 5-1: Pin Types

Pin Type	Description
I/O	Digital input/output
I	Digital input
O	Digital output
A, I	Analog input
A, O	Analog output
A, I/O	Analog input/output
PWR	Power
GND	Ground

Notes:

- In low-power scenarios, floating inputs may cause the power consumption of digital I/Os with the input function turned on to rise, so such I/Os need to be configured with a determined voltage according to their function, either by connecting to I/Os with determined output voltages on other chips, or by connecting corresponding pull-up or pull-down resistors.

5.2.1 Big Core Domain GPIO (PA) List

Table 5-2: GPIO (PA) Pin List

Pin Number SF32LB58x (BGA256)	Pin Name	Type	Sel #	Function
N13	PA00	I/O	0	GPIO_A0
			1	SD1_DIO7
			3	CAN1_TXD
			4	I2C1_SCL
			5	ATIM1_CH1
			6	UART3_RXD
			Others	Reserved
R13	PA01	I/O	0	GPIO_A1
			1	SD1_DIO2
			2	MPI4_DIO2
			Others	Reserved
L12	PA02	I/O	0	GPIO_A2
			2	SD1_CLKIN
			3	CAN2_RXD
			5	ATIM1_CH1N
			6	UART3_RXD
			Others	Reserved
M12	PA03	I/O	0	GPIO_A3
			1	SD1_DIO5
			3	CAN1_RXD
			4	I2C1_SDA
			5	ATIM1_CH2
			6	UART3_TXD
			Others	Reserved
R12	PA04	I/O	0	GPIO_A4
			1	SD1_DIO1
			2	MPI4_DIO1
			Others	Reserved
T12	PA05	I/O	0	GPIO_A5
			1	SD1_DIO0
			2	MPI4_DIO0
			Others	Reserved
R11	PA06	I/O	0	GPIO_A6
			1	SD1_DIO3
			2	MPI4_DIO3
			Others	Reserved
T11	PA07	I/O	0	GPIO_A7
			1	SD1_DIO4
			2	SCI_CLK
			3	UART2_TXD
			5	ATIM1_CH2N
			Others	Reserved

Continued on the next page

Table 5-2: GPIO (PA) Pin List (continued)

Pin Number SF32LB58x (BGA256)	Pin Name	Type	Sel #	Function
N12	PA08	I/O	0	GPIO_A8
			1	SD1_DIO6
			2	SCI_DIO
			3	UART2_RXD
			5	ATIM1_CH3
			Others	Reserved
L11	PA09	I/O	0	GPIO_A9
			1	SD1_CLK
			2	MPI4_CLK
			Others	Reserved
M11	PA10	I/O	0	GPIO_A10
			1	SD1_CMD
			2	MPI4_CS
			Others	Reserved
L10	PA11	I/O	0	GPIO_A11
			2	SCI_RST
			3	CAN2_TXD
			4	I2C1_SDA
			5	ATIM1_CH3N
			6	UART3_TXD
			Others	Reserved
M10	PA12	I/O	0	GPIO_A12
			4	GPTIM1_CH1
			5	ATIM1_CH4
			7	LCDC1_DPI_CLK
			Others	Reserved
N10	PA13	I/O	0	GPIO_A13
			4	GPTIM1_CH2
			5	ATIM1_BKIN
			7	LCDC1_DPI_DE
			Others	Reserved
N9	PA14	I/O	0	GPIO_A14
			2	I2S1_LRCK
			7	LCDC1_DPI_HSYNC
			Others	Reserved
R10	PA15	I/O	0	GPIO_A15
			4	GPTIM1_CH3
			5	ATIM1_BKIN2
			7	LCDC1_DPI_VSYNC
			Others	Reserved
T9	PA16	I/O	0	GPIO_A16
			1	I2C1_SDA
			2	UART2_TXD
			Others	Reserved

Continued on the next page

Table 5-2: GPIO (PA) Pin List (continued)

Pin Number SF32LB58x (BGA256)	Pin Name	Type	Sel #	Function
R9	PA17	I/O	0	GPIO_A17
			1	I2C1_SCL
			2	UART2_RXD
			Others	Reserved
P9	PA18	I/O	0	GPIO_A18
			1	PDM1_DATA
			2	I2S1_SDI
			3	UART2_RTS
			4	I2C2_SCL
			7	LCDC1_DPI_SD
			Others	Reserved
M9	PA19	I/O	0	GPIO_A19
			2	SCI_RST
			4	GPTIM1_CH4
			5	ATIM1_ETR
			7	LCDC1_DPI_CM
			8	LCDC1_JDI_VCK
			Others	Reserved
L9	PA20	I/O	0	GPIO_A20
			1	UART3_RXD
			2	SPI1_DI
			3	UART2_CTS
			Others	Reserved
L8	PA21	I/O	0	GPIO_A21
			1	UART3_TXD
			2	SPI1_DO
			3	UART2_RTS
			Others	Reserved
N8	PA22	I/O	0	GPIO_A22
			1	PDM2_DATA
			4	GPTIM1_ETR
			5	ATIM2_CH1
			7	LCDC1_DPI_R0
			8	LCDC1_JDI_VST
			Others	Reserved
T8	PA23	I/O	0	GPIO_A23
			1	PDM1_CLK
			2	I2S1_BCK
			3	UART2_CTS
			4	I2C2_SDA
			7	LCDC1_DPI_R1
			Others	Reserved
R8	PA24	I/O	0	GPIO_A24
			5	LCDC1_8080_RSTB
			6	LCDC1_SPI_RSTB
			7	LCDC1_DPI_R2
			Others	Reserved

Continued on the next page

Table 5-2: GPIO (PA) Pin List (continued)

Pin Number SF32LB58x (BGA256)	Pin Name	Type	Sel #	Function
M8	PA25	I/O	0	GPIO_A25
			1	PDM2_CLK
			2	SD1_CLKIN
			4	GPTIM2_CH1
			5	ATIM2_CH1N
			7	LCDC1_DPI_R3
			8	LCDC1_JDI_XRST
			Others	Reserved
M7	PA26	I/O	0	GPIO_A26
			2	SCI_CLK
			4	GPTIM2_CH2
			5	ATIM2_CH2
			6	LCDC1_8080_DIO2
			7	LCDC1_DPI_R4
			Others	Reserved
L7	PA27	I/O	0	GPIO_A27
			2	SCI_DIO
			4	GPTIM2_CH3
			5	ATIM2_CH2N
			6	LCDC1_8080_DIO3
			7	LCDC1_DPI_R5
			8	LCDC1_JDI_XRST
			Others	Reserved
M6	PA28	I/O	0	GPIO_A28
			1	UART2_TXD
			2	SPI1_CLK
			4	I2C2_SCL
			Others	Reserved
N6	PA29	I/O	0	GPIO_A29
			1	UART2_RXD
			2	SPI1_CS
			4	I2C2_SDA
			Others	Reserved
M5	PA30	I/O	0	GPIO_A30
			1	SPI2_CS
			2	SD1_DIO1
			3	MPI4_CS
			Others	Reserved
N5	PA31	I/O	0	GPIO_A31
			1	UART1_TXD
			4	I2C3_SCL
			Others	Reserved
N4	PA32	I/O	0	GPIO_A32
			1	UART1_RXD
			4	I2C3_SDA
			Others	Reserved

Continued on the next page

Table 5-2: GPIO (PA) Pin List (continued)

Pin Number SF32LB58x (BGA256)	Pin Name	Type	Sel #	Function
N3	PA33	I/O	0	GPIO_A33
			2	SD1_DIO7
			5	UART2_CTS
			Others	Reserved
L6	PA34	I/O	0	GPIO_A34
			2	SD1_CMD
			5	UART2_RTS
			Others	Reserved
M4	PA35	I/O	0	GPIO_A35
			2	SD1_DIO6
			5	UART3_CTS
			Others	Reserved
N1	PA36	I/O	0	GPIO_A36
			2	SD1_DIO2
			3	MPI4_DIO2
			Others	Reserved
L5	PA37	I/O	0	GPIO_A37
			1	SPI2_DO
			2	SD1_DIO5
			3	MPI4_DIO1
			4	SPI2_DIO
			Others	Reserved
K5	PA38	I/O	0	GPIO_A38
			2	SD1_DIO4
			3	MPI4_DIO3
			Others	Reserved
M1	PA39	I/O	0	GPIO_A39
			1	SPI2_CLK
			2	SD1_CLK
			3	MPI4_CLK
			Others	Reserved
K4	PA40	I/O	0	GPIO_A40
			1	SPI2_DI
			2	SD1_DIO3
			3	MPI4_DIO0
			Others	Reserved
L2	PA41	I/O	0	GPIO_A41
			2	SD1_DIO0
			5	UART3_RTS
			Others	Reserved
K6	PA42	I/O	0	GPIO_A42
			4	GPTIM2_CH4
			5	ATIM2_CH3
			6	LCDC1_8080_DIO4
			Others	Reserved

Continued on the next page

Table 5-2: GPIO (PA) Pin List (continued)

Pin Number SF32LB58x (BGA256)	Pin Name	Type	Sel #	Function
J6	PA43	I/O	0	GPIO_A43
			5	LCDC1_8080_TE
			6	LCDC1_SPI_TE
			7	LCDC1_DPI_R6
			8	LCDC1_JDI_HCK
			Others	Reserved
K3	PA44	I/O	0	GPIO_A44
			1	MPI3_CS
			5	LCDC1_8080_CS
			6	LCDC1_SPI_CS
			7	LCDC1_DPI_R7
			8	LCDC1_JDI_HST
			Others	Reserved
K2	PA45	I/O	0	GPIO_A45
			1	MPI3_DIO3
			5	LCDC1_8080_DIO1
			6	LCDC1_SPI_DIO3
			7	LCDC1_DPI_G0
			8	LCDC1_JDI_ENB
			Others	Reserved
K1	PA46	I/O	0	GPIO_A46
			1	MPI3_CLK
			5	LCDC1_8080_WR
			6	LCDC1_SPI_CLK
			7	LCDC1_DPI_G1
			8	LCDC1_JDI_R1
			Others	Reserved
J5	PA47	I/O	0	GPIO_A47
			1	MPI3_DIO2
			5	LCDC1_8080_DIO0
			6	LCDC1_SPI_DIO2
			7	LCDC1_DPI_G2
			8	LCDC1_JDI_R2
			Others	Reserved
J4	PA48	I/O	0	GPIO_A48
			1	MPI3_DIO1
			5	LCDC1_8080_DC
			6	LCDC1_SPI_DIO1
			7	LCDC1_DPI_G3
			8	LCDC1_JDI_G1
			Others	Reserved
J2	PA49	I/O	0	GPIO_A49
			4	GPTIM1_CH1
			5	ATIM2_CH3N
			Others	Reserved

Continued on the next page

Table 5-2: GPIO (PA) Pin List (continued)

Pin Number SF32LB58x (BGA256)	Pin Name	Type	Sel #	Function
J1	PA50	I/O	0	GPIO_A50
			1	MPI3_DIO0
			5	LCDC1_8080_RD
			6	LCDC1_SPI_DIO0
			7	LCDC1_DPI_G4
			8	LCDC1_JDI_G2
			Others	Reserved
G6	PA51	I/O	0	SWCLK
			1	GPIO_A51
			4	GPTIM1_CH2
			5	ATIM2_CH4
			6	LCDC1_8080_DIO5
			Others	Reserved
F6	PA52	I/O	0	SWDIO
			1	GPIO_A52
			4	GPTIM1_CH3
			5	ATIM2_BKIN
			6	LCDC1_8080_DIO6
			Others	Reserved
G5	PA53	I/O	0	GPIO_A53
			7	LCDC1_DPI_G5
			Others	Reserved
G4	PA54	I/O	0	GPIO_A54
			1	SPI1_DO
			2	SPI1_DIO
			3	UART2_RTS
			7	LCDC1_DPI_G6
			Others	Reserved
H2	PA55	I/O	0	GPIO_A55
			4	GPTIM1_CH4
			5	ATIM2_BKIN2
			7	LCDC1_DPI_G7
			Others	Reserved
G2	PA56	I/O	0	GPIO_A56
			1	SPI1_CLK
			3	UART2_CTS
			7	LCDC1_DPI_B0
			Others	Reserved
F4	PA57	I/O	0	GPIO_A57
			1	SPI1_DI
			2	UART2_RXD
			7	LCDC1_DPI_B1
			Others	Reserved

Continued on the next page

Table 5-2: GPIO (PA) Pin List (continued)

Pin Number SF32LB58x (BGA256)	Pin Name	Type	Sel #	Function
E5	PA58	I/O	0	GPIO_A58
			3	LPTIM1_ETR
			4	GPTIM2_CH1
			5	ATIM2_ETR
			6	LCDC1_8080_DIO7
			7	LCDC1_DPI_B2
			Others	Reserved
E4	PA59	I/O	0	GPIO_A59
			1	I2C4_SDA
			2	UART1_TXD
			3	UART3_RTS
			Others	Reserved
E3	PA60	I/O	0	GPIO_A60
			1	I2C4_SCL
			2	UART1_RXD
			3	UART3_CTS
			Others	Reserved
F1	PA61	I/O	0	GPIO_A61
			1	SPI1_CS
			2	UART2_TXD
			7	LCDC1_DPI_B3
			Others	Reserved
F2	PA62	I/O	0	GPIO_A62
			1	I2C2_SCL
			2	UART1_RTS
			3	#GPCOMP_P
			7	LCDC1_DPI_B4
			Others	Reserved
E2	PA63	I/O	0	GPIO_A63
			1	I2C2_SDA
			2	UART1_CTS
			3	#GPCOMP_N
			7	LCDC1_DPI_B5
			Others	Reserved
D5	PA64	I/O	0	GPIO_A64
			3	#WKUP_PIN6
			Others	Reserved
D6	PA65	I/O	0	GPIO_A65
			3	#WKUP_PIN7
			4	GPTIM2_CH2
			5	ATIM1_CH1
			7	LCDC1_DPI_B6
			8	LCDC1_JDI_B1
			Others	Reserved
C7	PA66	I/O	0	GPIO_A66
			3	#WKUP_PIN8
			Others	Reserved

Continued on the next page

Table 5-2: GPIO (PA) Pin List (continued)

Pin Number SF32LB58x (BGA256)	Pin Name	Type	Sel #	Function
D7	PA67	I/O	0	GPIO_A67
			3	#WKUP_PIN9
			4	GPTIM2_CH3
			5	ATIM1_CH1N
			7	LCDC1_DPI_B7
			8	LCDC1_JDI_B2
			Others	Reserved
E7	PA68	I/O	0	GPIO_A68
			3	#WKUP_PIN10
			Others	Reserved
E8	PA69	I/O	0	GPIO_A69
			3	#WKUP_PIN11
			Others	Reserved
F9	PA70	I/O	0	GPIO_A70
			1	SD2_CMD
			2	SPI2_CS
			Others	Reserved
A8	PA71	I/O	0	GPIO_A71
			1	BT_ACTIVE
			Others	Reserved
B8	PA72	I/O	0	GPIO_A72
			1	BT_PRIORITY
			Others	Reserved
B9	PA73	I/O	0	GPIO_A73
			1	BT_COLLISION
			2	UART1_RTS
			3	LPTIM1_OUT
			4	GPTIM2_CH4
			5	ATIM1_CH2
			Others	Reserved
A9	PA74	I/O	0	GPIO_A74
			1	WLAN_ACTIVE
			2	UART1_CTS
			3	LPTIM1_IN
			4	GPTIM2_ETR
			5	ATIM1_CH2N
			6	LCDC1_SPI_RSTB
			7	LCDC1_8080_RSTB
			Others	Reserved
D9	PA75	I/O	0	GPIO_A75
			1	SD2_DIO1
			2	SPI2_DI
			Others	Reserved
E9	PA76	I/O	0	GPIO_A76
			1	SD2_DIO0
			2	SPI2_DO
			Others	Reserved

Continued on the next page

Table 5-2: GPIO (PA) Pin List (continued)

Pin Number SF32LB58x (BGA256)	Pin Name	Type	Sel #	Function
F10	PA77	I/O	0	GPIO_A77
			1	SD2_CLK
			2	SPI2_CLK
			Others	Reserved
E10	PA78	I/O	0	GPIO_A78
			1	SPI2_DI
			2	SD2_CLKIN
			4	GPTIM2_ETR
			5	ATIM1_CH3
			Others	Reserved
D10	PA79	I/O	0	GPIO_A79
			1	SD2_DIO2
			Others	Reserved
B10	PA80	I/O	0	GPIO_A80
			6	LCDC1_SPI_TE
			7	LCDC1_8080_TE
			Others	Reserved
C10	PA81	I/O	0	GPIO_A81
			1	SD2_DIO3
			Others	Reserved
F12	PA82	I/O	0	GPIO_A82
			2	I2S2_SDO
			4	GPTIM1_CH1
			5	ATIM1_CH3N
			6	LCDC1_SPI_DIO1
			7	LCDC1_8080_DC
			8	LCDC1_JDI_SCS
			Others	Reserved
E11	PA83	I/O	0	GPIO_A83
			1	SPI2_CLK
			Others	Reserved
E12	PA84	I/O	0	GPIO_A84
			2	I2S2_LRCK
			4	GPTIM1_CH2
			5	ATIM2_CH1
			6	LCDC1_SPI_DIO2
			7	LCDC1_8080_DIO0
			8	LCDC1_JDI_SCLK
			Others	Reserved
B11	PA85	I/O	0	GPIO_A85
			Others	Reserved

Continued on the next page

Table 5-2: GPIO (PA) Pin List (continued)

Pin Number SF32LB58x (BGA256)	Pin Name	Type	Sel #	Function
F13	PA86	I/O	0	GPIO_A86
			2	I2S2_SDI
			4	GPTIM1_CH3
			5	ATIM2_CH1N
			6	LCDC1_SPI_DIO3
			7	LCDC1_8080_DIO1
			8	LCDC1_JDI_SO
			Others	Reserved
A11	PA87	I/O	0	GPIO_A87
			1	SPI2_CS
			Others	Reserved
G14	PA88	I/O	0	GPIO_A88
			6	LCDC1_SPI_CS
			7	LCDC1_8080_CS
			Others	Reserved
C11	PA89	I/O	0	GPIO_A89
			1	SPI2_DO
			3	SPI2_DIO
			Others	Reserved
E13	PA90	I/O	0	GPIO_A90
			2	I2S2_MCLK
			4	GPTIM1_CH4
			5	ATIM2_CH2
			6	LCDC1_SPI_CLK
			7	LCDC1_8080_WR
			8	LCDC1_JDI_DISP
			Others	Reserved
D12	PA91	I/O	0	GPIO_A91
			2	I2S2_BCK
			4	GPTIM1_ETR
			5	ATIM2_CH2N
			6	LCDC1_SPI_DIO0
			7	LCDC1_8080_RD
			8	LCDC1_JDI_EXTCOMIN
			Others	Reserved
F15	PA92	I/O	0	GPIO_A92
			1	I2C3_SCL
			2	UART3_RXD
			3	UART3_CTS
			Others	Reserved
E14	PA93	I/O	0	GPIO_A93
			1	I2C3_SDA
			2	UART3_TXD
			3	UART3_RTS
			Others	Reserved

5.2.2 LITTLE Core Domain GPIO (PB) List

Table 5-3: GPIO (PB) Pin List

Pin Number SF32LB58x (BGA256)	Pin Name	Type	Sel #	Function
M13	PB00	I/O	0	GPIO_B0
			1	I2C7_SDA
			2	UART6_RXD
			5	GPTIM3_CH1
			6	LPTIM3_IN
			Others	Reserved
L13	PB01	I/O	0	GPIO_B1
			1	I2C7_SCL
			2	UART6_TXD
			5	GPTIM3_CH2
			6	LPTIM3_OUT
			Others	Reserved
M14	PB02	I/O	0	GPIO_B2
			2	LCDC2_JDI_B1
			3	LCDC2_SPI_TE
			4	LCDC2_JDI_SCLK
			5	GPTIM3_CH3
			Others	Reserved
R14	PB03	I/O	0	GPIO_B3
			2	LCDC2_JDI_B2
			3	LCDC2_SPI_DIO1
			4	LCDC2_JDI_SCS
			5	GPTIM3_CH4
			6	UART4_RTS
			Others	Reserved
T14	PB04	I/O	0	GPIO_B4
			2	LCDC2_JDI_G2
			3	LCDC2_SPI_DIO2
			4	LCDC2_JDI_DISP
			5	GPTIM4_CH1
			6	UART4_CTS
			Others	Reserved
R15	PB05	I/O	0	GPIO_B5
			2	LCDC2_JDI_HCK
			3	LCDC2_SPI_RSTB
			4	LCDC2_JDI_EXTCOMIN
			5	GPTIM4_CH2
			6	UART6_RTS
			Others	Reserved

Continued on the next page

Table 5-3: GPIO (PB) Pin List (continued)

Pin Number SF32LB58x (BGA256)	Pin Name	Type	Sel #	Function
T15	PB06	I/O	0	GPIO_B6
			2	LCDC2_JDI_R2
			3	LCDC2_SPI_DIO3
			4	LCDC2_JDI_SO
			5	GPTIM4_CH3
			6	UART6_CTS
			Others	Reserved
L15	PB07	I/O	0	SWCLK
			1	GPIO_B7
			2	UART4_RXD
			5	GPTIM4_CH4
			Others	Reserved
M15	PB08	I/O	0	GPIO_B8
			2	LCDC2_JDI_G1
			3	LCDC2_SPI_CS
			5	GPTIM5_CH1
			6	BT_ACTIVE
			Others	Reserved
P15	PB09	I/O	0	GPIO_B9
			2	LCDC2_JDI_R1
			3	LCDC2_SPI_DIO0
			4	UART6_TXD
			5	GPTIM5_CH2
			6	WLAN_ACTIVE
			Others	Reserved
N15	PB10	I/O	0	GPIO_B10
			2	LCDC2_JDI_HST
			3	LCDC2_SPI_CLK
			4	UART6_RXD
			5	GPTIM5_CH3
			Others	Reserved
M16	PB11	I/O	0	SWDIO
			1	GPIO_B11
			2	UART4_TXD
			5	GPTIM5_CH4
			Others	Reserved
N16	PB12	I/O	0	GPIO_B12
			1	SPI4_CLK
			2	LCDC2_JDI_ENB
			3	I2C7_SCL
			Others	Reserved
L16	PB13	I/O	0	GPIO_B13
			1	UART6_RXD
			2	UART4_CTS
			5	GPTIM3_CH1
			Others	Reserved

Continued on the next page

Table 5-3: GPIO (PB) Pin List (continued)

Pin Number SF32LB58x (BGA256)	Pin Name	Type	Sel #	Function
K16	PB14	I/O	0	GPIO_B14
			1	UART6_TXD
			2	UART4_RTS
			5	GPTIM3_CH2
			Others	Reserved
P17	PB15	I/O	0	GPIO_B15
			1	SPI4_DI
			2	LCDC2_JDI_VCK
			3	UART6_CTS
			Others	Reserved
R16	PB16	I/O	0	GPIO_B16
			1	SPI4_DO
			2	LCDC2_JDI_XRST
			3	I2C7_SDA
			4	SPI4_DIO
			Others	Reserved
T17	PB17	I/O	0	GPIO_B17
			1	UART5_RXD
			2	SPI3_CLK
			Others	Reserved
R17	PB18	I/O	0	GPIO_B18
			1	UART5_TXD
			2	SPI3_DI
			Others	Reserved
N17	PB19	I/O	0	GPIO_B19
			1	SPI4_CS
			2	LCDC2_JDI_VST
			3	UART6_RTS
			Others	Reserved
J16	PB20	I/O	0	GPIO_B20
			5	GPTIM3_CH3
			Others	Reserved
N18	PB21	I/O	0	GPIO_B21
			3	SPI3_CLK
			5	GPTIM3_CH4
			Others	Reserved
P18	PB22	I/O	0	GPIO_B22
			3	SPI3_DO
			4	SPI3_DIO
			5	GPTIM4_CH1
			Others	Reserved
R18	PB23	I/O	0	GPIO_B23
			1	UART5_CTS
			2	SPI3_DO
			4	SPI3_DIO
			5	GPTIM4_CH2
			Others	Reserved

Continued on the next page

Table 5-3: GPIO (PB) Pin List (continued)

Pin Number SF32LB58x (BGA256)	Pin Name	Type	Sel #	Function
P19	PB24	I/O	0	GPIO_B24
			3	I2S3_SDO
			5	GPTIM4_CH3
			Others	Reserved
T19	PB25	I/O	0	GPIO_B25
			3	SPI3_DI
			5	GPTIM4_CH4
			Others	Reserved
R19	PB26	I/O	0	GPIO_B26
			1	UART5_RTS
			2	SPI3_CS
			5	GPTIM5_CH1
			8	#DCTEST0
			Others	Reserved
R20	PB27	I/O	0	GPIO_B27
			2	SPI4_CLK
			3	I2S3_SDI
			5	GPTIM5_CH2
			8	#DCTEST1
			Others	Reserved
R21	PB28	I/O	0	GPIO_B28
			1	I2C6_SCL
			2	UART6_RXD
			8	#LPCOMP1_P
			Others	Reserved
T20	PB29	I/O	0	GPIO_B29
			1	I2C6_SDA
			2	UART6_TXD
			8	#LPCOMP1_N
			Others	Reserved
P20	PB30	I/O	0	GPIO_B30
			2	SPI4_DO
			3	I2S3_BCK
			4	SPI4_DIO
			5	GPTIM5_CH3
			8	#LPCOMP2_P
			Others	Reserved
P21	PB31	I/O	0	GPIO_B31
			2	SPI4_DI
			3	I2S3_LRCK
			4	AUD_CLK_EXT
			5	GPTIM5_CH4
			8	#LPCOMP2_N
			Others	Reserved
N19	PB32	I/O	0	GPIO_B32
			8	#GPADC_CH0
			Others	Reserved

Continued on the next page

Table 5-3: GPIO (PB) Pin List (continued)

Pin Number SF32LB58x (BGA256)	Pin Name	Type	Sel #	Function
H16	PB33	I/O	0	GPIO_B33
			5	LPTIM3_ETR
			8	#GPADC_CH1
			Others	Reserved
N20	PB34	I/O	0	GPIO_B34
			2	SPI4_CS
			3	I2S3_MCLK
			8	#GPADC_CH2
			Others	Reserved
L17	PB35	I/O	0	GPIO_B35
			8	#GPADC_CH3
			Others	Reserved
G16	PB36	I/O	0	GPIO_B36
			1	UART4_RXD
			5	GPTIM3_CH1
			8	#GPADC_CH4
			Others	Reserved
F16	PB37	I/O	0	GPIO_B37
			1	UART4_TXD
			5	GPTIM3_CH2
			8	#GPADC_CH5
			Others	Reserved
K17	PB38	I/O	0	GPIO_B38
			2	UART6_CTS
			5	GPTIM3_CH3
			8	#GPADC_CH6
			Others	Reserved
M18	PB39	I/O	0	GPIO_B39
			2	UART6_RTS
			5	GPTIM3_CH4
			8	#GPADC_CH7
			Others	Reserved
L18	PB40	I/O	0	GPIO_B40
			3	SPI3_CS
			5	GPTIM3_ETR
			8	#SDADC_CH0
			Others	Reserved
H17	PB41	I/O	0	GPIO_B41
			2	WLAN_ACTIVE
			4	I2S3_SDO
			5	GPTIM4_CH1
			8	#SDADC_CH1
			Others	Reserved

Continued on the next page

Table 5-3: GPIO (PB) Pin List (continued)

Pin Number SF32LB58x (BGA256)	Pin Name	Type	Sel #	Function
M20	PB42	I/O	0	GPIO_B42
			4	I2S3_SDI
			5	GPTIM4_CH2
			8	#SDADC_CH2
			Others	Reserved
M21	PB43	I/O	0	GPIO_B43
			2	UART4_CTS
			3	UART5_CTS
			4	I2S3_BCK
			5	GPTIM4_CH3
			8	#SDADC_CH3
			Others	Reserved
A19	PB44	I/O	0	GPIO_B44
			2	UART4_RTS
			3	UART5_RTS
			4	I2S3_LRCK
			5	GPTIM4_CH4
			8	#ACTEST0
			Others	Reserved
A20	PB45	I/O	0	GPIO_B45
			2	BT_ACTIVE
			5	GPTIM4_ETR
			8	#ACTEST1
			Others	Reserved
B19	PB46	I/O	0	GPIO_B46
			3	AUD_CLK_EXT
			4	I2S3_MCLK
			5	GPTIM5_CH1
			Others	Reserved
B16	PB47	I/O	0	GPIO_B47
			1	I2C5_SDA
			2	UART6_RXD
			5	GPTIM5_CH2
			Others	Reserved
C17	PB48	I/O	0	GPIO_B48
			1	I2C5_SCL
			2	UART6_TXD
			5	GPTIM5_CH3
			Others	Reserved
C19	PB49	I/O	0	GPIO_B49
			2	UART6_CTS
			3	UART6_RXD
			5	GPTIM5_CH4
			Others	Reserved

Continued on the next page

Table 5-3: GPIO (PB) Pin List (continued)

Pin Number SF32LB58x (BGA256)	Pin Name	Type	Sel #	Function
D19	PB50	I/O	0	GPIO_B50
			2	UART6_RTS
			3	UART6_TXD
			5	GPTIM5_ETR
			Others	Reserved
D18	PB51	I/O	0	GPIO_B51
			1	PMIC_SDA
			2	UART4_CTS
			3	UART5_CTS
			5	LPCOMP1_OUT
			Others	Reserved
D17	PB52	I/O	0	GPIO_B52
			1	PMIC_SCLK
			2	UART4_RTS
			3	UART5_RTS
			5	LPCOMP2_OUT
			Others	Reserved
B15	PB53	I/O	0	GPIO_B53
			Others	Reserved
C14	PB54	I/O	0	GPIO_B54
			8	#WKUP_PIN0
			Others	Reserved
C15	PB55	I/O	0	GPIO_B55
			8	#WKUP_PIN1
			Others	Reserved
D16	PB56	I/O	0	GPIO_B56
			2	UART4_CTS
			3	SPI3_CLK
			8	#WKUP_PIN2
			Others	Reserved
D14	PB57	I/O	0	GPIO_B57
			2	UART4_RTS
			3	SPI3_DO
			4	SPI3_DIO
			8	#WKUP_PIN3
			Others	Reserved
D15	PB58	I/O	0	GPIO_B58
			2	UART6_RXD
			3	SPI3_DI
			8	#WKUP_PIN4
			Others	Reserved
E15	PB59	I/O	0	GPIO_B59
			2	UART6_TXD
			3	SPI3_CS
			8	#WKUP_PIN5
			Others	Reserved

5.2.3 List of Dedicated Pins (Power, RF, Analog, I/O)

Table 5-4: List of Dedicated Pins (Power, RF, Analog, I/O)

Pin Number SF32LB58x (BGA256)	Pin Name	Type	Description
A15	PBR<0>	I/O	AON GPIO
B14	PBR<1>	I/O	AON GPIO
A14	PBR<2>	I/O	AON GPIO
B13	PBR<3>	I/O	AON GPIO
B12	PBR<4>	I/O	AON GPIO
A12	PBR<5>	I/O	AON GPIO
B2	PVDD_PMU1	PWR	Power input
B3	PVDD_PMU2	PWR	Power input
C2	PVSS_PMU1	GND	Power ground
C3	PVSS_PMU2	GND	Power ground
C1	PMU_BUCK1_VSW	A,I/O	Buck1 LX
D1	PMU_BUCK1_VOUT	PWR	Buck1 FB
B1	PMU_BUCK2_VOUT	PWR	Buck2 FB
A2	PMU_BUCK2_VSW	A,I/O	Buck2 LX
A3	VSS	GND	Power ground
A4	VSS	GND	Power ground
B4	VDD_EXT	PWR	Ext VDD input
B5	VDD_EXT	PWR	Ext VDD input
D2	HPSYS_LDO_VOUT	PWR	LDO ext Capacitor Point
C4	LPMU_VDD07_RET	PWR	LDO ext Capacitor Point
C5	LPMU_VDD11_RTC	PWR	LDO ext Capacitor Point
B7	XTAL32K_XI	A,I	XTAL IN
A6	XTAL32K_XO	A,O	XTAL OUT
A17	XTAL48M_XI	A,I	XTAL IN
A18	XTAL48M_XO	A,O	XTAL OUT
C21	BRF_ANT	A,I/O	RF ANT
E20	AVDD_BRF	PWR	RF power
B20	AVSS_RRF	GND	RF ground
B21	AVSS_RRF	GND	RF ground
D20	AVSS_TRF	GND	RF ground
D21	AVSS_TRF	GND	RF ground
C20	AVSS_VCO	GND	RF ground
E21	AVSS_TRF2	GND	RF ground
K18	AVDD33_ANA	PWR	Analog power input
J18	AVDD33_AUD	PWR	Audio power input
P5	AVDD33_USB	PWR	USB power input
P3	AVDD18_DSI	PWR	DSI power input
H6	VDDIOA	PWR	PA<12:93> power input
P12	VDDIOA2	PWR	PA<0:11> power input
E17	VDDIOB	PWR	PB/PBR power input
M2	VDDIOSA	PWR	SIPA power input
G1	VDDIOSB	PWR	SIPB power input
L14	VDDIOSC	PWR	SIPC power input
F20	MIC_BIAS	PWR	MIC power output
R6	USB2_DN	A,I/O	USB Negative IO
T6	USB2_DP	A,I/O	USB Positive IO
T5	USB2_REXT	A,O	

Continued on the next page

Table 5-4: List of Dedicated Pins (Power, RF, Analog, I/O) (continued)

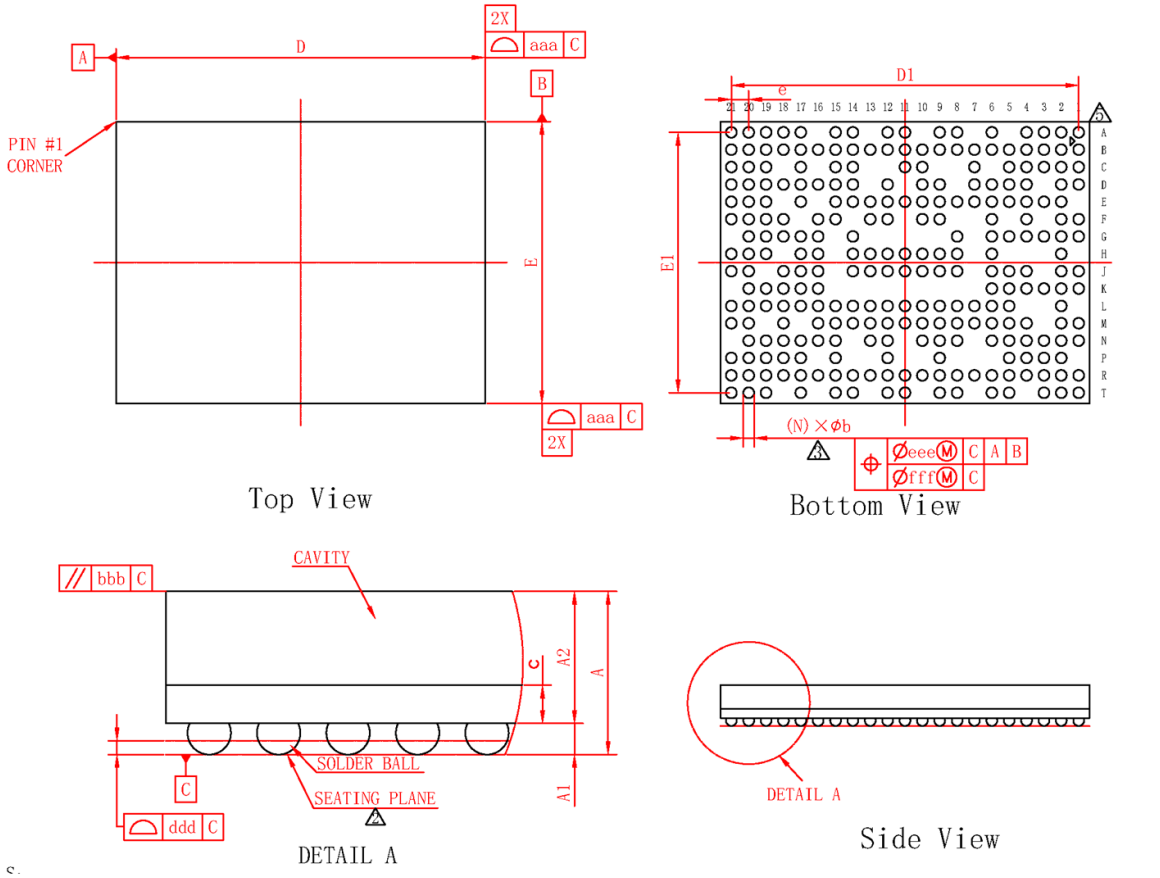
Pin Number SF32LB58x (BGA256)	Pin Name	Type	Description
D4	RSTN	I	ResetN input
E6	BOOT_MODE	I	Boot mode input
G18	ADC1N	A,I	ADC1 Negative input
G19	ADC1P	A,I	ADC1 Positive input
F18	ADC2N	A,I	ADC2 Negative input
F19	ADC2P	A,I	ADC2 Positive input
J21	DAC1N	A,O	DAC1 Negative output
J20	DAC1P	A,O	DAC1 Positive output
H20	DAC2N	A,O	DAC2 Negative output
H21	DAC2P	A,O	DAC2 Positive output
L20	GPADC_VREFN	GND	Ground
L21	GPADC_VREFP	A,I	GPADC Positive VREF input
L19	SDMADC_INPUT	A,I	SDMADC input
K19	SDMADC_VREF	A,I	SDMADC VREF input
K20	SDMADC_VSS_VREF	GND	Ground
B18	AVSS_BB	GND	RF Ground
B17	AVSS_CAU	GND	Ground
P2	AVSS_DSI	GND	Ground
J17	AVSS33_ANA	GND	Ground
G20	AVSS33_AUD	GND	Ground
F21	AUD_VREF	A,I	Audio VREF input
H19	AUD_VREF_GND	GND	Ground
T2	DSI_CLKN	A,I/O	DSI Negative clock output
T3	DSI_CLKP	A,I/O	DSI Positive clock output
R1	DSI_D0N	A,I/O	DSI Lane 0 Negative inout
R2	DSI_D0P	A,I/O	DSI Lane 0 Positive inout
R3	DSI_D1N	A,I/O	DSI Lane 1 Negative output
R4	DSI_D1P	A,I/O	DSI Lane 1 Positive output
P4	DSI_REXT	A,O	
T1	AVSS_DSI	GND	Ground
A1	VSS	GND	Ground
A21	VSS	GND	Ground
B6	VSS	GND	Ground
E19	VSS	GND	Ground
G3	VSS	GND	Ground
G8	VSS	GND	Ground
G17	VSS	GND	Ground
H8	VSS	GND	Ground
H9	VSS	GND	Ground
H10	VSS	GND	Ground
H11	VSS	GND	Ground
H12	VSS	GND	Ground
H13	VSS	GND	Ground
H14	VSS	GND	Ground
J8	VSS	GND	Ground
J9	VSS	GND	Ground
J10	VSS	GND	Ground
J11	VSS	GND	Ground
J12	VSS	GND	Ground
J13	VSS	GND	Ground

Continued on the next page

Table 5-4: List of Dedicated Pins (Power, RF, Analog, I/O) (continued)

Pin Number SF32LB58x (BGA256)	Pin Name	Type	Description
J14	VSS	GND	Ground
N2	VSS	GND	Ground
R5	VSS	GND	Ground
R7	VSS	GND	Ground
T21	VSS	GND	Ground

5.3 Package Dimensions



symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.840	0.940	1.040	0.033	0.037	0.041
A1	0.130	0.180	0.230	0.005	0.007	0.009
A2	0.710	0.760	0.810	0.028	0.030	0.032
c	0.180	0.220	0.260	0.007	0.009	0.010
D	8.400	8.500	8.600	0.331	0.335	0.339
E	6.400	6.500	6.600	0.252	0.256	0.260
D1	---	8.000	---	---	0.315	---
E1	---	6.000	---	---	0.236	---
e	---	0.400	---	---	0.016	---
b	0.200	0.250	0.300	0.008	0.010	0.012
aaa	0.100			0.004		
bbb	0.100			0.004		
ddd	0.080			0.003		
eee	0.150			0.006		
fff	0.050			0.002		
Ball Diam	0.250			0.010		
N	256			256		
MD/ME	21/16			21/16		

TECHNOLOGY SPECIFICATION[技术要求]

1. BALL PAD OPENING: 0.230mm; [球形防焊开口: 0.230mm;]
2. PRIMARY DATUM C AND SEATING PLANE ARE THE SOLDER BALLS;
   [主要基准C和底面是锡球;]
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C; [尺寸b是测量最大锡球直径, 平行于主要基准C;]
4. SPECIAL CHARACTERISTICS C CLASS: bbb, ddd; [特殊特性C类: bbb, ddd;]
5. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY;
   [PIN 1 标识仅供参考;]
6. BAN TO USE THE LEVEL 1 ENVIRONMENT-RELATED SUBSTANCES;
   [禁止使用一级环境管理物质;]

Figure 5-2: SF32LB58x (BGA256) Package Dimensions

5.4 Carrier Tape Dimensions

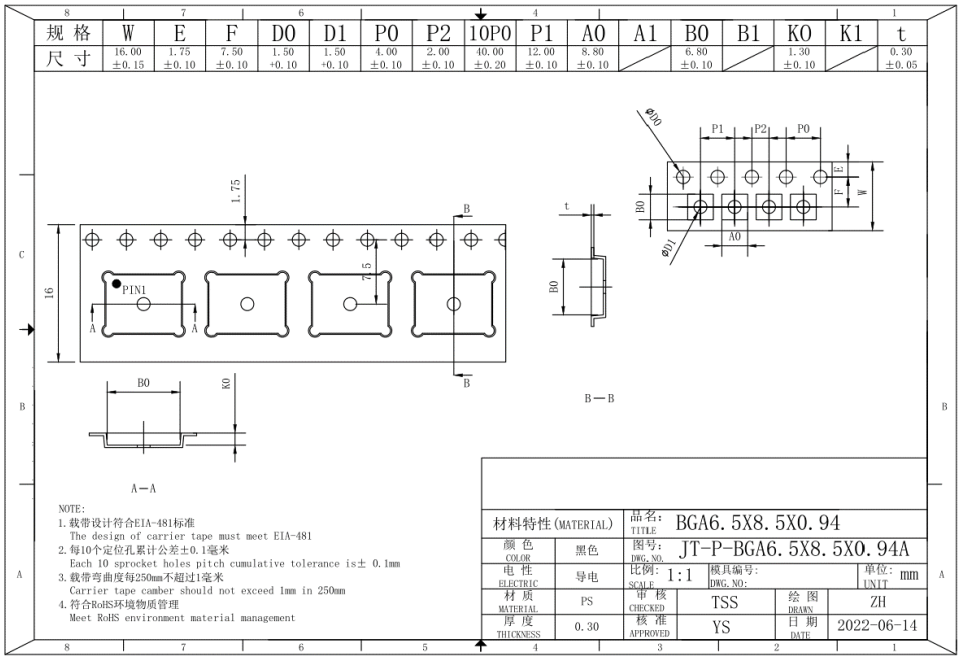
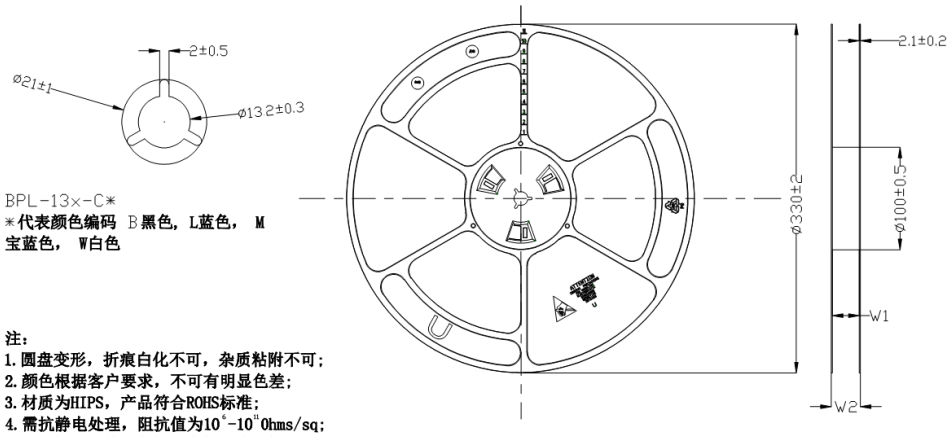


Figure 5-3: Carrier Tape Dimensions

5.5 Reel Dimensions



BPL-13x-C*
*代表颜色编码 B黑色，L蓝色， M宝蓝色， W白色

注：
1. 圆盘变形，折痕白化不可，杂质粘附不可；
2. 颜色根据客户要求，不可有明显色差；
3. 材质为HIPS，产品符合ROHS标准；
4. 需抗静电处理，阻抗值为10^{6}-10^{9}Ohms/sq；
5. 需用拉里针检测每批圆盘拉断力，标准＞10Kg

规 格	料 号	W1	W2
13*100*12mm	BPL-1312-C*	$12.5^{+1.5}_{-0}$	17.5±1
13*100*16mm	BPL-1316-C*	$16.5^{+1.5}_{-0}$	21.5±1
13*100*24mm	BPL-1324-C*	$24.5^{+1.5}_{-0}$	29.5±1

Figure 5-4: Reel Dimensions

5.6 Graded Reflow Soldering

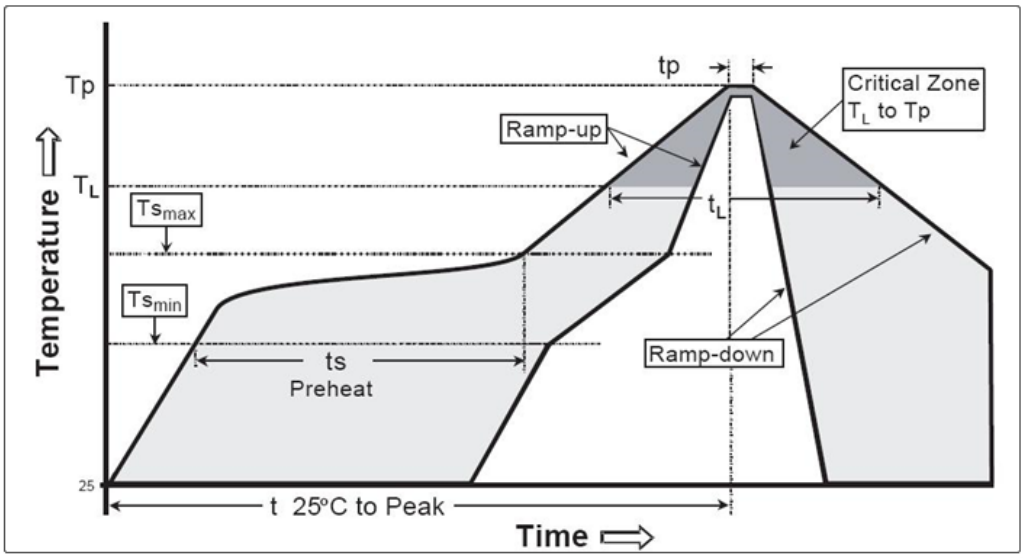


Figure 5-5: Graded Reflow Soldering

Table 5-5: Comparison Table of Graded Reflow Soldering

Item	Tin-lead Process	Lead-free Process
Average Ramp-up Rate (Ts_{max} to T_p)	Max. 3°C/s	Max. 3°C/s
Preheat Temperature Min.(Ts_{min}) Preheat Temperature Max. (Ts_{max}) Preheat Time (Ts_{min} to Ts_{max})	100°C 100°C 60-120s	150°C 200°C 60-180s
Temperature_Time Maintained above (T_L) Time_Time Maintained above (t_L)	183°C 60-150s	217°C 60-150s
Peak Temperature （T_p）	225+0/-5°C	240+0/-5°C
Time of Peak Temperature （tp）	10-30s	20-40s
Ramp-down Rate	Max. 6°C/s	Max. 6°C/s
Time_25°C to Peak Temperature (t)	Max. 6 mins	Max. 8 mins

Table 5-6: Peak Reflow Temperature – Lead-free

Packaging Thickness	Volume (mm^3) <350	Volume (mm^3) ≥350
<2.5mm	240 + 0/-5°C	225 + 0/-5°C
≥2.5mm	225 + 0/-5°C	225 + 0/-5°C

Table 5-7: Graded Reflow Temperature – Lead-free

Packaging Thickness	Volume (mm^3) <350	Volume (mm^3) 350-2000	Volume (mm^3) >2000
<1.6mm	260 + 0 °C	260 + 0 °C	260 + 0 °C
1.6mm –2.5mm	260 + 0 °C	250 + 0 °C	245 + 0 °C
≥2.5mm	250 + 0 °C	245 + 0 °C	245 + 0 °C

5.7 Ordering Information

Table 5-8: Ordering Information

Part No.	Package Size	SiP Specification	Pack Quantity (PCS)
SF32LB583VCC36	BGA256: 8.5×6.5×0.94mm-0.4	64Mb pSRAM + 8Mb Nor Flash	3000
SF32LB585V5E56	BGA256: 8.5×6.5×0.94mm-0.4	256Mb pSRAM + 64Mb Nor Flash	3000
SF32LB587VEE56	BGA256: 8.5×6.5×0.94mm-0.4	512Mb pSRAM + 32Mb Nor Flash	3000

Address: 5F, Building 12, 88 Daerwen Road, Pudong New Area, Shanghai 201203, P. R. China
Email: sales@sifli.com