思 澈 科 技

SF32LB52x

用户手册

V0.3（非正式发布）

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更新历史

文档状态说明

文档状态	版本范围	说明
草稿	0.0.0 ~0.9.9	初稿，非正式发布，信息为初步数据，反映量产前产品的规格与性能，不能保证准确性，随时可能更改，思澈科技将不会主动通知
发布版	1.0.0 ~1.9.9	正式发布，信息有可能还会小范围修正，以便更准确地反映量产产品的规格与性能；如有更改，思澈科技将不会主动通知

本文档更新历史

日期	版本	发布说明
2024-06-11	0.3	更新小核相关信息
2023-07-06	0.2	更正功耗数值，更新 AON 寄存器表和 DMA 章节内容
2023-06-15	0.1	初稿

产品概述

SF32LB52x 是一系列用于超低功耗人工智能物联网（AIoT）场景下的高集成度、高性能 MCU 芯片。芯片采用了基于 Arm Cortex-M33 STAR-MC1 处理器的大小核架构，集成高性能 2D/2.5D 图形引擎，双模蓝牙 5.3，以及音频 codec，可广泛用于腕带类可穿戴电子设备、智能移动终端、智能家居等各种应用场景。

芯片中大核性能处理器最高工作频率达 192MHz，单核性能达 787 CoreMark，支持动态频率功耗调节，功耗效率最高可达 4.8uA/CoreMark，在用于提供丰富应用和流畅人机交互所需的高性能算力的同时，还可作为 Sensor Hub 控制多种传感器以及运行蓝牙协议栈，从而很好地兼顾流畅人机交互所需的高计算性能与长待机时间所需的超低功耗运行之间的平衡关系。

芯片内集成 2D/2.5D GPU，主频最高达到 192MHz，支持双图层叠加，alpha 混叠，硬件加速的实时旋转和缩放，以及各种常用图形格式转换。支持硬件加速无损压缩图形解压缩，支持原生动画，可以大幅提高带宽利用率，降低存储成本。芯片内置 LCD 控制器，支持 8080/QSPI 等多种接口，可不依赖于 CPU 自主实现最高 60fps 的全屏刷新帧率，并支持低功耗息屏常显。

集成双模蓝牙 5.3 收发机，经典蓝牙 EDR2 模式最高发射功率 13dBm，接收峰值功耗低至 2.4mA@3.8V，低功耗蓝牙接收灵敏度达到-100dBm（1Mbps），经典蓝牙 EDR2 模式灵敏度-95.5dBm。集成高保真音频 ADC 和 DAC，支持蓝牙通话和连接耳机 MP3 播放。

功能框图

图 0-1: 功能框图

产品特性

CPU 与内存

- 性能处理器/大核（HCPU）
  - 处理器：Arm Cortex-M33 STAR-MC1
  - 主频：最高 192MHz，可调节
  - 单核最高 296 DMIPS，787 EEMBC CoreMark
  - I-Cache + D-Cache：32KB(2-way)+16KB(4-way)
  - SRAM：512KB（全部为 Retention SRAM）
  - CoreMark 功耗效率：低至 23uA/MHz @3.8V
  - 单精度浮点运算单元（FPU）
  - 内存保护单元（MPU）
- 超低功耗处理器/小核（LCPU）
  - 处理器：Arm Cortex-M33 STAR-MC1
  - 主频：最高 24MHz，可调节
  - SRAM：64KB（全部为 Retention SRAM）

无线连接

- 双模蓝牙 5.3，支持 BLE Audio
- 灵敏度：-100dBm（BLE/1Mbps），-96.3dBm（BR），-95.5dBm（EDR2）
- 最大发射功率：13dBm（EDR2/3），19dBm（BR/BLE）
- 接收机峰值功耗（BR）：2.4mA@3.8V

音频

- 1× 高保真 24-bit 音频 DAC
  - Noise floor: 3.7uVrms
  - SNR(with 10kohm load and A-Weighted): 109dB
  - Dynamic Range: 109dB
  - Sample rate: 8k/ 16k/ 11.025k/ 22.05k/ 24k/ 32k/ 44.1k/ 48kHz
  - 支持 192 级数字音量，具有过零检测功能
- 1× 高保真 24-bit 音频 ADC
  - SNR(A-Weighted): 99dB, Dynamic Range: 99dB
  - Sample rate: 8k/ 11.025k/ 12k/ 16k/ 22.05k/ 24k/ 32k/ 44.1k/ 48kHz
  - 数字高通滤波器可用于消除 ADC 的直流偏置
  - 支持单端和全差分输入麦克风
  - Micbias LDO，输出电压为 1.4V~2.8V，输出电流为 0~2mA

图形显示

- 2D/2.5D 图形引擎—ePicasso™2.0
  - 支持硬件加速的旋转、缩放和镜像
  - 最大解析度 512×512
  - 支持 aRGB8565，aRGB8888，L8，A8/4/2，YUV，支持 alpha 混叠
- 无损解压缩加速器—eZip™2.0
  - 硬件无损图形解压缩
  - 支持 eZip-A 原生无损动画
  - 支持与 ePicasso™2.0 联动，无须中间缓存
- LCD 控制器
  - 支持 8080，SPI，Dual-SPI，Quad-SPI
  - 支持单图层与纯色背景图层的 alpha 混叠
  - 独立 LCD 控制器，支持息屏常显模式

存储接口

- 支持合封（SiP）OPI-PSRAM，接口最高频率 144MHz
- 1×MPI(QSPI)，支持 NOR、NAND、QPI-PSRAM
- 1×SD/SDIO，支持 SD3.0，SDIO3.0，eMMC

其它

- DMA
  - 通用 DMA：用于与外设间高效率数据搬运
  - extDMA：用于与外部存储间高效率数据搬运
- 安全
  - AES 加速器
  - HASH 加速器
  - CRC 加速器
  - 真随机数发生器（TRNG）
  - PSA Certified Level 1 认证
- 定时器
  - 2×16b GPTIM，2×32b BTIM，1×32b ATIM，2×24b LPTIM
  - 1×RTC
  - 2× 看门狗 24b WDT，1× 独立看门狗 IWDT
- 模拟
  - 1×12-bit 通用 SAR ADC，共 8 通道
  - 1× 片上温度传感器
  - 1×24-bit 音频 ADC，1×24-bit 音频 DAC
- 连接外设
  - 最多 45 个 GPIO
  - 3×UART，4× I^2C，2×SPI
  - 1× I^2S，1× PDM
  - 1×USB2.0 FS
  - 外设任务控制器（PTC）
- 电源管理
  - 内置高效率 Buck 及低功耗 LDO

- 提供两路对外 3.3V 供电，最大电流 150mA×2
- 休眠功耗：2uA
- 内置 560mA 锂电池线性充电器，支持 4.2V-4.45V 满电电压
- VBAT 电压范围：3.2V-4.7V
- VBUS 电压范围：4.6V-5.5V

封装

- QFN68L，45 个 GPIO，7mm×7mm×0.85mm

应用场景

智能穿戴

- 高端智能手表
- 智能手环
- 可穿戴医疗器材
- 健身器材

工业

- 高性价比显示方案
- 图形化人机交互设备
- 工业传感器控制中心
- 工业设备监测
- 工业仪器仪表

车载

- 电动车中控设备
- 汽车钥匙
- 穿戴式汽车遥控设备

家庭自动化

- 中小型智能家电
- 智能门锁

通用

- 低功耗传感器中心
- 蓝牙 mesh

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1 芯片总览

1.1 系统架构

SF32LB52x 是一系列用于超低功耗人工智能物联网（AIoT）场景下的高集成度、高性能 MCU 芯片。芯片采用了基于 Arm Cortex-M33 STAR-MC1 处理器的大小核架构，其中：

- 性能处理器/大核（HCPU）：配备 32KB 指令缓存（I-Cache）和 16KB 数据缓存（D-Cache），512KB SRAM（全部为 Retention SRAM）。最高主频 192MHz，可动态切换 D 挡和 S 挡，高效访问片内和片外存储。作为系统主控，S 挡主要用于系统控制、人机交互、高性能计算等；同时作为低功耗传感器中心，D 挡可用于低功耗场景下的各种数据采集和处理。
- 超低功耗处理器/小核（LCPU）：最高主频 24MHz，64KB SRAM（全部为 Retention SRAM），用于低功耗蓝牙的传输控制和基本数据处理。

1.2 Cortex-M33 STAR-MC1 “星辰”处理器

Cortex-M33 STAR-MC1 处理器是安谋中国（Arm China）推出的“星辰”系列产品的第一款处理器，该处理器继承了 Cortex-M33 的主要特点，支持现有的 Arm v8-M 架构的全部功能，具有有序（in order）三级流水线，可显著降低系统功耗，具有部分双发射 16 位指令能力，并进一步改进了协处理器接口，增加了对缓存（Cache）的支持。

Cortex-M33 STAR-MC1 性能达到 1.5DMIPS/MHz 和 4.02Coremark/MHz，与上一代同档位 Arm 处理器相比，在相同主频下，Cortex-M33 STAR-MC1 的性能提升 20%。

Cortex-M33 STAR-MC1 提供了协处理器（Coprocessor）接口，以便根据不同场景需求进一步提高定制计算的能力。通过 MCR（Move from Coprocessor to Register）和 MRC（Move from Register to Coprocessor）指令，可以在 Cortex-M33 STAR-MC1 和协处理器之间转移寄存器数据和计算结果数据，非常适合所需数据量不大、计算复杂但相对碎片化、延迟较小的运算。在协处理器计算的同时，Cortex-M33 STAR-MC1 处理器仍然可以并行执行其它指令，从而明显提高执行效率。

此外，该处理器还支持数字信号处理（DSP）指令集和浮点数运算单元（FPU）。

Cortex-M33 STAR-MC1 引入了紧耦合内存（TCM）和缓存（Cache）技术，增强了各种不同特点的内置和外置存储系统的使用灵活性，确保在各种不同场景下处理器响应的实时性和计算效率。

1.3 性能处理器（大核）系统（HPSYS）

1.3.1 总线架构

HPSYS 内部提供了基于 AHB 协议的总线矩阵，支持多个主设备并行访问多个从设备地址空间。

如图1-1所示，总线主设备位于上侧，从设备地址空间位于右侧，交叉处的黑色圆点代表总线连通。

HCPU 与 DMAC1 能够访问 HPSYS 的所有地址空间。

DTCM 与 HPSYS_RAM0 共享 128KB 地址空间，可由 HCPU 及其它主设备访问。

HP_PERI 包含 APB 相关外设以及 AHB 相关外设，可由 HCPU、DMAC1 以及 PTC1 访问。

多个主设备同时访问同一个从设备地址空间时，基于轮询仲裁原则决定访问次序。

图中边框不相连的多个主设备同时访问不同从设备地址空间时，互相不受影响。边框相连的两个主设备同时发起访问时，基于固定优先级或轮询仲裁原则决定访问次序。

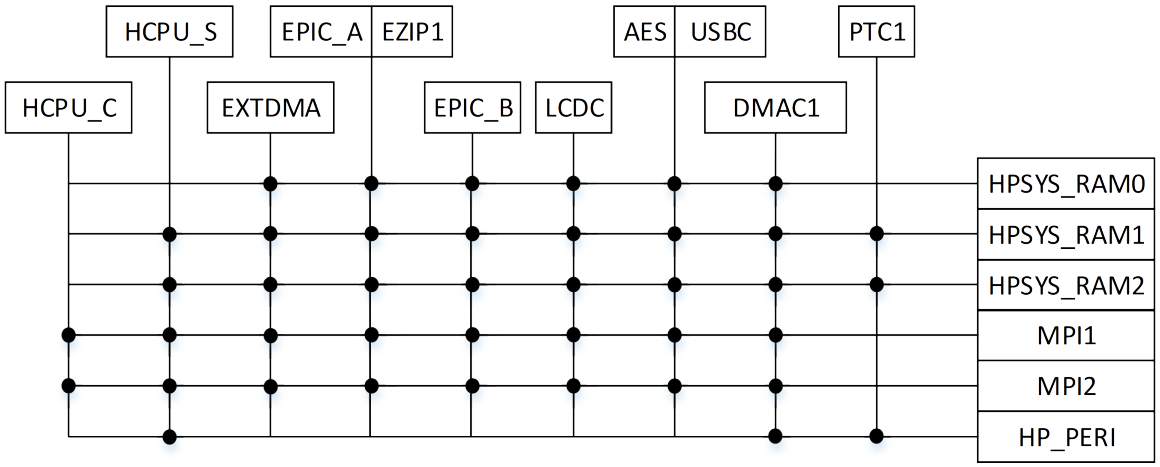

图 1-1: 性能处理器（大核）系统总线架构

1.3.2 存储器类型

1.3.2.1 Cache

HCPU 配置有 32KB 2-way I-Cache（一级指令缓存）和 16KB 4-way D-Cache（一级数据缓存），可大幅提升 XIP 时 CPU 执行效率。软件需合理配置 MPU（Memory Protection Unit）设置 cache 地址段和非 cache 地址段，兼顾效率和易用性。

1.3.2.2 TCM

HCPU 配置有 128KB zero-wait-cycle D-TCM，地址空间为 0x2000_0000-0x2001_FFFF，可用于放置对实时性要求较高的代码和数据。该 TCM memory 挂在总线上，可以被其他 AHB master 访问。

1.3.2.3 SRAM

HPSYS 总线上共有 512KB SRAM，其中包括：

- 0x2000_0000-0x2001_FFFF，128KB zero-wait-cycle SRAM（与 D-TCM 共享），所有 AHB master 均可访问，最高频率为 192MHz。
- 0x2002_0000-0x2007_FFFF，384KB zero-wait-cycle SRAM，所有 AHB master 均可访问，最高频率为 192MHz。

1.3.2.4 片外 RAM

HPSYS 支持合封四线和八线 pSRAM，地址空间为 0x6000_0000-0x61FF_FFFF，实际可访问地址由外挂颗粒容量决定。接口最高频率为 DDR 144MHz，数据位宽为 8-bit。

1.3.2.5 片外 Flash

HPSYS 支持外挂 NOR/NAND FLASH，其中：

- 0x6000_0000-0x61FF_FFFF 地址段可挂合封 FLASH，推荐使用频率为 96MHz
- 0x6200_0000-0x9FFF_FFFF 地址段可挂外置 FLASH，推荐使用频率为 60MHz

1.3.3 地址映射

表 1-1: HPSYS 地址映射

Category	Memory /IP	Address Space	HCPU				LCPU	
			Starting Address		Ending Address		Starting Address	Ending Address
HPSYS_ITCM		**64KB**	**0x0000_0000**		**0x0000_FFFF**		**NA**	**NA**
	ROM	64KB	0x0000_0000		0x0000_FFFF		-	-
	Reserved	-	-		-		-	-
External Memory		**1024MB**	**0x1000_0000**	**0x6000_0000**	**0x1FFF_FFFF**	**0x9FFF_FFFF**	**0x6000_0000**	**0x9FFF_FFFF**
	MPI1 Memory	32MB	0x1000_0000	0x6000_0000	0x11FF_FFFF	0x61FF_FFFF	0x6000_0000	0x61FF_FFFF
	MPI2 Memory	224MB/992MB	0x1200_0000	0x6200_0000	0x1FFF_FFFF	0x9FFF_FFFF	0x6200_0000	0x9FFF_FFFF
HPSYS_RAM		**512KB**	**0x2000_0000**		**0x2007_FFFF**		**0x2A00_0000**	**0x2A07_FFFF**
	RAM0 (DTCM)	128KB	0x2000_0000		0x2001_FFFF		0x2A00_0000	0x2A01_FFFF
	RAM1	128KB	0x2002_0000		0x2003_FFFF		0x2A02_0000	0x2A03_FFFF
	RAM2	256KB	0x2004_0000		0x2007_FFFF		0x2A04_0000	0x2A07_FFFF
HPSYS_APB1		**256KB**	**0x5000_0000**		**0x5003_FFFF**		**0x5000_0000**	**0x5003_FFFF**
	RCC1	4KB	0x5000_0000		0x5000_0FFF		0x5000_0000	0x5000_0FFF
	ADMA	4KB	0x5000_1000		0x5000_1FFF		0x5000_1000	0x5000_1FFF
	SECU1	4KB	0x5000_2000		0x5000_2FFF		0x5000_2000	0x5000_2FFF
	PINMUX1	4KB	0x5000_3000		0x5000_3FFF		0x5000_3000	0x5000_3FFF
	ATIM1	4KB	0x5000_4000		0x5000_4FFF		0x5000_4000	0x5000_4FFF
	AUDPRC	4KB	0x5000_5000		0x5000_5FFF		0x5000_5000	0x5000_5FFF
	EZIP1	4KB	0x5000_6000		0x5000_6FFF		0x5000_6000	0x5000_6FFF
	EPIC	4KB	0x5000_7000		0x5000_7FFF		0x5000_7000	0x5000_7FFF
	LCDC1	4KB	0x5000_8000		0x5000_8FFF		0x5000_8000	0x5000_8FFF
	I2S1	4KB	0x5000_9000		0x5000_9FFF		0x5000_9000	0x5000_9FFF
	Reserved	4KB	0x5000_A000		0x5000_AFFF		0x5000_A000	0x5000_AFFF
	SYSCFG1	4KB	0x5000_B000		0x5000_BFFF		0x5000_B000	0x5000_BFFF
	EFUSEC	4KB	0x5000_C000		0x5000_CFFF		0x5000_C000	0x5000_CFFF
	AES	4KB	0x5000_D000		0x5000_DFFF		0x5000_D000	0x5000_DFFF
	Reserved	4KB	0x5000_E000		0x5000_EFFF		0x5000_E000	0x5000_EFFF
	TRNG	4KB	0x5000_F000		0x5000_FFFF		0x5000_F000	0x5000_FFFF
	Reserved	4KB	0x5001_0000		0x5001_0FFF		0x5001_0000	0x5001_0FFF
	Reserved	4KB	0x5001_1000		0x5001_1FFF		0x5001_1000	0x5001_1FFF
	Reserved	4KB	0x5001_2000		0x5001_2FFF		0x5001_2000	0x5001_2FFF
	Reserved	4KB	0x5001_3000		0x5001_3FFF		0x5001_3000	0x5001_3FFF
	Reserved	4KB	0x5001_4000		0x5001_4FFF		0x5001_4000	0x5001_4FFF
	Reserved	4KB	0x5001_5000		0x5001_5FFF		0x5001_5000	0x5001_5FFF
	Reserved	4KB	0x5001_6000		0x5001_6FFF		0x5001_6000	0x5001_6FFF
	Reserved	4KB	0x5001_7000		0x5001_7FFF		0x5001_7000	0x5001_7FFF
	Reserved	4KB	0x5001_8000		0x5001_8FFF		0x5001_8000	0x5001_8FFF
	Reserved	4KB	0x5001_9000		0x5001_9FFF		0x5001_9000	0x5001_9FFF
	Reserved	4KB	0x5001_A000		0x5001_AFFF		0x5001_A000	0x5001_AFFF
	Reserved	4KB	0x5001_B000		0x5001_BFFF		0x5001_B000	0x5001_BFFF
	Reserved	4KB	0x5001_C000		0x5001_CFFF		0x5001_C000	0x5001_CFFF
	Reserved	4KB	0x5001_D000		0x5001_DFFF		0x5001_D000	0x5001_DFFF
	Reserved	4KB	0x5001_E000		0x5001_EFFF		0x5001_E000	0x5001_EFFF
	Reserved	4KB	0x5001_F000		0x5001_FFFF		0x5001_F000	0x5001_FFFF
	Reserved	128KB	0x5002_0000		0x5003_FFFF		0x5002_0000	0x5003_FFFF
HPSYS_AHB1		**256KB**	**0x5004_0000**		**0x5007_FFFF**		**0x5004_0000**	**0x5007_FFFF**
	Reserved	4KB	0x5004_0000		0x5004_0FFF		0x5004_0000	0x5004_0FFF
	MPI1	4KB	0x5004_1000		0x5004_1FFF		0x5004_1000	0x5004_1FFF

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表 1-1: HPSYS 地址映射（续）

Category	Memory /IP	Address Space	HCPU		LCPU	
			Starting Address	Ending Address	Starting Address	Ending Address
	MPI2	4KB	0x5004_2000	0x5004_2FFF	0x5004_2000	0x5004_2FFF
	Reserved	4KB	0x5004_3000	0x5004_3FFF	0x5004_3000	0x5004_3FFF
	Reserved	4KB	0x5004_4000	0x5004_4FFF	0x5004_4000	0x5004_4FFF
	SDMMC1	4KB	0x5004_5000	0x5004_5FFF	0x5004_5000	0x5004_5FFF
	Reserved	4KB	0x5004_6000	0x5004_6FFF	0x5004_6000	0x5004_6FFF
	USBC	4KB	0x5004_7000	0x5004_7FFF	0x5004_7000	0x5004_7FFF
	CRC1	4KB	0x5004_8000	0x5004_8FFF	0x5004_8000	0x5004_8FFF
	Reserved	28KB	0x5004_9000	0x5004_FFFF	0x5004_9000	0x5004_FFFF
	GFX_RAM	64KB	0x5005_0000	0x5005_FFFF	0x5005_0000	0x5005_FFFF
	Reserved	128KB	0x5006_0000	0x5007_FFFF	0x5006_0000	0x5007_FFFF
HPSYS_APB2		**128KB**	**0x5008_0000**	**0x5009_FFFF**	**0x5008_0000**	**0x5009_FFFF**
	PTC1	4KB	0x5008_0000	0x5008_0FFF	0x5008_0000	0x5008_0FFF
	DMAC1	4KB	0x5008_1000	0x5008_1FFF	0x5008_1000	0x5008_1FFF
	MAILBOX1	4KB	0x5008_2000	0x5008_2FFF	0x5008_2000	0x5008_2FFF
	Reserved	4KB	0x5008_3000	0x5008_3FFF	0x5008_3000	0x5008_3FFF
	USART1	4KB	0x5008_4000	0x5008_4FFF	0x5008_4000	0x5008_4FFF
	USART2	4KB	0x5008_5000	0x5008_5FFF	0x5008_5000	0x5008_5FFF
	USART3	4KB	0x5008_6000	0x5008_6FFF	0x5008_6000	0x5008_6FFF
	GPADC	4KB	0x5008_7000	0x5008_7FFF	0x5008_7000	0x5008_7FFF
	AUDCODEC	4KB	0x5008_8000	0x5008_8FFF	0x5008_8000	0x5008_8FFF
	TSEN	4KB	0x5008_9000	0x5008_9FFF	0x5008_9000	0x5008_9FFF
	Reserved	4KB	0x5008_A000	0x5008_AFFF	0x5008_A000	0x5008_AFFF
	Reserved	4KB	0x5008_B000	0x5008_BFFF	0x5008_B000	0x5008_BFFF
	Reserved	4KB	0x5008_C000	0x5008_CFFF	0x5008_C000	0x5008_CFFF
	Reserved	4KB	0x5008_D000	0x5008_DFFF	0x5008_D000	0x5008_DFFF
	Reserved	4KB	0x5008_E000	0x5008_EFFF	0x5008_E000	0x5008_EFFF
	Reserved	4KB	0x5008_F000	0x5008_FFFF	0x5008_F000	0x5008_FFFF
	GPTIM1	4KB	0x5009_0000	0x5009_0FFF	0x5009_0000	0x5009_0FFF
	Reserved	4KB	0x5009_1000	0x5009_1FFF	0x5009_1000	0x5009_1FFF
	BTIM1	4KB	0x5009_2000	0x5009_2FFF	0x5009_2000	0x5009_2FFF
	Reserved	4KB	0x5009_3000	0x5009_3FFF	0x5009_3000	0x5009_3FFF
	WDT1	4KB	0x5009_4000	0x5009_4FFF	0x5009_4000	0x5009_4FFF
	SPI1	4KB	0x5009_5000	0x5009_5FFF	0x5009_5000	0x5009_5FFF
	SPI2	4KB	0x5009_6000	0x5009_6FFF	0x5009_6000	0x5009_6FFF
	Reserved	4KB	0x5009_7000	0x5009_7FFF	0x5009_7000	0x5009_7FFF
	Reserved	4KB	0x5009_8000	0x5009_8FFF	0x5009_8000	0x5009_8FFF
	Reserved	4KB	0x5009_9000	0x5009_9FFF	0x5009_9000	0x5009_9FFF
	PDM1	4KB	0x5009_A000	0x5009_AFFF	0x5009_A000	0x5009_AFFF
	Reserved	4KB	0x5009_B000	0x5009_BFFF	0x5009_B000	0x5009_BFFF
	I2C1	4KB	0x5009_C000	0x5009_CFFF	0x5009_C000	0x5009_CFFF
	I2C2	4KB	0x5009_D000	0x5009_DFFF	0x5009_D000	0x5009_DFFF
	I2C3	4KB	0x5009_E000	0x5009_EFFF	0x5009_E000	0x5009_EFFF
	I2C4	4KB	0x5009_F000	0x5009_FFFF	0x5009_F000	0x5009_FFFF
HPSYS_AHB2		**64KB**	**0x500A_0000**	**0x500A_FFFF**	**0x500A_0000**	**0x500A_FFFF**
	GPIO1	4KB	0x500A_0000	0x500A_0FFF	0x500A_0000	0x500A_0FFF
	Reserved	60KB	0x500A_1000	0x500A_FFFF	0x500A_1000	0x500A_FFFF
HPSYS_APB3		**64KB**	**0x500B_0000**	**0x500B_FFFF**	**0x500B_0000**	**0x500B_FFFF**
	GPTIM2	4KB	0x500B_0000	0x500B_0FFF	0x500B_0000	0x500B_0FFF
	BTIM2	4KB	0x500B_1000	0x500B_1FFF	0x500B_1000	0x500B_1FFF
	Reserved	56KB	0x500B_2000	0x500B_FFFF	0x500B_2000	0x500B_FFFF
HPSYS_APB4		**256KB**	**0x500C_0000**	**0x500F_FFFF**	**0x500C_0000**	**0x500F_FFFF**
	HPSYS_AON	4KB	0x500C_0000	0x500C_0FFF	0x500C_0000	0x500C_0FFF
	LPTIM1	4KB	0x500C_1000	0x500C_1FFF	0x500C_1000	0x500C_1FFF
	LPTIM2	4KB	0x500C_2000	0x500C_2FFF	0x500C_2000	0x500C_2FFF
	Reserved	4KB	0x500C_3000	0x500C_3FFF	0x500C_3000	0x500C_3FFF
	Reserved	24KB	0x500C_4000	0x500C_9FFF	0x500C_4000	0x500C_9FFF
	PMUC	4KB	0x500C_A000	0x500C_AFFF	0x500C_A000	0x500C_AFFF
	RTC	4KB	0x500C_B000	0x500C_BFFF	0x500C_B000	0x500C_BFFF
	IWDT	4KB	0x500C_C000	0x500C_CFFF	0x500C_C000	0x500C_CFFF
	Reserved	12KB	0x500C_D000	0x500C_FFFF	0x500C_D000	0x500C_FFFF
	Reserved	64KB	0x500D_0000	0x500D_FFFF	0x500D_0000	0x500D_FFFF
	Reserved	64KB	0x500E_0000	0x500E_FFFF	0x500E_0000	0x500E_FFFF
	EUROPA	4KB	0x500F_0000	0x500F_0FFF	0x500F_0000	0x500F_0FFF
	Reserved	60KB	0x500F_1000	0x500F_FFFF	0x500F_1000	0x500F_FFFF

1.3.4 中断列表

表 1-2: HCPU 中断列表

IRQ #	IRQ Source
NMI	WDT1
IRQ[0]	AON

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表 1-2: HCPU 中断列表（续）

IRQ #	IRQ Source
IRQ[1]	LCPU_IRQ[1]
IRQ[2]	LCPU_IRQ[2]
IRQ[3]	LCPU_IRQ[3]
IRQ[4]	LCPU_IRQ[4]
IRQ[5]	LCPU_IRQ[5]
IRQ[6]	LCPU_IRQ[6]
IRQ[7]	LCPU_IRQ[7]
IRQ[8]	LCPU_IRQ[8]
IRQ[9]	LCPU_IRQ[9]
IRQ[10]	LCPU_IRQ[10]
IRQ[11]	LCPU_IRQ[11]
IRQ[12]	LCPU_IRQ[12]
IRQ[13]	LCPU_IRQ[13]
IRQ[14]	LCPU_IRQ[14]
IRQ[15]	LCPU_IRQ[15]
IRQ[16]	LCPU_IRQ[16]
IRQ[17]	LCPU_IRQ[17]
IRQ[18]	LCPU_IRQ[18]
IRQ[19]	LCPU_IRQ[19]
IRQ[20]	LCPU_IRQ[20]
IRQ[21]	LCPU_IRQ[21]
IRQ[22]	LCPU_IRQ[22]
IRQ[23]	LCPU_IRQ[23]
IRQ[24]	rsvd
IRQ[25]	rsvd
IRQ[26]	rsvd
IRQ[27]	rsvd
IRQ[28]	rsvd
IRQ[29]	rsvd
IRQ[30]	rsvd
IRQ[31]	rsvd
IRQ[32]	rsvd
IRQ[33]	rsvd
IRQ[34]	rsvd
IRQ[35]	rsvd
IRQ[36]	rsvd
IRQ[37]	rsvd
IRQ[38]	rsvd
IRQ[39]	rsvd
IRQ[40]	rsvd
IRQ[41]	rsvd
IRQ[42]	rsvd
IRQ[43]	rsvd
IRQ[44]	rsvd
IRQ[45]	rsvd
IRQ[46]	LPTIM1
IRQ[47]	LPTIM2
IRQ[48]	PMUC

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表 1-2: HCPU 中断列表（续）

IRQ #	IRQ Source
IRQ[49]	RTC
IRQ[50]	DMAC1_CH1
IRQ[51]	DMAC1_CH2
IRQ[52]	DMAC1_CH3
IRQ[53]	DMAC1_CH4
IRQ[54]	DMAC1_CH5
IRQ[55]	DMAC1_CH6
IRQ[56]	DMAC1_CH7
IRQ[57]	DMAC1_CH8
IRQ[58]	MAILBOX2_CH1
IRQ[59]	USART1
IRQ[60]	SPI1
IRQ[61]	I2C1
IRQ[62]	EPIC
IRQ[63]	LCDC1
IRQ[64]	I2S1
IRQ[65]	GPADC
IRQ[66]	EFUSEC
IRQ[67]	AES
IRQ[68]	PTC1
IRQ[69]	TRNG
IRQ[70]	GPTIM1
IRQ[71]	GPTIM2
IRQ[72]	BTIM1
IRQ[73]	BTIM2
IRQ[74]	USART2
IRQ[75]	SPI2
IRQ[76]	I2C2
IRQ[77]	EXTDMA
IRQ[78]	I2C4
IRQ[79]	SDMMC1
IRQ[80]	MAILBOX2_CH2
IRQ[81]	rsvd
IRQ[82]	PDM1
IRQ[83]	rsvd
IRQ[84]	GPIO1
IRQ[85]	MPI1
IRQ[86]	MPI2
IRQ[87]	rsvd
IRQ[88]	rsvd
IRQ[89]	EZIP1
IRQ[90]	AUDPRC
IRQ[91]	TSEN
IRQ[92]	USBC
IRQ[93]	I2C3
IRQ[94]	ATIM1
IRQ[95]	USART3
IRQ[96]	AUD_HP

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表 1-2: HCPU 中断列表（续）

IRQ #	IRQ Source
IRQ[97]	rsvd
IRQ[98]	SECU1
IRQ[99]	rsvd

1.4 电源管理

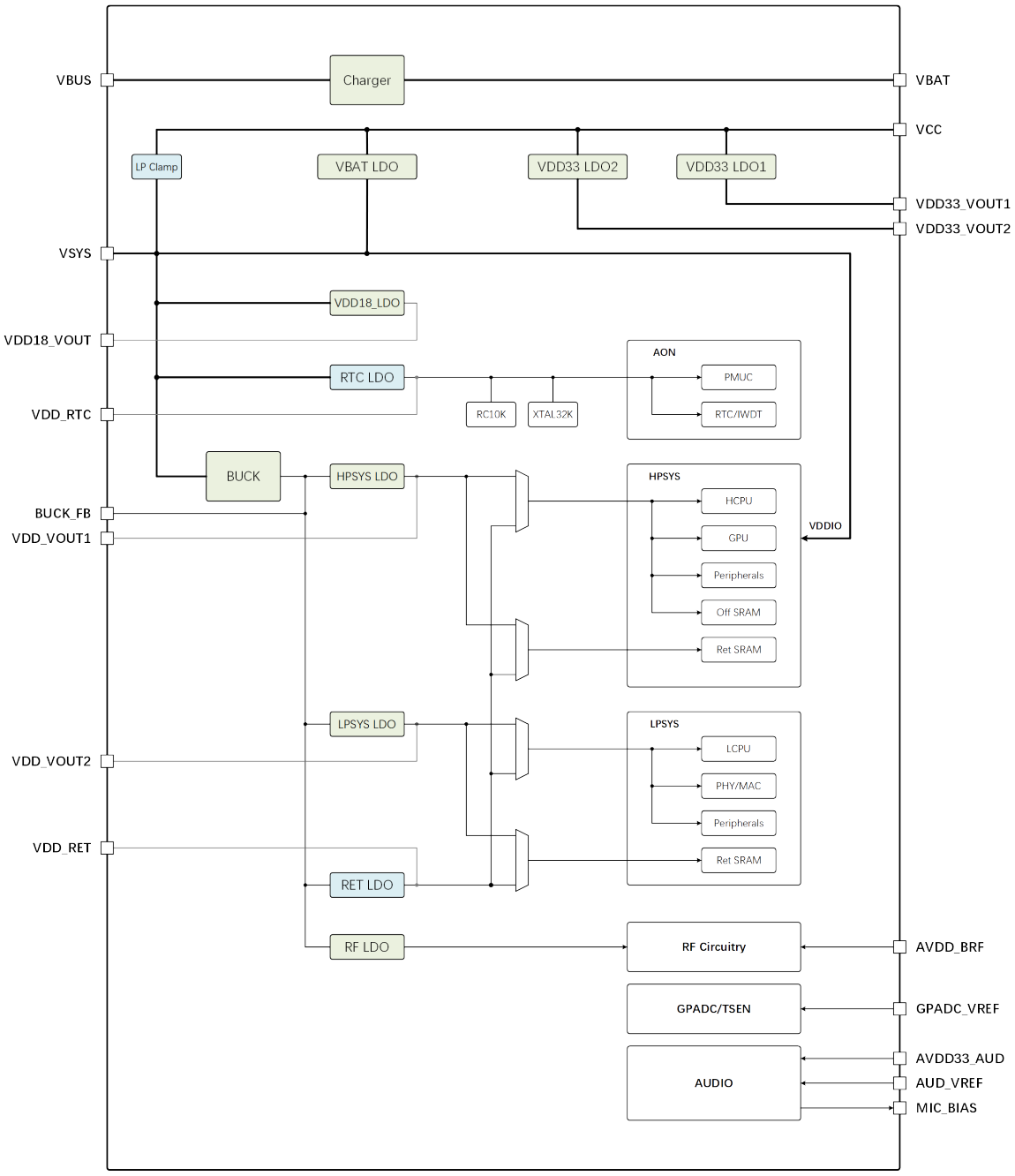

图 1-2: QFN 封装电源管理架构

1.4.1 充电模块

芯片集成了锂电池充电模块。充电电流和满电电压均可调节，充电电流最大支持 560mA。客户可根据电池规格和 VBUS 端线阻的大小，设置相应的参数。

图1-3是电池的充电曲线。当电池电压低于 V_{cc} 时，充电模块处于 Trickle Charge 模式，会以较低的电流 I_{tri} 给电池充电。当电池电压高于 V_{cc} 之后，充电模块处于 Constant Charge 模式，并且以恒流 I_{cc} 充电直到电池电压接近设置的满电电压 V_{cv}。之后，充电模块就进入 Constant Voltage 模式。在这个模式下，充电电流会慢慢下降，直到电流小于截止充电电流 I_{end}，充电环路自动断开，进入 Charger Full 模式。满电之后，如果电源适配器没有断开，那么电池电压经过一段时间消耗降低到 Re-Charge Threshold，会自动开启充电程序直到电池满电。

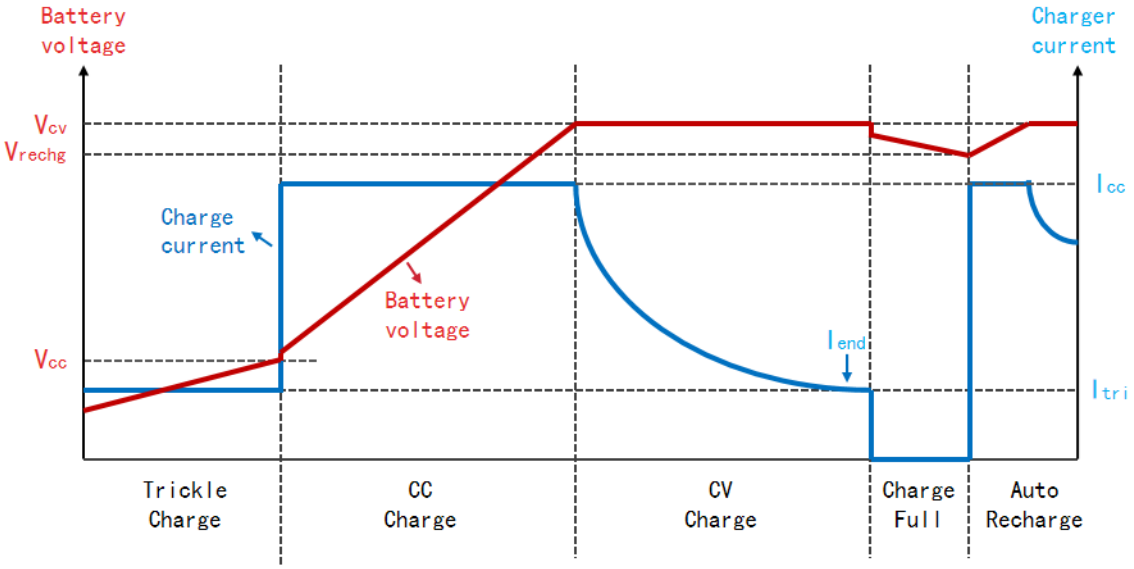

图 1-3: 充电曲线

2 时钟与复位

2.1 简介

时钟与复位模块用于控制芯片时钟与复位，可实现时钟选择、时钟分频、各模块使能、各模块复位等功能。

2.2 时钟源

芯片内部主要时钟源如下表。各功能模块时钟均基于这些时钟源产生。

表 2-1: 时钟源

时钟	频率	依赖关系
lrc10	~10kHz	无
lrc32	~32kHz	无
lxt32	32.768kHz	32k 晶振
hrc48	~48MHz	无
hxt48	48MHz	48M 晶振
dll1/2	48~384MHz	hxt48
audpll	49.152MHz	hxt48

hrc48 使用前应进行校准，校准相关寄存器为 HRCCAL1 和 HRCCAL2。

dll1/2 可独立产生不同频率的时钟，以 24MHz 为阶梯可配置，配置寄存器分别为 DLL1CR 和 DLL2CR。

2.3 系统时钟结构

系统时钟 clk_sys 可在 hrc48、hxt48 和 dll1 中选择。选择寄存器为 CSR_SEL_SYS。系统时钟频率的上限会随不同工作档位发生变化。

HCLK 由系统时钟 1 比 N 分频产生，分频比为 CFGR_HDIV。HCLK 是 HCPU、GPU、DMAC1 等 AHB 模块，以及 AHB 总线和 SRAM 的工作时钟。

PCLK 由 HCLK 1 比 2^N 分频产生，分频比为 2^{CFGR_PDIV1}。PCLK 是 GPTIM、BTIM1 等 APB 模块的工作时钟，以及 APB 总线时钟。

PCLK2 由 HCLK 1 比 2^N 分频产生，分频比为 2^{CFGR_PDIV2}。PCLK2 是 HPAON 模块的总线时钟。

MPI1/2 的工作时钟可在 clk_peri、dll1 和 dll2 中选择。选择寄存器为 CSR_SEL_MPI1/2。

USBC 的工作时钟可在 clk_sys 和 dll2 中选择，选择寄存器为 CSR_SEL_USB，并经 1 比 N 分频产生，分频比为 USBCR_DIV。USBC 的工作时钟频率需固定为 60MHz，时钟源频率应当为 60MHz 的整数倍。

USART/SPI/I2C 等外设的工作时钟 clk_peri 可在 hrc48 和 hxt48 中选择。选择寄存器为 CSR_SEL_PERI。clk_peri 独立于系统时钟，因此可在系统动态调节频率时保证外设工作不受影响。

BTIM2/GPTIM2 的工作时钟是 clk_peri 的二分频，可在系统动态调节频率时保证计数不受影响。

音频模块 I2S/AUDPRC/CODEC 的工作时钟来源于 audpll，而 PDM 的时钟为 audpll 的 16 分频。在使用某些音频采样率时，音频模块也可直接工作在 hxt48 上。

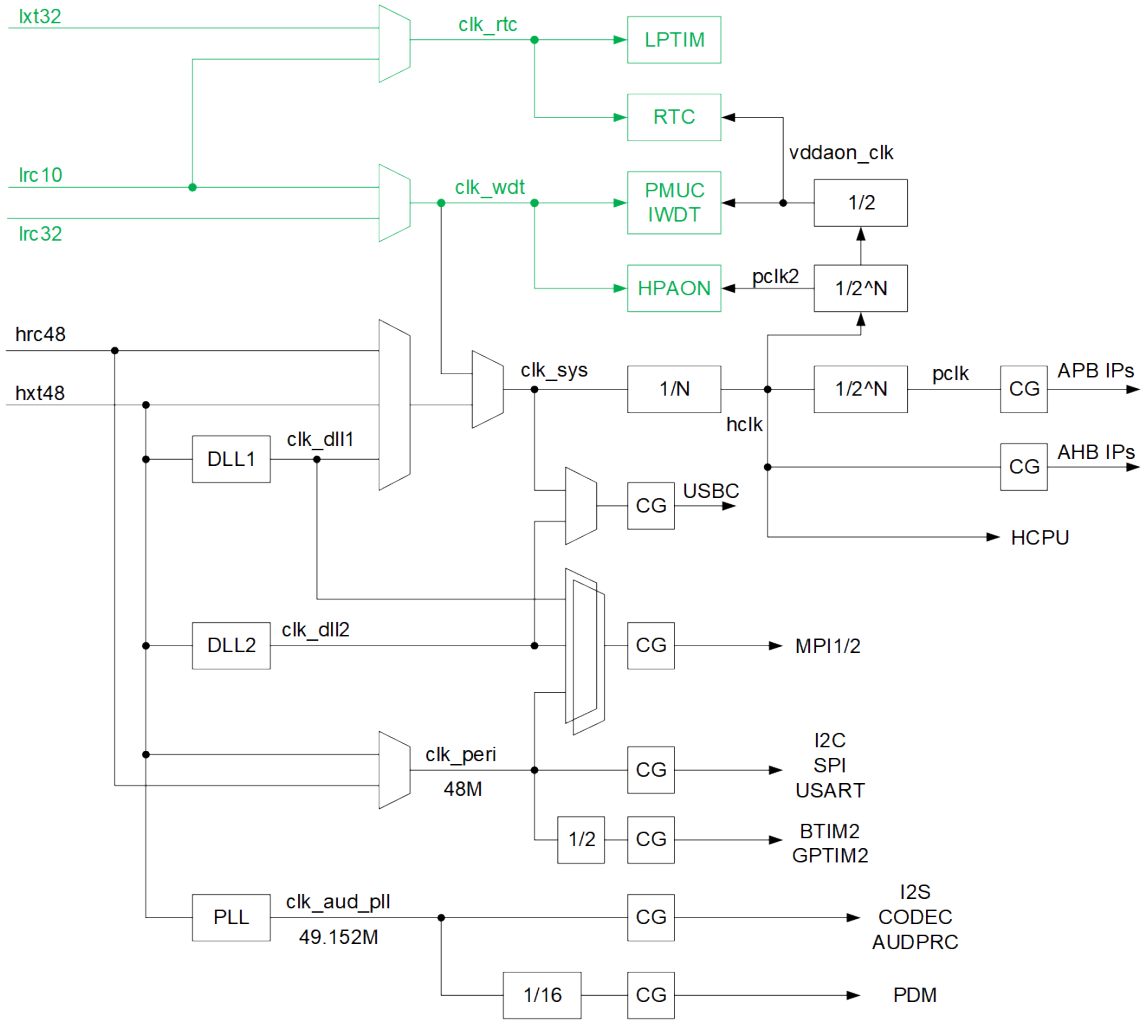

图 2-1: 系统时钟结构

低功耗时钟 clk_rtc 可在 lrc10 和 lxt32 中选择，是 RTC、LPTIM 等模块的工作时钟。clk_rtc 相关模块时钟选择方法见下表。

表 2-2: clk_rtc 相关模块时钟选择方法

模块	RTC->CR_LPCKSEL=0	RTC->CR_LPCKSEL=1
RTC	lrc10	lxt32
LPTIM1	lrc10	lxt32
LPTIM2	lrc10	lxt32
GTIM	lrc10	lxt32

低功耗时钟 clk_wdt 可在 lrc10 和 lrc32 中选择，是 PMUC、IWDT 等模块的工作时钟。clk_wdt 相关模块时钟选择方法见下表。

表 2-3: clk_wdt 相关模块时钟选择方法

模块	PMUC->CR_SEL_LPCLK=0	PMUC->CR_SEL_LPCLK=1
WDT1	lrc10	lrc32
IWDT	lrc10	lrc32
PMUC	lrc10	lrc32

2.4 模块使能

ENR1 和 ENR2 寄存器控制各模块使能。模块对应比特为 1 时，该模块寄存器可以访问，模块能够工作。模块对应比特为 0 时，该模块的工作时钟与总线时钟均关闭，模块停止工作，寄存器也无法访问，但寄存器值不会被复位。

ESR1 和 ESR2 寄存器可用于按位操作打开模块使能。向模块对应比特位写 1，可以打开对应模块使能，其它模块不受影响。

ECR1 和 ECR2 寄存器可用于按位操作关闭模块使能。向模块对应比特位写 1，可以关闭对应模块使能，其它模块不受影响。

2.5 模块复位

RSTR1 和 RSTR2 寄存器控制各模块复位。模块对应比特为 1 时，该模块寄存器与内部状态均被复位。模块对应比特为 0 时，模块停止复位。

2.6 HPSYS_RCC 寄存器

表 2-4: HPSYS_RCC 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00			**RSTR1**	**Reset Register 1**
[31]	rw	1'h0	PTC1	
[30]		1'h0	RSVD	
[29]		1'h0	RSVD	
[28]	rw	1'h0	I2C2	
[27]	rw	1'h0	I2C1	
[26]		1'h0	RSVD	
[25]	rw	1'h0	PDM1	
[24]		1'h0	RSVD	
[23]		1'h0	RSVD	
[22]	rw	1'h0	EXTDMA	
[21]	rw	1'h0	SPI2	
[20]	rw	1'h0	SPI1	
[19]		1'h0	RSVD	
[18]	rw	1'h0	BTIM2	
[17]	rw	1'h0	BTIM1	
[16]	rw	1'h0	GPTIM2	

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表 2-4: HPSYS_RCC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[15]	rw	1'h0	GPTIM1	
[14]	rw	1'h0	TRNG	
[13]	rw	1'h0	CRC1	
[12]	rw	1'h0	AES	
[11]	rw	1'h0	EFUSEC	
[10]	rw	1'h0	SYSCFG1	
[9]		1'h0	RSVD	
[8]	rw	1'h0	I2S1	
[7]	rw	1'h0	LCDC1	
[6]	rw	1'h0	EPIC	
[5]	rw	1'h0	EZIP1	
[4]	rw	1'h0	USART2	
[3]	rw	1'h0	USART1	
[2]	rw	1'h0	PINMUX1	
[1]	rw	1'h0	MAILBOX1	
[0]	rw	1'h0	DMAC1	0 - no reset; 1 - reset
0x04			**RSTR2**	**Reset Register 2**
[31:26]		6'h0	RSVD	
[25]	rw	1'h0	I2C4	
[24]		1'h0	RSVD	
[23]	rw	1'h0	TSEN	
[22]	rw	1'h0	GPADC	
[21]		1'h0	RSVD	
[20]	rw	1'h0	AUDPRC	
[19]	rw	1'h0	AUDCODEC	
[18]		1'h0	RSVD	
[17]		1'h0	RSVD	
[16]		1'h0	RSVD	
[15]		1'h0	RSVD	
[14]		1'h0	RSVD	
[13]		1'h0	RSVD	
[12]	rw	1'h0	USART3	
[11]		1'h0	RSVD	
[10]		1'h0	RSVD	
[9]	rw	1'h0	ATIM1	
[8]	rw	1'h0	I2C3	
[7]		1'h0	RSVD	
[6]	rw	1'h0	USBC	
[5]		1'h0	RSVD	
[4]	rw	1'h0	SDMMC1	
[3]		1'h0	RSVD	
[2]	rw	1'h0	MPI2	
[1]	rw	1'h0	MPI1	
[0]	rw	1'h0	GPIO1	0 - no reset; 1 - reset
0x08			**ENR1**	**Enable Register 1**
[31]	rw	1'h0	PTC1	
[30]		1'h0	RSVD	
[29]		1'h0	RSVD	

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表 2-4: HPSYS_RCC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[28]	rw	1'h1	I2C2	
[27]	rw	1'h1	I2C1	
[26]		1'h0	RSVD	
[25]	rw	1'h0	PDM1	
[24]		1'h0	RSVD	
[23]	rw	1'h1	SECU1	
[22]	rw	1'h1	EXTDMA	
[21]	rw	1'h0	SPI2	
[20]	rw	1'h0	SPI1	
[19]		1'h0	RSVD	
[18]	rw	1'h1	BTIM2	
[17]	rw	1'h1	BTIM1	
[16]	rw	1'h1	GPTIM2	
[15]	rw	1'h1	GPTIM1	
[14]	rw	1'h1	TRNG	
[13]	rw	1'h1	CRC1	
[12]	rw	1'h1	AES	
[11]	rw	1'h1	EFUSEC	
[10]	rw	1'h1	SYSCFG1	
[9]		1'h0	RSVD	
[8]	rw	1'h0	I2S1	
[7]	rw	1'h0	LCDC1	
[6]	rw	1'h0	EPIC	
[5]	rw	1'h0	EZIP1	
[4]	rw	1'h1	USART2	
[3]		1'h0	RSVD	
[2]	rw	1'h1	PINMUX1	
[1]	rw	1'h1	MAILBOX1	
[0]	rw	1'h1	DMAC1	write 1 to set module enable, write 0 to disable module
0x0C			**ENR2**	**Enable Register 2**
[31:26]		6'h0	RSVD	
[25]	rw	1'h1	I2C4	
[24]		1'h0	RSVD	
[23]	rw	1'h0	TSEN	
[22]	rw	1'h1	GPADC	
[21]		1'h0	RSVD	
[20]	rw	1'h0	AUDPRC	
[19]	rw	1'h0	AUDCODEC	
[18]		1'h0	RSVD	
[17]		1'h0	RSVD	
[16]		1'h0	RSVD	
[15]		1'h0	RSVD	
[14]		1'h0	RSVD	
[13]		1'h0	RSVD	
[12]	rw	1'h1	USART3	
[11]		1'h0	RSVD	
[10]		1'h0	RSVD	
[9]	rw	1'h0	ATIM1	

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表 2-4: HPSYS_RCC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[8]	rw	1'h1	I2C3	
[7]		1'h0	RSVD	
[6]	rw	1'h0	USBC	
[5]		1'h0	RSVD	
[4]	rw	1'h0	SDMMC1	
[3]		1'h0	RSVD	
[2]	rw	1'h1	MPI2	
[1]	rw	1'h1	MPI1	
[0]	rw	1'h1	GPIO1	write 1 to set module enable, write 0 to disable module
0x10			**ESR1**	**Enable Set Register 1**
[31]	w	1'h0	PTC1	
[30]		1'h0	RSVD	
[29]		1'h0	RSVD	
[28]	w	1'h0	I2C2	
[27]	w	1'h0	I2C1	
[26]		1'h0	RSVD	
[25]	w	1'h0	PDM1	
[24]		1'h0	RSVD	
[23]	w	1'h0	SECU1	
[22]	w	1'h0	EXTDMA	
[21]	w	1'h0	SPI2	
[20]	w	1'h0	SPI1	
[19]		1'h0	RSVD	
[18]	w	1'h0	BTIM2	
[17]	w	1'h0	BTIM1	
[16]	w	1'h0	GPTIM2	
[15]	w	1'h0	GPTIM1	
[14]	w	1'h0	TRNG	
[13]	w	1'h0	CRC1	
[12]	w	1'h0	AES	
[11]	w	1'h0	EFUSEC	
[10]	w	1'h0	SYSCFG1	
[9]		1'h0	RSVD	
[8]	w	1'h0	I2S1	
[7]	w	1'h0	LCDC1	
[6]	w	1'h0	EPIC	
[5]	w	1'h0	EZIP1	
[4]	w	1'h0	USART2	
[3]		1'h0	RSVD	
[2]	w	1'h0	PINMUX1	
[1]	w	1'h0	MAILBOX1	
[0]	w	1'h0	DMAC1	write 1 to set module enable, write 0 has no effect
0x14			**ESR2**	**Enable Set Register 2**
[31:26]		6'h0	RSVD	
[25]	w	1'h0	I2C4	
[24]		1'h0	RSVD	
[23]	w	1'h0	TSEN	
[22]	w	1'h0	GPADC	

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表 2-4: HPSYS_RCC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[21]		1'h0	RSVD	
[20]	w	1'h0	AUDPRC	
[19]	w	1'h0	AUDCODEC	
[18]		1'h0	RSVD	
[17]		1'h0	RSVD	
[16]		1'h0	RSVD	
[15]		1'h0	RSVD	
[14]		1'h0	RSVD	
[13]		1'h0	RSVD	
[12]	w	1'h0	USART3	
[11]		1'h0	RSVD	
[10]		1'h0	RSVD	
[9]	w	1'h0	ATIM1	
[8]	w	1'h0	I2C3	
[7]		1'h0	RSVD	
[6]	w	1'h0	USBC	
[5]		1'h0	RSVD	
[4]	w	1'h0	SDMMC1	
[3]		1'h0	RSVD	
[2]	w	1'h0	MPI2	
[1]	w	1'h0	MPI1	
[0]	w	1'h0	GPIO1	write 1 to set module enable, write 0 has no effect
0x18			**ECR1**	**Enable Clear Register 1**
[31]	w	1'h0	PTC1	
[30]		1'h0	RSVD	
[29]		1'h0	RSVD	
[28]	w	1'h0	I2C2	
[27]	w	1'h0	I2C1	
[26]		1'h0	RSVD	
[25]	w	1'h0	PDM1	
[24]		1'h0	RSVD	
[23]	w	1'h0	SECU1	
[22]	w	1'h0	EXTDMA	
[21]	w	1'h0	SPI2	
[20]	w	1'h0	SPI1	
[19]		1'h0	RSVD	
[18]	w	1'h0	BTIM2	
[17]	w	1'h0	BTIM1	
[16]	w	1'h0	GPTIM2	
[15]	w	1'h0	GPTIM1	
[14]	w	1'h0	TRNG	
[13]	w	1'h0	CRC1	
[12]	w	1'h0	AES	
[11]	w	1'h0	EFUSEC	
[10]	w	1'h0	SYSCFG1	
[9]		1'h0	RSVD	
[8]	w	1'h0	I2S1	
[7]	w	1'h0	LCDC1	

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表 2-4: HPSYS_RCC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[6]	w	1'h0	EPIC	
[5]	w	1'h0	EZIP1	
[4]	w	1'h0	USART2	
[3]		1'h0	RSVD	
[2]	w	1'h0	PINMUX1	
[1]	w	1'h0	MAILBOX1	
[0]	w	1'h0	DMAC1	write 1 to clear module enable, write 0 has no effect
0x1C			**ECR2**	**Enable Clear Register 2**
[31:26]		6'h0	RSVD	
[25]	w	1'h0	I2C4	
[24]		1'h0	RSVD	
[23]	w	1'h0	TSEN	
[22]	w	1'h0	GPADC	
[21]		1'h0	RSVD	
[20]	w	1'h0	AUDPRC	
[19]	w	1'h0	AUDCODEC	
[18]		1'h0	RSVD	
[17]		1'h0	RSVD	
[16]		1'h0	RSVD	
[15]		1'h0	RSVD	
[14]		1'h0	RSVD	
[13]		1'h0	RSVD	
[12]	w	1'h0	USART3	
[11]		1'h0	RSVD	
[10]		1'h0	RSVD	
[9]	w	1'h0	ATIM1	
[8]	w	1'h0	I2C3	
[7]		1'h0	RSVD	
[6]	w	1'h0	USBC	
[5]		1'h0	RSVD	
[4]	w	1'h0	SDMMC1	
[3]		1'h0	RSVD	
[2]	w	1'h0	MPI2	
[1]	w	1'h0	MPI1	
[0]	w	1'h0	GPIO1	write 1 to clear module enable, write 0 has no effect
0x20			**CSR**	**Clock Select Register**
[31:16]		16'h0	RSVD	
[15]	rw	1'b0	SEL_USBC	select clock source for USBC. 0 - clk_sys; 1 - dll2
[14:13]	rw	2'h0	SEL_TICK	select clock source for systick reference. 0 - clk_rtc; 1 - RSVD; 2 - hrc48; 3 - hxt48
[12]	rw	1'h1	SEL_PERI	select clock source for clk_peri. 0 - hrc48; 1 - hxt48. clk_peri is the clock source of USART/SPI/I2C/GPTIM2/BTIM2
[11:10]		2'h0	RSVD	
[9:8]		2'h0	RSVD	
[7:6]	rw	2'h0	SEL_MPI2	select clock source for MPI2. 0 - clk_peri; 1 - dll1; 2 - dll2; 3 - dbl96
[5:4]	rw	2'h0	SEL_MPI1	select clock source for MPI1. 0 - clk_peri; 1 - dll1; 2 - dll2; 3 - dbl96
[3]		1'h0	RSVD	
[2]	rw	1'h0	SEL_SYS_LP	if set to 1, clk_sys will switch to clk_wdt

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表 2-4: HPSYS_RCC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[1:0]	rw	2'h0	SEL_SYS	select clock source for clk_sys. 0 - hrc48; 1 - hxt48; 2 - dbl96; 3 - dll1
0x24			**CFGR**	**Clock Configuration Register**
[31:22]		10'h0	RSVD	
[21:16]	rw	6'h2	TICKDIV	systick reference is divided by TICKDIV
[15]		1'h0	RSVD	
[14:12]	rw	3'b100	PDIV2	PCLK2 = HCLK2 / (2^PDIV2), by default divided by 16
[11]		1'b0	RSVD	
[10:8]	rw	3'b001	PDIV1	PCLK1 = HCLK2 / (2^PDIV1), by default divided by 2
[7:0]	rw	8'h1	HDIV	HCLK = CLK_SYS / HDIV
0x28			**USBCR**	**USBC Control Register**
[31:3]		29'b0	RSVD	
[2:0]	rw	3'h4	DIV	USBC function clock is divided by DIV. USBC function clock should keep at 60MHz. For example, if USBC clock source is 240MHz dll2, DIV should be 4.
0x2C			**DLL1CR**	**DLL1 Control Register**
[31]	r	1'b0	READY	0: dll not ready 1: dll ready
[30:14]		17'h7	RSVD	
[13]	rw	1'b1	OUT_DIV2_EN	0: dll output not divided 1: dll output divided by 2
[12:6]	rw	7'h69	RSVD	
[5:2]	rw	4'h0	STG	dll lock frequency is (STG+1)×24MHz
[1]	rw	1'b0	RSVD	
[0]	rw	1'b0	EN	0: dll disabled 1: dll enabled
0x30			**DLL2CR**	**DLL2 Control Register**
[31]	r	1'b0	READY	0: dll not ready 1: dll ready
[30:14]		17'h7	RSVD	
[13]	rw	1'b1	OUT_DIV2_EN	0: dll output not divided 1: dll output divided by 2
[12:6]	rw	7'h69	RSVD	
[5:2]	rw	4'h0	STG	dll lock frequency is (STG+1)×24MHz
[1]	rw	1'b0	RSVD	
[0]	rw	1'b0	EN	0: dll disabled 1: dll enabled
0x34			**HRCCAL1**	**HRC Calibration Register 1**
[31]	r	1'b0	CAL_DONE	
[30]	rw	1'b0	CAL_EN	
[29:16]		14'b0	RSVD	
[15:0]	rw	16'h8000	CAL_LENGTH	
0x38			**HRCCAL2**	**HRC Calibration Register 2**
[31:16]	r	16'h0	HXT_CNT	
[15:0]	r	16'h0	HRC_CNT	
0x44			**DWCFGR**	**Deep WFI mode Clock Configuration Register**
[31:19]		13'h0	RSVD	
[18]	rw	1'h1	SEL_SYS_LP	0 - SYSCLK; 1 - CLK_LP
[17:16]	rw	2'h0	SEL_SYS	0 - HRC48; 1 - HXT48; 2 - RSVD; 3 - DLL1
[15]	rw	1'h1	DIV_EN	enable PDIV1, PDIV2 and HDIV reconfiguration during deep wfi

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表 2-4: HPSYS_RCC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[14:12]	rw	3'b001	PDIV2	PCLK2 = HCLK / (2^PDIV2) during deep wfi
[11]		1'b0	RSVD	
[10:8]	rw	3'b001	PDIV1	PCLK = HCLK / (2^PDIV1) during deep wfi
[7:0]	rw	8'h1	HDIV	HCLK = CLK_SYS / HDIV during deep wfi

3 低功耗模式

3.1 简介

芯片支持多种低功耗模式，可满足不同场景下的低功耗需求。越省电的低功耗模式，唤醒源也更加受限，唤醒时间也更长。

3.2 主要工作模式汇总

芯片的主要工作模式见下表。除 active 模式外，其它模式均为低功耗模式。

工作模式	CPU	外设	SRAM	IO	LPTIM	唤醒源	唤醒时间
active	run	run	可访问	可翻转	run		
sleep	stop	run	可访问	可翻转	run	任意中断	<1us
deepsleep	stop	stop	不可访问 全保留	电平保持	run	RTC, 唤醒 IO, IO(PA), LPTIM1, 蓝牙	~250us
standby	reset	reset	不可访问 保留 384KB	电平保持	run	RTC, 唤醒 IO, LPTIM1, 蓝牙	~1ms
hibernate	reset	reset	不可访问 不保留	高阻/ 上拉/下拉	reset	RTC, 唤醒 IO	>2ms

3.2.1 Active 模式

处于 Active 模式时，CPU 与外设正常运行，SRAM 可访问，IO 可正常翻转。为降低运行时的功耗，可以为 CPU 与外设选择合适的时钟源与时钟频率，并仅在外设工作时打开外设的模块使能。Active 模式可以选择不同的工作档位，以满足高性能或低功耗运行等场景的需求。

所有低功耗模式仅能从 active 模式进入，并且退出时统一回到 active 模式。

3.2.2 Sleep 模式

处于 sleep 模式时，CPU 暂停执行指令，外设仍正常运行，SRAM 可访问，IO 可正常翻转。

PMR_MODE 寄存器为 0 时，CPU 通过执行 WFI 或 WFE 指令进入 sleep 模式，并可以被预先使能的中断快速唤醒并继续运行。

3.2.3 Deepsleep 模式

处于 deepsleep 模式时，系统内大部分时钟均被关闭，仅保留低功耗时钟。CPU 与外设均停止运行。SRAM 不可访问，内容均可保留。配置为输出的 IO 不可翻转，保持进入 deepsleep 模式之前的电平不变。

deepsleep 模式主要的唤醒源包括 RTC，唤醒 IO，IO(PA)，LPTIM1，以及蓝牙子系统的请求。唤醒源通过 WER 寄存器配置。

进入 deepsleep 模式前，应当先将系统时钟切换到 hrc48 上，避免唤醒后因 hxt48 或 dll 时钟未就绪造成唤醒延迟。

CPU 首先将 PMR_MODE 寄存器配置为 2，再执行 WFI 指令即可进入 deepsleep 模式。

唤醒源生效时，系统经过一定的初始化时间 (约 250us) 即可退出 deepsleep 模式，重新回到 active 模式。CPU，外设以及内存的状态均未丢失，CPU 可从进入 deepsleep 时的位置继续运行。

退出 deepsleep 模式时，系统会产生 AON 中断。软件可在中断处理函数中通过 WSR 寄存器查询唤醒源并进行相应处理。退出中断处理函数前，软件应通过 WCR 寄存器清除唤醒源，并清除 AON 中断标志位。软件还应及时将 PMR_MODE 寄存器清 0，避免进入错误的低功耗模式。唤醒后部分时钟 (如 hxt48，dll1/2 等) 需重新开启并等待稳定后才能使用。

3.2.4 Standby 模式

处于 standby 模式时，系统内大部分时钟与供电均被关闭，仅保留低功耗模块的时钟与供电。CPU 与外设均被复位。SRAM 不可访问，可保留 384KB(0x20020000~0x2007ffff)。配置为输出的 IO 不可翻转，保持进入 standby 模式之前的电平不变。

standby 模式主要的唤醒源包括 RTC，唤醒 IO，LPTIM1，以及蓝牙子系统的请求。唤醒源通过 WER 寄存器配置。

CPU 首先将 PMR_MODE 寄存器配置为 3，再执行 WFI 指令即可进入 standby 模式。

唤醒源生效时，系统经过一定的初始化时间 (约 1ms) 即可退出 standby 模式，重新进入 active 模式。CPU 和外设的状态均被复位，SRAM 保留 384KB，软件从启动地址重新运行，根据 PMR_MODE 选择不同的启动分支。

退出 standby 模式时，子系统会产生 AON 中断。软件可在中断处理函数中通过 WSR 寄存器查询唤醒源并进行相应处理。退出中断处理函数前，软件应通过 WCR 寄存器清除唤醒源，并清除 AON 中断标志位。软件还应及时将 PMR_MODE 寄存器清 0，避免进入错误的低功耗模式。唤醒后系统时钟自动切换到 hrc48。如需其它时钟源，应当重新开启并等待稳定后才能使用。唤醒后除低功耗模块以外的大部分外设被复位，使用前应当重新初始化。

3.2.5 Hibernate 模式

Hibernate 模式下芯片大部分时钟与供电均被关闭，仅保留部分低功耗模块的时钟与供电。CPU，外设，HPSYS_AON 寄存器均被复位。SRAM 内容均不保留。唤醒 IO 可配置为高阻，上拉或下拉，其它 IO 进入高阻状态。

Hibernate 模式下仅有 PMUC，RTC 和 IWDT 模块在工作，这些模块的寄存器可保持。

Hibernate 模式的唤醒源包括 RTC 和唤醒 IO。

将 PMUC 寄存器的 CR_HIBER_EN 置 1 可进入 hibernate 模式。唤醒源生效时，芯片经过一定的初始化时间 (>2ms) 即可退出 hibernate 模式，重新进入 active 模式，软件从启动地址重新运行，根据 CR_HIBER_EN 执行相应操作，并应及时将 CR_HIBER_EN 清 0。

3.3 HPSYS_AON 寄存器

表 3-1: HPSYS_AON 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00			**PMR**	**Power Mode Register**
[31:2]		30'h0	RSVD	
[1:0]	rw	2'h0	MODE	Power Mode: 2'h0 - active; 2'h1 - light sleep; 2'h2 - deep sleep; 2'h3 - standby
0x04			**CR1**	**Control Register 1**
[31]	rw	1'h0	GTIM_EN	Enable global timer
[30:12]		19'h0	RSVD	
[11:9]	rw	3'h0	PIN3_MODE	mode for wakeup PIN3 (PA27)
[8:6]	rw	3'h0	PIN2_MODE	mode for wakeup PIN2 (PA26)
[5:3]	rw	3'h0	PIN1_MODE	mode for wakeup PIN1 (PA25)
[2:0]	rw	3'h0	PIN0_MODE	mode for wakeup PIN0 (PA24) 0 - high level, 1 - low level, 2 - pos edge, 3 - neg edge, 4/5/6/7: pos or neg edge
0x08			**CR2**	**Control Register 2**
[31:24]		8'h0	RSVD	
[23:21]	rw	3'h0	PIN15_MODE	mode for wakeup PIN15 (PA39)
[20:18]	rw	3'h0	PIN14_MODE	mode for wakeup PIN14 (PA38)
[17:15]	rw	3'h0	PIN13_MODE	mode for wakeup PIN13 (PA37)
[14:12]	rw	3'h0	PIN12_MODE	mode for wakeup PIN12 (PA36)
[11:9]	rw	3'h0	PIN11_MODE	mode for wakeup PIN11 (PA35)
[8:6]	rw	3'h0	PIN10_MODE	mode for wakeup PIN10 (PA34) 0 - high level, 1 - low level, 2 - pos edge, 3 - neg edge, 4/5/6/7: pos or neg edge
[5:0]		6'h0	RSVD	
0x0C			**CR3**	**Control Register 3**
[31:15]		17'h0	RSVD	
[14:12]	rw	3'h0	PIN20_MODE	mode for wakeup PIN20 (PA44)
[11:9]	rw	3'h0	PIN19_MODE	mode for wakeup PIN19 (PA43)
[8:6]	rw	3'h0	PIN18_MODE	mode for wakeup PIN18 (PA42)
[5:3]	rw	3'h0	PIN17_MODE	mode for wakeup PIN17 (PA41)
[2:0]	rw	3'h0	PIN16_MODE	mode for wakeup PIN16 (PA40) 0 - high level, 1 - low level, 2 - pos edge, 3 - neg edge, 4/5/6/7: pos or neg edge
0x10			**ACR**	**Active Mode Control register**
[31]	r	1'b0	HXT48_RDY	Indicate HXT48 is ready
[30]	r	1'b0	HRC48_RDY	Indicate HRC48 is ready
[29:2]		28'h1	RSVD	
[1]	rw	1'b1	HXT48_REQ	Request HXT48 in active mode
[0]	rw	1'b1	HRC48_REQ	Request HRC48 in active mode
0x14			**LSCR**	**Light Sleep Ctrl Register**
[31:3]		29'b0	RSVD	
[2]	rw	1'b1	PWR_REQ	Request power during Light Sleep mode
[1]	rw	1'b1	HXT48_REQ	Request HXT48 in Light Sleep mode
[0]	rw	1'b1	HRC48_REQ	Request HRC48 in Light Sleep mode
0x18			**DSCR**	**Deep Sleep Ctrl Register**
[31:3]		29'b0	RSVD	
[2]	rw	1'b1	PWR_REQ	Request power during Deep Sleep mode
[1]	rw	1'b0	HXT48_REQ	Request HXT48 in Deep Sleep mode
[0]	rw	1'b0	HRC48_REQ	Request HRC48 in Deep Sleep mode
0x1C			**SBCR**	**Standby Mode Ctrl Register**
[31:3]		29'b0	RSVD	
[2]	rw	1'b0	PWR_REQ	Request power during Standby mode

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表 3-1: HPSYS_AON 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[1]	rw	1'b0	HXT48_REQ	Request HXT48 in Standby mode
[0]	rw	1'b0	HRC48_REQ	Request HRC48 in Standby mode
0x20			**WER**	**Wakeup Enable register**
[31:29]		3'b0	RSVD	
[28]	rw	1'b0	PIN20	Set 1 to enable PA44 as wakeup source
[27]	rw	1'b0	PIN19	Set 1 to enable PA43 as wakeup source
[26]	rw	1'b0	PIN18	Set 1 to enable PA42 as wakeup source
[25]	rw	1'b0	PIN17	Set 1 to enable PA41 as wakeup source
[24]	rw	1'b0	PIN16	Set 1 to enable PA40 as wakeup source
[23]	rw	1'b0	PIN15	Set 1 to enable PA39 as wakeup source
[22]	rw	1'b0	PIN14	Set 1 to enable PA38 as wakeup source
[21]	rw	1'b0	PIN13	Set 1 to enable PA37 as wakeup source
[20]	rw	1'b0	PIN12	Set 1 to enable PA36 as wakeup source
[19]	rw	1'b0	PIN11	Set 1 to enable PA35 as wakeup source
[18]	rw	1'b0	PIN10	Set 1 to enable PA34 as wakeup source
[17:12]		6'b0	RSVD	
[11]	rw	1'b0	PIN3	Set 1 to enable PA27 as wakeup source
[10]	rw	1'b0	PIN2	Set 1 to enable PA26 as wakeup source
[9]	rw	1'b0	PIN1	Set 1 to enable PA25 as wakeup source
[8]	rw	1'b0	PIN0	Set 1 to enable PA24 as wakeup source
[7]	rw	1'b0	LP2HP_IRQ	Set 1 to enable MAILBOX2 as wakeup source
[6]	rw	1'b0	LP2HP_REQ	Set 1 to enable LPSYS request as wakeup source
[5:4]		2'b0	RSVD	
[3]	rw	1'b0	PMUC	Set 1 to enable PMUC as wakeup source
[2]	rw	1'b0	LPTIM1	Set 1 to enable LPTIM1 as wakeup source
[1]	rw	1'b0	GPIO1	Set 1 to enable IO(PA) as wakeup source
[0]	rw	1'b0	RTC	Set 1 to enable RTC as wakeup source
0x24			**WSR**	**Wakeup Status register**
[31:29]		3'b0	RSVD	
[28]	r	1'b0	PIN20	Indicates the wakeup status from PA44 request. Note: the status is masked by WER
[27]	r	1'b0	PIN19	Indicates the wakeup status from PA43 request. Note: the status is masked by WER
[26]	r	1'b0	PIN18	Indicates the wakeup status from PA42 request. Note: the status is masked by WER
[25]	r	1'b0	PIN17	Indicates the wakeup status from PA41 request. Note: the status is masked by WER
[24]	r	1'b0	PIN16	Indicates the wakeup status from PA40 request. Note: the status is masked by WER
[23]	r	1'b0	PIN15	Indicates the wakeup status from PA39 request. Note: the status is masked by WER
[22]	r	1'b0	PIN14	Indicates the wakeup status from PA38 request. Note: the status is masked by WER
[21]	r	1'b0	PIN13	Indicates the wakeup status from PA37 request. Note: the status is masked by WER
[20]	r	1'b0	PIN12	Indicates the wakeup status from PA36 request. Note: the status is masked by WER
[19]	r	1'b0	PIN11	Indicates the wakeup status from PA35 request. Note: the status is masked by WER
[18]	r	1'b0	PIN10	Indicates the wakeup status from PA34 request. Note: the status is masked by WER
[17:12]		6'b0	RSVD	
[11]	r	1'b0	PIN3	Indicates the wakeup status from PA27 request. Note: the status is masked by WER
[10]	r	1'b0	PIN2	Indicates the wakeup status from PA26 request. Note: the status is masked by WER
[9]	r	1'b0	PIN1	Indicates the wakeup status from PA25 request. Note: the status is masked by WER
[8]	r	1'b0	PIN0	Indicates the wakeup status from PA24 request. Note: the status is masked by WER
[7]	r	1'b0	LP2HP_IRQ	Indicates the wakeup status from MAILBOX2. Note: the status is masked by WER
[6]	r	1'b0	LP2HP_REQ	Indicates the wakeup status from LPSYS request. Note: the status is masked by WER
[5:4]		2'b0	RSVD	

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表 3-1: HPSYS_AON 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[3]	r	1'b0	PMUC	Indicates the wakeup status from PMUC. Note: the status is masked by WER
[2]	r	1'b0	LPTIM1	Indicates the wakeup status from LPTIM1. Note: the status is masked by WER
[1]	r	1'b0	GPIO1	Indicates the wakeup status from IO(PA). Note: the status is masked by WER
[0]	r	1'b0	RTC	Indicates the wakeup status from RTC. Note: the status is masked by WER
0x28			**WCR**	**Wakeup Clear register**
[31]	w1c	1'b0	AON	Write 1 to clear the AON wakeup IRQ status
[30:29]		2'b0	RSVD	
[28]	w1c	1'b0	PIN20	Write 1 to clear PA44 wakeup source. Only valid if PIN wakeup is configured as edge trigger
[27]	w1c	1'b0	PIN19	Write 1 to clear PA43 wakeup source. Only valid if PIN wakeup is configured as edge trigger
[26]	w1c	1'b0	PIN18	Write 1 to clear PA42 wakeup source. Only valid if PIN wakeup is configured as edge trigger
[25]	w1c	1'b0	PIN17	Write 1 to clear PA41 wakeup source. Only valid if PIN wakeup is configured as edge trigger
[24]	w1c	1'b0	PIN16	Write 1 to clear PA40 wakeup source. Only valid if PIN wakeup is configured as edge trigger
[23]	w1c	1'b0	PIN15	Write 1 to clear PA39 wakeup source. Only valid if PIN wakeup is configured as edge trigger
[22]	w1c	1'b0	PIN14	Write 1 to clear PA38 wakeup source. Only valid if PIN wakeup is configured as edge trigger
[21]	w1c	1'b0	PIN13	Write 1 to clear PA37 wakeup source. Only valid if PIN wakeup is configured as edge trigger
[20]	w1c	1'b0	PIN12	Write 1 to clear PA36 wakeup source. Only valid if PIN wakeup is configured as edge trigger
[19]	w1c	1'b0	PIN11	Write 1 to clear PA35 wakeup source. Only valid if PIN wakeup is configured as edge trigger
[18]	w1c	1'b0	PIN10	Write 1 to clear PA34 wakeup source. Only valid if PIN wakeup is configured as edge trigger
[17:12]		6'b0	RSVD	
[11]	w1c	1'b0	PIN3	Write 1 to clear PA27 wakeup source. Only valid if PIN wakeup is configured as edge trigger
[10]	w1c	1'b0	PIN2	Write 1 to clear PA26 wakeup source. Only valid if PIN wakeup is configured as edge trigger
[9]	w1c	1'b0	PIN1	Write 1 to clear PA25 wakeup source. Only valid if PIN wakeup is configured as edge trigger
[8]	w1c	1'b0	PIN0	Write 1 to clear PA24 wakeup source. Only valid if PIN wakeup is configured as edge trigger
[7:0]		8'b0	RSVD	Note: for RTC/IO(PA)/LPTIM/PMUC, clear the wakeup status directly in the orignal module
0x2C			**ISSR**	**Inter System Wakeup Register**
[31:6]		26'b0	RSVD	
[5]	r	1'h1	LP_ACTIVE	read 1 indicates LPSYS is active
[4]	rw	1'h1	HP_ACTIVE	write 1 to indicates HPSYS is active
[3:2]		2'b0	RSVD	
[1]	r	1'b0	LP2HP_REQ	indicate LPSYS request exists
[0]	rw	1'b0	HP2LP_REQ	write 1 to request LPSYS to stay in active mode
0x30			**ANACR**	**Analog Control Register**

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表 3-1: HPSYS_AON 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:2]		30'b0	RSVD	
[1]	rw	1'b0	VHP_ISO	Set 1 to force off all HPSYS related analog modules
[0]	rw	1'b0	PA_ISO	Set 1 to force IO(PA) into retention mode
0x34			**GTIMR**	**Global Timer Register**
[31:0]	r	32'h0	CNT	Global timer value
0x38			**RESERVE0**	**Reserve Register 0**
[31:0]	rw	32'b0	DATA	
0x3C			**RESERVE1**	**Reserve Register 1**
[31:0]	rw	32'b0	DATA	

4 输入输出

4.1 简介

芯片最多支持 45 个可配置的通用 IO 管脚 PA00~PA44。每个通用 IO 可独立选择输入输出功能，并独立配置驱动强度和上下拉电阻。当配置为 GPIO 功能时，每个通用 IO 均可根据电平的高低或翻转触发中断，并可将系统从某些低功耗模式中唤醒。其中 PA24~PA27 还支持配置为低功耗 IO，用于在低功耗模式下进行输出。

4.2 IO 结构

单个通用 IO 的结构如下图。

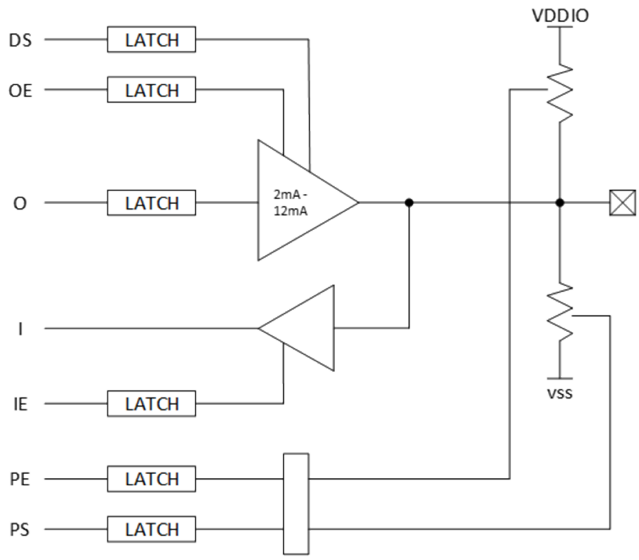

图 4-1: IO 结构

DS 用于配置驱动强度，由 PINMUX 对应 IO 的 DS0 和 DS1 寄存器指定。{DS1,DS0} 的值由 0 到 3，驱动强度逐渐增大。

IO 输出由 O 和 OE 确定，根据 PINMUX 对应 IO 的 FSEL 寄存器选择不同功能，自动映射到相应功能的输出。

IO 输入使能由 PINMUX 对应 IO 的 IE 寄存器控制。当 IE 为高时，输入电平 I 根据 PINMUX 对应 IO 的 FSEL 寄存器自动映射到相应功能的输入；当 IE 为低时，相应功能无法获取到 IO 的输入电平。

PE 和 PS 用于控制 IO 的上下拉电阻，由 PINMUX 对应 IO 的 PE 和 PS 寄存器指定。PE 为 0 时上下拉电阻均不生效。PE 为 1，PS 为 0 时，下拉电阻有效。PE 为 1，PS 为 1 时，上拉电阻有效。上下拉电阻的阻值约为 10k~40k 欧姆，与 IO 外部电路以及接口电平相关。

4.3 输入输出选择

通过配置 PINMUX 对应 IO 的 FSEL 寄存器，可以将可配置 IO 的输入输出映射为若干功能中的一种。每个 IO 能够映射的功能可以在 GPIO 管脚列表中查询。如果该功能为输入，或输入输出双向，还需要将对应 IO 的 IE 寄存器置 1。

每个通用 IO 均可映射为 GPIO 功能，此时 IO 的输出由 GPIO 模块控制。无论 IO 映射为哪种功能，IO 输入均能够从 GPIO 模块中读取，并可产生 GPIO 中断。

当某个 PA 映射为 PA_I2C_UART 功能时，该 IO 可以作为 HPSYS 中任意一个 I2C 或 USART 的接口信号使用。具体作为哪个接口信号还需要在 HPSYS_CFG 寄存器中指定。例如若要让 PA07 作为 USART2 的 TXD 使用，需设置 PINMUX 寄存器的 PAD_PA07_FSEL 为 4(对应 PA_I2C_UART)，并设置 HPSYS_CFG 寄存器的 USART2_PINR_TXD_PIN 为 7(对应 PA07)。应注意若将多个接口信号指定到同一个 IO 会引起功能错误。

当某个 PA 映射为 PA_TIM 功能时，该 IO 可以作为任意一个 ATIM/GPTIM/LPTIM 的接口信号使用。具体作为哪个接口信号还需要在 HPSYS_CFG 寄存器中指定。例如若要让 PA38 作为 GPTIM2 的 CH3 使用，需设置 PINMUX 寄存器的 PAD_PA38_FSEL 为 5(对应 PA_TIM)，并设置 HPSYS_CFG 寄存器的 GPTIM2_PINR_CH3_PIN 为 38(对应 PA38)。应注意若将多个接口信号指定到同一个 IO 会引起功能错误。

4.4 IO 高阻

芯片上电以后，IO 默认存在上拉或下拉电阻 (PE 默认值为 1)，需由软件将 IO 配置为所需状态。如果要让 IO 配置为高阻，需将 PE 设置为 0，IO 设置为 GPIO 功能，并且 GPIO 输出使能关闭。

4.5 GPIO 输出

当 IO 配置为 GPIO 功能时，IO 的 O 和 OE 控制信号由 GPIO 寄存器控制，从而产生 IO 的输出。通用 IO(PA00~PA44)由 HPSYS_GPIO 控制。GPIO 寄存器的每个比特对应一个通用 IO，例如 HPSYS_GPIO 中 DOER0 的比特 0 对应 PA00，比特 31 对应 PA31；DOER1 的比特 0 对应 PA32，比特 12 对应 PA44。

DOERx 寄存器直接控制 IO 的 OE 信号，为 1 时 IO 的输出导通，为 0 时 IO 的输出关断。软件可以直接配置 DOERx 寄存器，也可以配置 DOESRx 或 DOECRx 进行位操作以免影响其它 IO。

DORx 寄存器直接控制 IO 的 O 信号，为 1 时 IO 的输出为高电平，为 0 时 IO 的输出为低电平。软件可以直接配置 DORx 寄存器，也可以配置 DOSRx 或 DOCRx 进行位操作以免影响其它 IO。

GPIO 推挽输出的配置方法为：

推挽输出 0，需使 IO 的 OE 为 1 ，O 为 0，即 DOERx 对应比特配置为 1，DORx 对应比特配置为 0。

推挽输出 1，需使 IO 的 OE 为 1 ，O 为 1，即 DOERx 对应比特配置为 1，DORx 对应比特配置为 1。

当需要产生开漏输出时，应当首先根据翻转速率需求，使能 IO 内部上拉电阻 (PE=1,PS=1)，或在芯片外部连接上拉电阻。

GPIO 开漏输出的配置方法为：

开漏输出 0，需使 IO 的 OE 为 1 ，O 为 0，即 DOERx 对应比特配置为 1，DORx 对应比特配置为 0。

开漏输出 1，需使 IO 的 OE 为 0，即 DOERx 的对应比特配置为 0。

4.6 GPIO 输入

无论 IO 映射为哪种功能，IO 输入均能够从 GPIO 寄存器 DIRx 中读取，并可根据配置产生 GPIO 中断。

IO 中断使能应仅在需要时打开。软件可以直接配置 IERx 寄存器，也可以配置 IESRx 或 IECRx 进行位操作以免影响其它 IO。

即使 IO 未配置为 GPIO 功能，IO 中断仍可产生，因此当不需要 IO 产生中断时，应当确保其中断使能关闭。

GPIO 中断产生的条件包括 IO 输入信号为高电平/低电平/上升沿/下降沿/双边沿等，如下表所示。

IPH	IPL	ITR=0	ITR=1
0	0	不触发	不触发
0	1	低电平	下降沿
1	0	高电平	上升沿
1	1	无效配置	双边沿

ITR 用于选择中断条件类型。软件可以直接配置 ITRx 寄存器，也可以配置 ITSRx 或 ITCRx 进行位操作以免影响其它 IO。

IPH 用于使能高电平或上升沿中断条件。软件可以直接配置 IPHRx 寄存器，也可以配置 IPHSRx 或 IPHCRx 进行位操作以免影响其它 IO。

IPL 用于使能低电平或下降沿中断条件。软件可以直接配置 IPLRx 寄存器，也可以配置 IPLSRx 或 IPLCRx 进行位操作以免影响其它 IO。

产生中断的 IO 可通过 ISRx 查询。向 ISRx 的相应比特写 1 可以清除中断状态。

GPIO 中断可将系统从某些低功耗模式中唤醒。唤醒后，软件应查询 ISRx 判断唤醒源，并清除相关标志。

4.7 GPIO 管脚列表

表 4-1: 大核域 GPIO（PA）管脚列表

Pin Number		Pin Name	Type	Sel #	Functions
SF32LB520 (QFN68L)	SF32LB52x (QFN68L)				
51	51	PA00	I/O	0	GPIO_A0
				1	LCDC1_SPI_RSTB
				4	PA_I2C_UART
				5	PA_TIM
				7	LCDC1_8080_RSTB
				Others	Reserved
50	50	PA01	I/O	0	GPIO_A1
				4	PA_I2C_UART
				5	PA_TIM
				Others	Reserved
49	49	PA02	I/O	0	GPIO_A2
				1	LCDC1_SPI_TE
				3	I2S1_MCLK
				4	PA_I2C_UART
				5	PA_TIM
				6	LCDC1_JDI_B2
				7	LCDC1_8080_TE
				Others	Reserved
48	48	PA03	I/O	0	GPIO_A3
				1	LCDC1_SPI_CS
				3	I2S1_SDO
				4	PA_I2C_UART
				5	PA_TIM
				6	LCDC1_JDI_B1
				7	LCDC1_8080_CS
				Others	Reserved
47	47	PA04	I/O	0	GPIO_A4
				1	LCDC1_SPI_CLK
				3	I2S1_SDI
				4	PA_I2C_UART
				5	PA_TIM
				6	LCDC1_JDI_G1
				7	LCDC1_8080_WR
				Others	Reserved
46	46	PA05	I/O	0	GPIO_A5
				1	LCDC1_SPI_DIO0
				3	I2S1_BCK
				4	PA_I2C_UART
				5	PA_TIM
				6	LCDC1_JDI_R1
				7	LCDC1_8080_RD
				Others	Reserved

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表 4-1: GPIO（PA）管脚列表（续）

Pin Number		Pin Name	Type	Sel #	Functions
SF32LB520 (QFN68L)	SF32LB52x (QFN68L)				
45	45	PA06	I/O	0	GPIO_A6
				1	LCDC1_SPI_DIO1
				3	I2S1_LRCK
				4	PA_I2C_UART
				5	PA_TIM
				6	LCDC1_JDI_HST
				7	LCDC1_8080_DC
				Others	Reserved
44	44	PA07	I/O	0	GPIO_A7
				1	LCDC1_SPI_DIO2
				3	PDM1_CLK
				4	PA_I2C_UART
				5	PA_TIM
				6	LCDC1_JDI_ENB
				7	LCDC1_8080_DIO0
				Others	Reserved
43	43	PA08	I/O	0	GPIO_A8
				1	LCDC1_SPI_DIO3
				3	PDM1_DATA
				4	PA_I2C_UART
				5	PA_TIM
				6	LCDC1_JDI_VST
				7	LCDC1_8080_DIO1
				Others	Reserved
42	42	PA09	I/O	0	GPIO_A9
				4	PA_I2C_UART
				5	PA_TIM
				Others	Reserved
35	35	PA10	I/O	0	GPIO_A10
				4	PA_I2C_UART
				5	PA_TIM
				Others	Reserved
34	34	PA11	I/O	0	GPIO_A11
				4	PA_I2C_UART
				5	PA_TIM
				Others	Reserved
33	33	PA12	I/O	0	GPIO_A12
				1	MPI2_CS
				2	SD1_DIO2
				4	PA_I2C_UART
				5	PA_TIM
				Others	Reserved

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表 4-1: GPIO（PA）管脚列表（续）

Pin Number		Pin Name	Type	Sel #	Functions
SF32LB520 (QFN68L)	SF32LB52x (QFN68L)				
32	32	PA13	I/O	0	GPIO_A13
				1	MPI2_DIO1
				2	SD1_DIO3
				4	PA_I2C_UART
				5	PA_TIM
				Others	Reserved
31	31	PA14	I/O	0	GPIO_A14
				1	MPI2_DIO2
				2	SD1_CLK
				4	PA_I2C_UART
				5	PA_TIM
				Others	Reserved
30	30	PA15	I/O	0	GPIO_A15
				1	MPI2_DIO0
				2	SD1_CMD
				4	PA_I2C_UART
				5	PA_TIM
				Others	Reserved
29	29	PA16	I/O	0	GPIO_A16
				1	MPI2_CLK
				2	SD1_DIO0
				4	PA_I2C_UART
				5	PA_TIM
				Others	Reserved
28	28	PA17	I/O	0	GPIO_A17
				1	MPI2_DIO3
				2	SD1_DIO1
				4	PA_I2C_UART
				5	PA_TIM
				Others	Reserved
27	27	PA18	I/O	0	GPIO_A18
				2	SWDIO
				4	PA_I2C_UART
				5	PA_TIM
				Others	Reserved
26	26	PA19	I/O	0	GPIO_A19
				2	SWCLK
				4	PA_I2C_UART
				5	PA_TIM
				Others	Reserved

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表 4-1: GPIO（PA）管脚列表（续）

Pin Number		Pin Name	Type	Sel #	Functions
SF32LB520 (QFN68L)	SF32LB52x (QFN68L)				
25	25	PA20	I/O	0	GPIO_A20
				4	PA_I2C_UART
				5	PA_TIM
				Others	Reserved
24	-	PA21	I/O	0	GPIO_A21
				4	PA_I2C_UART
				5	PA_TIM
				Others	Reserved
11	11	PA22	I/O	0	GPIO_A22
				3	PDM1_CLK
				4	PA_I2C_UART
				5	PA_TIM
				8	#XTAL32K_XI
				Others	Reserved
10	10	PA23	I/O	0	GPIO_A23
				3	PDM1_DATA
				4	PA_I2C_UART
				5	PA_TIM
				8	#XTAL32K_XO
				Others	Reserved
9	9	PA24	I/O	0	GPIO_A24
				2	SPI1_DIO
				3	I2S1_MCLK
				4	PA_I2C_UART
				5	PA_TIM
				8	#WKUP_PIN0
				Others	Reserved
8	8	PA25	I/O	0	GPIO_A25
				2	SPI1_DI
				3	I2S1_SDO
				4	PA_I2C_UART
				5	PA_TIM
				7	#XTAL32K_EXT
				8	#WKUP_PIN1
				Others	Reserved
7	7	PA26	I/O	0	GPIO_A26
				4	PA_I2C_UART
				5	PA_TIM
				8	#WKUP_PIN2
				Others	Reserved

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表 4-1: GPIO（PA）管脚列表（续）

Pin Number		Pin Name	Type	Sel #	Functions
SF32LB520 (QFN68L)	SF32LB52x (QFN68L)				
6	6	PA27	I/O	0	GPIO_A27
				4	PA_I2C_UART
				5	PA_TIM
				8	#WKUP_PIN3
				Others	Reserved
5	5	PA28	I/O	0	GPIO_A28
				2	SPI1_CLK
				3	I2S1_SDI
				4	PA_I2C_UART
				5	PA_TIM
				7	#GPADC_CH1
				Others	Reserved
4	4	PA29	I/O	0	GPIO_A29
				2	SPI1_CS
				3	I2S1_BCK
				4	PA_I2C_UART
				5	PA_TIM
				7	#GPADC_CH2
				Others	Reserved
3	3	PA30	I/O	0	GPIO_A30
				2	#EFUSE_PWR
				3	I2S1_LRCK
				4	PA_I2C_UART
				5	PA_TIM
				7	#GPADC_CH3
				Others	Reserved
2	2	PA31	I/O	0	GPIO_A31
				4	PA_I2C_UART
				5	PA_TIM
				7	#GPADC_CH4
				Others	Reserved
1	1	PA32	I/O	0	GPIO_A32
				4	PA_I2C_UART
				5	PA_TIM
				7	#GPADC_CH5
				Others	Reserved

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表 4-1: GPIO（PA）管脚列表（续）

Pin Number		Pin Name	Type	Sel #	Functions
SF32LB520 (QFN68L)	SF32LB52x (QFN68L)				
67	67	PA33	I/O	0	GPIO_A33
				4	PA_I2C_UART
				5	PA_TIM
				7	#GPADC_CH6
				Others	Reserved
66	66	PA34	I/O	0	GPIO_A34
				4	PA_I2C_UART
				5	PA_TIM
				7	#GPADC_CH7
				8	#WKUP_PIN10
				Others	Reserved
65	65	PA35	I/O	0	GPIO_A35
				2	#USB11_DP
				4	PA_I2C_UART
				5	PA_TIM
				8	#WKUP_PIN11
				Others	Reserved
64	64	PA36	I/O	0	GPIO_A36
				2	#USB11_DM
				4	PA_I2C_UART
				5	PA_TIM
				8	#WKUP_PIN12
				Others	Reserved
63	63	PA37	I/O	0	GPIO_A37
				2	SPI2_DIO
				4	PA_I2C_UART
				5	PA_TIM
				7	LCDC1_8080_DIO2
				8	#WKUP_PIN13
				Others	Reserved
62	62	PA38	I/O	0	GPIO_A38
				2	SPI2_DI
				4	PA_I2C_UART
				5	PA_TIM
				8	#WKUP_PIN14
				Others	Reserved

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表 4-1: GPIO（PA）管脚列表（续）

Pin Number		Pin Name	Type	Sel #	Functions
SF32LB520 (QFN68L)	SF32LB52x (QFN68L)				
61	61	PA39	I/O	0	GPIO_A39
				2	SPI2_CLK
				4	PA_I2C_UART
				5	PA_TIM
				6	LCDC1_JDI_VCK
				7	LCDC1_8080_DIO3
				8	#WKUP_PIN15
				Others	Reserved
60	60	PA40	I/O	0	GPIO_A40
				2	SPI2_CS
				4	PA_I2C_UART
				5	PA_TIM
				6	LCDC1_JDI_XRST
				7	LCDC1_8080_DIO4
				8	#WKUP_PIN16
				Others	Reserved
59	59	PA41	I/O	0	GPIO_A41
				4	PA_I2C_UART
				5	PA_TIM
				6	LCDC1_JDI_HCK
				7	LCDC1_8080_DIO5
				8	#WKUP_PIN17
				Others	Reserved
58	58	PA42	I/O	0	GPIO_A42
				4	PA_I2C_UART
				5	PA_TIM
				6	LCDC1_JDI_R2
				7	LCDC1_8080_DIO6
				8	#WKUP_PIN18
				Others	Reserved
57	57	PA43	I/O	0	GPIO_A43
				4	PA_I2C_UART
				5	PA_TIM
				6	LCDC1_JDI_G2
				7	LCDC1_8080_DIO7
				8	#WKUP_PIN19
				Others	Reserved
56	56	PA44	I/O	0	GPIO_A44
				4	PA_I2C_UART
				5	PA_TIM
				8	#WKUP_PIN20
				Others	Reserved

4.8 HPSYS_PINMUX 寄存器

表 4-2: HPSYS_PINMUX 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x0			**PAD_SA00**	
[31:12]		20'h0	RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x4			**PAD_SA01**	
[31:12]		20'h0	RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x8			**PAD_SA02**	
[31:12]		20'h0	RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0xC			**PAD_SA03**	
[31:12]		20'h0	RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x10			**PAD_SA04**	

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表 4-2: HPSYS_PINMUX 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:12]		20'h0	RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x14			**PAD_SA05**	
[31:12]		20'h0	RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h1	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x18			**PAD_SA06**	
[31:12]		20'h0	RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h1	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x1C			**PAD_SA07**	
[31:12]		20'h0	RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x20			**PAD_SA08**	
[31:12]		20'h0	RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength

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表 4-2: HPSYS_PINMUX 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x24			**PAD_SA09**	
[31:12]		20'h0	RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x28			**PAD_SA10**	
[31:12]		20'h0	RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x2C			**PAD_SA11**	
[31:12]		20'h0	RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x30			**PAD_SA12**	
[31:12]		20'h0	RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h1	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down

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表 4-2: HPSYS_PINMUX 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x34			**PAD_PA00**	
[31:12]		20'h0	RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x38			**PAD_PA01**	
[31:12]		20'h0	RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x3C			**PAD_PA02**	
[31:12]		20'h0	RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x40			**PAD_PA03**	
[31:12]		20'h0	RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x44			**PAD_PA04**	
[31:12]		20'h0	RSVD	

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表 4-2: HPSYS_PINMUX 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x48			**PAD_PA05**	
[31:12]		20'h0	RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x4C			**PAD_PA06**	
[31:12]		20'h0	RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x50			**PAD_PA07**	
[31:12]		20'h0	RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x54			**PAD_PA08**	
[31:12]		20'h0	RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate

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表 4-2: HPSYS_PINMUX 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x58			**PAD_PA09**	
[31:12]		20'h0	RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h1	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x5C			**PAD_PA10**	
[31:12]		20'h0	RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h1	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x60			**PAD_PA11**	
[31:12]		20'h0	RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x64			**PAD_PA12**	
[31:12]		20'h0	RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h1	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device

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表 4-2: HPSYS_PINMUX 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[3:0]	rw	4'h0	FSEL	Function Select
0x68			**PAD_PA13**	
[31:12]		20'h0	RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x6C			**PAD_PA14**	
[31:12]		20'h0	RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x70			**PAD_PA15**	
[31:12]		20'h0	RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x74			**PAD_PA16**	
[31:12]		20'h0	RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x78			**PAD_PA17**	
[31:12]		20'h0	RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW

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表 4-2: HPSYS_PINMUX 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h1	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x7C			**PAD_PA18**	
[31:12]		20'h0	RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h1	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x80			**PAD_PA19**	
[31:12]		20'h0	RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x84			**PAD_PA20**	
[31:12]		20'h0	RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x88			**PAD_PA21**	
[31:12]		20'h0	RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input

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表 4-2: HPSYS_PINMUX 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x8C			**PAD_PA22**	
[31:12]		20'h0	RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h0	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h0	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x90			**PAD_PA23**	
[31:12]		20'h0	RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h0	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h0	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x94			**PAD_PA24**	
[31:12]		20'h0	RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x98			**PAD_PA25**	
[31:12]		20'h0	RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select

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表 4-2: HPSYS_PINMUX 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
0x9C			**PAD_PA26**	
[31:12]		20'h0	RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0xA0			**PAD_PA27**	
[31:12]		20'h0	RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h1	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0xA4			**PAD_PA28**	
[31:12]		20'h0	RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h1	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0xA8			**PAD_PA29**	
[31:12]		20'h0	RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h1	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0xAC			**PAD_PA30**	
[31:12]		20'h0	RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength

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表 4-2: HPSYS_PINMUX 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0xB0			**PAD_PA31**	
[31:12]		20'h0	RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0xB4			**PAD_PA32**	
[31:12]		20'h0	RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0xB8			**PAD_PA33**	
[31:12]		20'h0	RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0xBC			**PAD_PA34**	
[31:12]		20'h0	RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer

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表 4-2: HPSYS_PINMUX 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[5]	rw	1'h1	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0xC0			**PAD_PA35**	
[31:12]		20'h0	RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0xC4			**PAD_PA36**	
[31:12]		20'h0	RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h1	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0xC8			**PAD_PA37**	
[31:12]		20'h0	RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0xCC			**PAD_PA38**	
[31:12]		20'h0	RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0xD0			**PAD_PA39**	

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表 4-2: HPSYS_PINMUX 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:12]		20'h0	RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS	Drive Select. Logic LOW selects 4mA drive,logic HIGH selects 20mA drive
[9]		1'b0	RSVD	
[8]	rw	1'h0	MODE	Mode Select. Logic LOW enables GPIO mode,logic HIGH enables I2C mode
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0xD4			**PAD_PA40**	
[31:12]		20'h0	RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS	Drive Select. Logic LOW selects 4mA drive,logic HIGH selects 20mA drive
[9]		1'b0	RSVD	
[8]	rw	1'h0	MODE	Mode Select. Logic LOW enables GPIO mode,logic HIGH enables I2C mode
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0xD8			**PAD_PA41**	
[31:12]		20'h0	RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS	Drive Select. Logic LOW selects 4mA drive,logic HIGH selects 20mA drive
[9]		1'b0	RSVD	
[8]	rw	1'h0	MODE	Mode Select. Logic LOW enables GPIO mode,logic HIGH enables I2C mode
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0xDC			**PAD_PA42**	
[31:12]		20'h0	RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS	Drive Select. Logic LOW selects 4mA drive,logic HIGH selects 20mA drive
[9]		1'b0	RSVD	
[8]	rw	1'h0	MODE	Mode Select. Logic LOW enables GPIO mode,logic HIGH enables I2C mode
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0xE0			**PAD_PA43**	
[31:12]		20'h0	RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength

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表 4-2: HPSYS_PINMUX 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0xE4			**PAD_PA44**	
[31:12]		20'h0	RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select

4.9 HPSYS_CFG 寄存器

表 4-3: HPSYS_CFG 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00			**BMR**	**Boot Mode Register**
[31:1]		31'h0	RSVD	
[0]	r	1'h0	BOOT_MODE	0 - normal mode, 1 - download mode
0x04			**IDR**	**ID Register**
[31:24]	r	8'hC2	SID	Series ID
[23:16]	r	8'h04	CID	Chip ID
[15:8]	r	8'h0	PID	Package ID
[7:0]	r	8'h0	REVID	Revision ID
0x10			**SYSCR**	**System Configure Register**
[31:3]		29'h0	RSVD	
[2]	rw	1'h0	LDO_VSEL	select work mode 0: D0/D1 1: S0/S1
[1]	rw	1'h0	SDNAND	If set to 1, MPI2 memory space is allocated to SDMMC1
[0]	rw	1'h0	WDT1_REBOOT	If set to 1, WDT1 reset will reboot the whole chip
0x14			**RTC_TR**	**RTC Time Register**
[31]	r	1'h0	PM	
[30:29]	r	2'h0	HT	
[28:25]	r	4'h0	HU	
[24:22]	r	3'h0	MNT	
[21:18]	r	4'h0	MNU	
[17:15]	r	3'h0	ST	
[14:11]	r	4'h0	SU	
[10]		1'h0	RSVD	

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表 4-3: HPSYS_CFG 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[9:0]	r	10'h0	SS	
0x18			**RTC_DR**	**RTC Date Register**
[31]	r	1'h0	ERR	
[30:25]		6'h0	RSVD	
[24]	r	1'h0	CB	
[23:20]	r	4'h0	YT	
[19:16]	r	4'h0	YU	
[15:13]	r	3'h1	WD	
[12]	r	1'h0	MT	
[11:8]	r	4'h1	MU	
[7:6]		2'h0	RSVD	
[5:4]	r	2'h0	DT	
[3:0]	r	4'h1	DU	
0x48			**I2C1_PINR**	**I2C1 Pin Register**
[31:14]		18'h0	RSVD	
[13:8]	rw	6'h3f	SDA_PIN	
[7:6]		2'h0	RSVD	
[5:0]	rw	6'h3f	SCL_PIN	select PA. 0 for PA00, 44 for PA44.
0x4C			**I2C2_PINR**	**I2C2 Pin Register**
[31:14]		18'h0	RSVD	
[13:8]	rw	6'h3f	SDA_PIN	
[7:6]		2'h0	RSVD	
[5:0]	rw	6'h3f	SCL_PIN	
0x50			**I2C3_PINR**	**I2C3 Pin Register**
[31:14]		18'h0	RSVD	
[13:8]	rw	6'h3f	SDA_PIN	
[7:6]		2'h0	RSVD	
[5:0]	rw	6'h3f	SCL_PIN	
0x54			**I2C4_PINR**	**I2C4 Pin Register**
[31:14]		18'h0	RSVD	
[13:8]	rw	6'h3f	SDA_PIN	
[7:6]		2'h0	RSVD	
[5:0]	rw	6'h3f	SCL_PIN	
0x58			**USART1_PINR**	**USART1 Pin Register**
[31:30]		2'h0	RSVD	
[29:24]	rw	6'h3f	CTS_PIN	
[23:22]		2'h0	RSVD	
[21:16]	rw	6'h3f	RTS_PIN	
[15:14]		2'h0	RSVD	
[13:8]	rw	6'd18	RXD_PIN	
[7:6]		2'h0	RSVD	
[5:0]	rw	6'd19	TXD_PIN	
0x5C			**USART2_PINR**	**USART2 Pin Register**
[31:30]		2'h0	RSVD	
[29:24]	rw	6'h3f	CTS_PIN	
[23:22]		2'h0	RSVD	
[21:16]	rw	6'h3f	RTS_PIN	
[15:14]		2'h0	RSVD	

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表 4-3: HPSYS_CFG 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[13:8]	rw	6'h3f	RXD_PIN	
[7:6]		2'h0	RSVD	
[5:0]	rw	6'h3f	TXD_PIN	
0x60			**USART3_PINR**	**USART3 Pin Register**
[31:30]		2'h0	RSVD	
[29:24]	rw	6'h3f	CTS_PIN	
[23:22]		2'h0	RSVD	
[21:16]	rw	6'h3f	RTS_PIN	
[15:14]		2'h0	RSVD	
[13:8]	rw	6'h3f	RXD_PIN	
[7:6]		2'h0	RSVD	
[5:0]	rw	6'h3f	TXD_PIN	
0x64			**GPTIM1_PINR**	**GPTIM1 Pin Register**
[31:30]		2'b0	RSVD	
[29:24]	rw	6'h3f	CH4_PIN	
[23:22]		2'b0	RSVD	
[21:16]	rw	6'h3f	CH3_PIN	
[15:14]		2'b0	RSVD	
[13:8]	rw	6'h3f	CH2_PIN	
[7:6]		2'b0	RSVD	
[5:0]	rw	6'h3f	CH1_PIN	
0x68			**GPTIM2_PINR**	**GPTIM2 Pin Register**
[31:30]		2'b0	RSVD	
[29:24]	rw	6'h3f	CH4_PIN	
[23:22]		2'b0	RSVD	
[21:16]	rw	6'h3f	CH3_PIN	
[15:14]		2'b0	RSVD	
[13:8]	rw	6'h3f	CH2_PIN	
[7:6]		2'b0	RSVD	
[5:0]	rw	6'h3f	CH1_PIN	
0x6C			**ETR_PINR**	**GPTIM ETR Pin Register**
[31:14]		18'b0	RSVD	
[13:8]	rw	6'h3f	ETR2_PIN	GPTIM2_ETR
[7:6]		2'b0	RSVD	
[5:0]	rw	6'h3f	ETR1_PIN	GPTIM1_ETR
0x70			**LPTIM1_PINR**	**LPTIM1 Pin Register**
[31:22]		10'h0	RSVD	
[21:16]	rw	6'h3f	ETR_PIN	
[15:14]		2'b0	RSVD	
[13:8]	rw	6'h3f	OUT_PIN	
[7:6]		2'b0	RSVD	
[5:0]	rw	6'h3f	IN_PIN	
0x74			**LPTIM2_PINR**	**LPTIM2 Pin Register**
[31:22]		10'h0	RSVD	
[21:16]	rw	6'h3f	ETR_PIN	
[15:14]		2'b0	RSVD	
[13:8]	rw	6'h3f	OUT_PIN	
[7:6]		2'b0	RSVD	

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表 4-3: HPSYS_CFG 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[5:0]	rw	6'h3f	IN_PIN	
0x78			**ATIM1_PINR1**	**ATIM1 Pin Register 1**
[31:30]		2'b0	RSVD	
[29:24]	rw	6'h3f	CH4_PIN	
[23:22]		2'b0	RSVD	
[21:16]	rw	6'h3f	CH3_PIN	
[15:14]		2'b0	RSVD	
[13:8]	rw	6'h3f	CH2_PIN	
[7:6]		2'b0	RSVD	
[5:0]	rw	6'h3f	CH1_PIN	
0x7C			**ATIM1_PINR2**	**ATIM1 Pin Register 2**
[31:22]		10'b0	RSVD	
[21:16]	rw	6'h3f	CH3N_PIN	
[15:14]		2'b0	RSVD	
[13:8]	rw	6'h3f	CH2N_PIN	
[7:6]		2'b0	RSVD	
[5:0]	rw	6'h3f	CH1N_PIN	
0x80			**ATIM1_PINR3**	**ATIM1 Pin Register 3**
[31:22]		10'b0	RSVD	
[21:16]	rw	6'h3f	ETR_PIN	
[15:14]		2'b0	RSVD	
[13:8]	rw	6'h3f	BK2_PIN	
[7:6]		2'b0	RSVD	
[5:0]	rw	6'h3f	BK_PIN	

4.10 HPSYS_GPIO 寄存器

表 4-4: HPSYS_GPIO 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00			**DIR0**	**Data Input Register**
[31:0]	r	32'h0	IN	GPIO[31:0] input value
0x04			**DOR0**	**Data Output Register**
[31:0]	rw	32'h0	OUT	GPIO[31:0] output value if output enabled
0x08			**DOSR0**	**Data Output Set Register**
[31:0]	w	32'h0	DOS	set 1 to pull up output of corresponding GPIO[31:0]
0x0C			**DOCR0**	**Data Output Clear Register**
[31:0]	w	32'h0	DOC	set 1 to pull down output of corresponding GPIO[31:0]
0x10			**DOER0**	**Data Output Enable Register**
[31:0]	rw	32'h0	DOE	GPIO[31:0] output enable
0x14			**DOESR0**	**Data Output Enable Set Register**
[31:0]	w	32'h0	DOES	set 1 to enable output of corresponding GPIO[31:0]
0x18			**DOECR0**	**Data Output Enable Clear Register**
[31:0]	w	32'h0	DOEC	set 1 to disable output of corresponding GPIO[31:0]
0x1C			**IER0**	**Interrupt Enable Register**
[31:0]	rw	32'h0	IER	GPIO[31:0] interrupt enable
0x20			**IESR0**	**Interrupt Enable Set Register**

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表 4-4: HPSYS_GPIO 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:0]	w	32'h0	IES	set 1 to enable interrupt of corresponding GPIO[31:0]
0x24			**IECR0**	**Interrupt Enable Clear Register**
[31:0]	w	32'h0	IEC	set 1 to disable interrupt of corresponding GPIO[31:0]
0x28			**ITR0**	**Interrupt Type Register**
[31:0]	rw	32'h0	ITR	GPIO[31:0] interrupt type
0x2C			**ITSR0**	**Interrupt Type Set Register**
[31:0]	w	32'h0	ITS	set 1 for edge-sensitive interrupt mode of corresponding GPIO[31:0]
0x30			**ITCR0**	**Interrupt Type Clear Register**
[31:0]	w	32'h0	ITC	set 1 for level-sensitive interrupt mode of corresponding GPIO[31:0]
0x34			**IPHR0**	**Interrupt Polarity High Register**
[31:0]	rw	32'h0	IPH	rising edge in edge mode, or high level in level mode of corresponding GPIO[31:0]
0x38			**IPHSR0**	**Interrupt Polarity High Set Register**
[31:0]	w	32'h0	IPHS	set 1 for rising edge in edge mode, or high level in level mode of corresponding GPIO[31:0]
0x3C			**IPHCR0**	**Interrupt Polarity High Clear Register**
[31:0]	w	32'h0	IPHC	set 1 for disable rising edge in edge mode, or high level in level mode of corresponding GPIO[31:0]
0x40			**IPLR0**	**Interrupt Polarity Low Register**
[31:0]	rw	32'h0	IPL	falling edge in edge mode, or low level in level mode of corresponding GPIO[31:0]
0x44			**IPLSR0**	**Interrupt Polarity Low Set Register**
[31:0]	w	32'h0	IPLS	set 1 for falling edge in edge mode, or low level in level mode of corresponding GPIO[31:0]
0x48			**IPLCR0**	**Interrupt Polarity Low Clear Register**
[31:0]	w	32'h0	IPLC	set 1 for disable falling edge in edge mode, or low level in level mode of corresponding GPIO[31:0]
0x4C			**ISR0**	**Interrupt Status Register**
[31:0]	rw	32'h0	IS	Interrupt status. Write 1 will clear interrupt status of corresponding GPIO[31:0]
0x60			**OEMR0**	**output mode Register**
[31:0]	rw	32'h0	OEM	output mode of corresponding GPIO[31:0]
0x64			**OEMSR0**	**output mode Set Register**
[31:0]	w	32'h0	OEMS	output mode Set of corresponding GPIO[31:0]
0x68			**OEMCR0**	**output mode Clear Register**
[31:0]	w	32'h0	OEMC	output mode Clear of corresponding GPIO[31:0]
0x80			**DIR1**	**Data Input Register**
[31:13]		19'h0	RSVD	
[12:0]	r	13'h0	IN	GPIO[44:32] input value
0x84			**DOR1**	**Data Output Register**
[31:13]		19'h0	RSVD	
[12:0]	rw	13'h0	OUT	GPIO[44:32] output value if output enabled
0x88			**DOSR1**	**Data Output Set Register**
[31:13]		19'h0	RSVD	
[12:0]	w	13'h0	DOS	set 1 to pull up output of corresponding GPIO[44:32]
0x8C			**DOCR1**	**Data Output Clear Register**
[31:13]		19'h0	RSVD	
[12:0]	w	13'h0	DOC	set 1 to pull down output of corresponding GPIO[44:32]
0x90			**DOER1**	**Data Output Enable Register**
[31:13]		19'h0	RSVD	
[12:0]	rw	13'h0	DOE	GPIO[44:32] output enable

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表 4-4: HPSYS_GPIO 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
0x94			**DOESR1**	**Data Output Enable Set Register**
[31:13]		19'h0	RSVD	
[12:0]	w	13'h0	DOES	set 1 to enable output of corresponding GPIO[44:32]
0x98			**DOECR1**	**Data Output Enable Clear Register**
[31:13]		19'h0	RSVD	
[12:0]	w	13'h0	DOEC	set 1 to disable output of corresponding GPIO[44:32]
0x9C			**IER1**	**Interrupt Enable Register**
[31:13]		19'h0	RSVD	
[12:0]	rw	13'h0	IER	GPIO[44:32] interrupt enable
0xA0			**IESR1**	**Interrupt Enable Set Register**
[31:13]		19'h0	RSVD	
[12:0]	w	13'h0	IES	set 1 to enable interrupt of corresponding GPIO[44:32]
0xA4			**IECR1**	**Interrupt Enable Clear Register**
[31:13]		19'h0	RSVD	
[12:0]	w	13'h0	IEC	set 1 to disable interrupt of corresponding GPIO[44:32]
0xA8			**ITR1**	**Interrupt Type Register**
[31:13]		19'h0	RSVD	
[12:0]	rw	13'h0	ITR	GPIO[44:32] interrupt type
0xAC			**ITSR1**	**Interrupt Type Set Register**
[31:13]		19'h0	RSVD	
[12:0]	w	13'h0	ITS	set 1 for edge-sensitive interrupt mode of corresponding GPIO[44:32]
0xB0			**ITCR1**	**Interrupt Type Clear Register**
[31:13]		19'h0	RSVD	
[12:0]	w	13'h0	ITC	set 1 for level-sensitive interrupt mode of corresponding GPIO[44:32]
0xB4			**IPHR1**	**Interrupt Polarity High Register**
[31:13]		19'h0	RSVD	
[12:0]	rw	13'h0	IPH	rising edge in edge mode, or high level in level mode of corresponding GPIO[44:32]
0xB8			**IPHSR1**	**Interrupt Polarity High Set Register**
[31:13]		19'h0	RSVD	
[12:0]	w	13'h0	IPHS	set 1 for rising edge in edge mode, or high level in level mode of corresponding GPIO[44:32]
0xBC			**IPHCR1**	**Interrupt Polarity High Clear Register**
[31:13]		19'h0	RSVD	
[12:0]	w	13'h0	IPHC	set 1 for disable rising edge in edge mode, or high level in level mode of corresponding GPIO[44:32]
0xC0			**IPLR1**	**Interrupt Polarity Low Register**
[31:13]		19'h0	RSVD	
[12:0]	rw	13'h0	IPL	falling edge in edge mode, or low level in level mode of corresponding GPIO[44:32]
0xC4			**IPLSR1**	**Interrupt Polarity Low Set Register**
[31:13]		19'h0	RSVD	
[12:0]	w	13'h0	IPLS	set 1 for falling edge in edge mode, or low level in level mode of corresponding GPIO[44:32]
0xC8			**IPLCR1**	**Interrupt Polarity Low Clear Register**
[31:13]		19'h0	RSVD	
[12:0]	w	13'h0	IPLC	set 1 for disable falling edge in edge mode, or low level in level mode of corresponding GPIO[44:32]

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表 4-4: HPSYS_GPIO 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
0xCC			**ISR1**	**Interrupt Status Register**
[31:13]		19'h0	RSVD	
[12:0]	rw	13'h0	IS	Interrupt status. Write 1 will clear interrupt status of corresponding GPIO[44:32]
0xE0			**OEMR1**	**output mode Register**
[31:13]		19'h0	RSVD	
[12:0]	rw	13'h0	OEM	output mode of corresponding GPIO[44:32]
0xE4			**OEMSR1**	**output mode Set Register**
[31:13]		19'h0	RSVD	
[12:0]	w	13'h0	OEMS	output mode Set of corresponding GPIO[44:32]
0xE8			**OEMCR1**	**output mode Clear Register**
[31:13]		19'h0	RSVD	
[12:0]	w	13'h0	OEMC	output mode Clear of corresponding GPIO[44:32]

5 DMA

5.1 DMAC

5.1.1 简介

DMAC(Direct Memory Access Controller) 用于实现总线上两个不同地址区间内数据的搬运工作。DMAC 共有 8 个独立通道，每个通道可配置源地址区间与目标地址区间，分别映射到各存储器或外设的地址范围内，从而实现存储器-存储器，存储器-外设，外设-存储器，外设-外设之间的高效率传输，有效缓解 CPU 的工作量。DMAC 支持外设响应模式和存储器搬运模式：在外设响应模式下，DMAC 基于外设的 DMA 请求进行搬运，从而适配外设的带宽；在存储器搬运模式下，DMAC 不等待外设的 DMA 请求，尽快完成数据搬运。当多个通道同时使能时，DMAC 依照优先级由高至低的次序依次搬运；并且在较低优先级的通道搬运过程中，较高优先级的通道能够进行抢占搬运。每个通道传输过半或完成时，能够产生中断或 PTC 触发。

5.1.2 主要特性

- 单 AHB 主控总线，可访问 SRAM，PSRAM，FLASH，AHB 和 APB 外设等
- 8 个独立的可配置通道
- 每个通道的 DMA 请求可在至多 64 个外设 DMA 请求中选择 1 个，或由软件请求
- 每个通道支持 4 档优先级配置，优先级相同时依照通道编号大小判决
- 支持外设到存储器、存储器到外设、存储器到存储器以及外设到外设的数据传输
- 源地址和目标地址均独立支持单字节、双字节、四字节访问。源和目标的地址必须根据传输数据单元的大小进行对齐，并支持地址自动递增
- 单次传输单元数可配置为 0 到 65535
- 支持循环缓冲模式，单次传输完成后自动重新启动
- 每个通道支持 3 种事件标志：传输完成、过半传输或传输错误，并能独立生成中断请求及 PTC 触发
- 每个通道支持可配置块尺寸的块传输模式

5.1.3 外设请求

每个通道通过配置 CSELR1/2_CxS 可在 64 个外设请求源中选择任意一个作为该通道的绑定请求源，该外设的应答信号也相应绑定到该通道上。DMAC 的外设请求表如下。

表 5-1: DMAC 外设请求表

CSELR1/2_CxS	DMAC1
0	mpi1
1	mpi2
2	/
3	i2c4
4	usart1_tx
5	usart1_rx

续表下页...

表 5-1: DMAC 外设请求表（续）

CSELR1/2_CxS	DMAC1
6	usart2_tx
7	usart2_rx
8	gptim1_update
9	gptim1_trigger
10	gptim1_cc1
11	gptim1_cc2
12	gptim1_cc3
13	gptim1_cc4
14	btim1
15	btim2
16	atim1_update
17	atim1_trigger
18	atim1_cc1
19	atim1_cc2
20	atim1_cc3
21	atim1_cc4
22	i2c1
23	i2c2
24	i2c3
25	atim1_com
26	usart3_tx
27	usart3_rx
28	spi1_tx
29	spi1_rx
30	spi2_tx
31	spi2_rx
32	i2s1_tx
33	i2s1_rx
34	/
35	/
36	pdm1_l
37	pdm1_r
38	gpadc
39	audadc_ch0
40	audadc_ch1
41	auddac_ch0
42	auddac_ch1
43	gptim2_update
44	gptim2_trigger
45	gptim2_cc1
46	audprc_tx_out_ch1
47	audprc_tx_out_ch0
48	audprc_tx_ch3
49	audprc_tx_ch2
50	audprc_tx_ch1
51	audprc_tx_ch0
52	audprc_rx_ch1
53	audprc_rx_ch0

续表下页...

表 5-1: DMAC 外设请求表（续）

CSELR1/2_CxS	DMAC1
54	gptim2_cc2
55	gptim2_cc3
56	gptim2_cc4
57	sdmmc1
58	/
59	/
60	/
61	/
62	/
63	/

5.1.4 DMAC 功能描述

5.1.4.1 DMAC 结构图

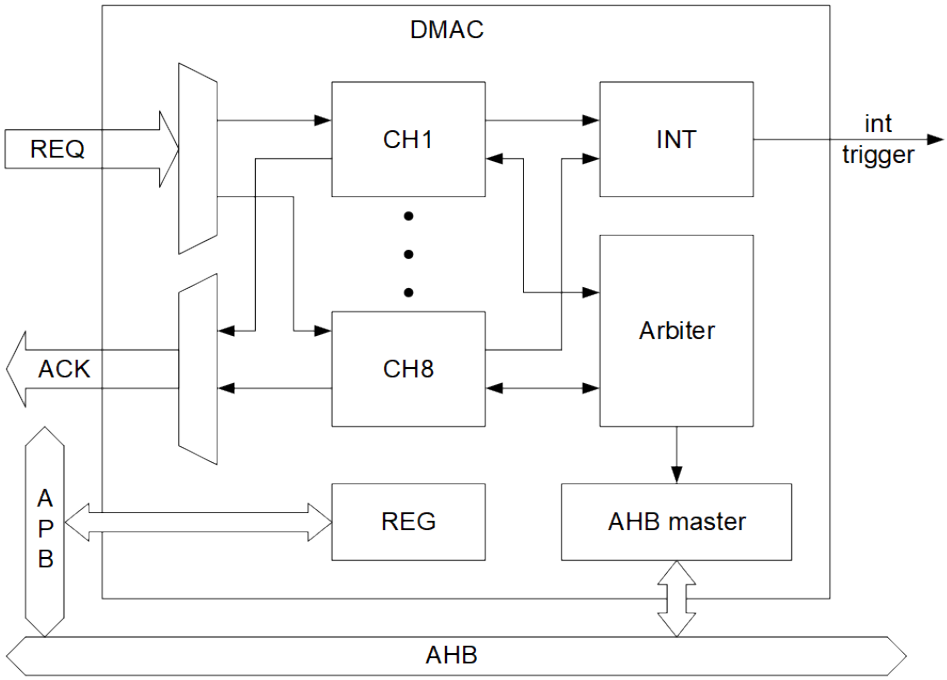

图 5-1: DMAC 结构图

5.1.4.2 传输效率

DMAC 和 CPU 及其它主控设备共享 AHB 总线。当 CPU 和 DMAC 同时访问相同的目标（存储器或外设）时，DMAC 请求可能会暂停 CPU 访问系统总线，由总线仲裁器执行循环调度，以保证 CPU 至少可以得到一半的总线带宽。同理，当其它主控设备与 DMAC 访问相同 AHB 目标时，DMAC 访问带宽也会下降。当总线没有其它访问时，DMAC 完成一笔单元传输最快需要 2 个 HCLK 周期，具体取决于访问目标的 AHB 等待周期。

5.1.4.3 传输模式

DMAC 的每个通道可独立配置为外设传输模式或存储器传输模式，由 CCRx_MEM2MEM 寄存器控制，主要区别在于是否启用外设请求/应答机制。外设传输模式通过请求/应答机制适配外设的数据带宽，仅在外设准备好了以后才发起传输，通常用于 UART 收发、I2S 音频输入输出、FLASH 烧写等场景。存储器传输模式不需等待请求信号，将以最大可能的数据带宽进行传输，通常用于 SRAM 搬运、CRC 校验等场景。

5.1.4.4 传输流程

外设传输模式下，DMAC 传输使用外设请求/应答机制，传输由外设请求发起，按照以下步骤进行传输：

1. 外设在需要传输数据时（如接收缓存满，或发送缓存空），向 DMAC 相关通道发送请求信号；
2. DMAC 按照相关通道的优先级来处理该请求，当该通道优先级为所有请求通道中最高时，启动该通道的单元传输或块传输；
3. 单元传输或块传输完成后，DMAC 向外设发送应答信号；
4. 外设获得 DMAC 的应答信号后，便会释放请求；
5. 检测到外设请求释放后，DMAC 就会释放应答信号；
6. 外设检测到应答信号释放后，如还有传输需求，可继续发送请求，再次启动 DMAC 单元传输或块传输。

存储器传输模式下，传输由软件发起，并当该通道优先级足够时，重复进行单元传输直至传输完成。

5.1.4.5 传输使能

DMAC 的 8 个通道独立使能。当 CCRx_EN 为 1 且 CNDTRx 不为 0 时，通道传输启动，在外设传输模式下开始响应外设请求，在存储器传输模式下立即开始传输。需要注意当通道使能时，即使上一笔传输已经完成，重新写入非 0 的 CNDTRx 也会立刻启动 DMAC 传输，在此之前应当确保其它参数已经配置完毕，或者在写入 CNDTRx 时保证 CCRx_EN 为 0。

5.1.4.6 传输单元

DMAC 传输的基本单位是一个传输单元，包括 3 个步骤：

1. 通过总线单次读取源地址数据，单字节/双字节/四字节可配置；
2. 将读取到的数据单次写入目标地址，单字节/双字节/四字节可配置；
3. 更新计数，根据计数结果停止传输，或计算下一次传输的地址。

5.1.4.7 传输数量

DMAC 每个通道传输的数量由 CNDTRx 控制，以传输单元计数，支持范围 0~65535。例如配置为四字节传输，则通道单次传输最大数据量为 65535×4=262140 字节。配置 CNDTRx 并启动单元传输 (CCRx_EN=1) 后，每完成一个传输单元，CNDTRx 寄存器值减 1。非循环模式下 (CCRx_CIRC=0)，CNDTRx 减到 0 就会停止传输。循环模式下 (CCRx_CIRC=1)，CNDTRx 减到 0 后会立即重新加载软件配置的初始值，并继续传输。

5.1.4.8 循环模式

循环模式下，传输不会自动停止。在循环模式下，最后一次数据传输完成后，CNDTRx 寄存器将自动重新加载初始编程值。当前的内部地址寄存器重新加载 CPARx 和 CM0ARx 寄存器中的基址值。循环模式下通过判断过半传输与传输完成标志，能够实现乒乓缓存的功能。

5.1.4.9 传输方向

DMAC 的传输方向由 CCRx_DIR 决定。

表 5-2: DMAC 传输方向

	源起始地址 (读)	目标起始地址 (写)
DIR=0	CPARx	CM0ARx
DIR=1	CM0ARx	CPARx

5.1.4.10 传输位宽

DMAC 传输时，对总线源地址和目标地址的访问可独立通过 CCRx_MSIZE 和 CCRx_PSIZE 配置为单字节/双字节/四字节类型。DMAC 不提供数据打包和拆分的功能，因此当源地址和目标地址访问数据位宽不一致时，数据会有截取或补偿，基于下表示例

表 5-3: DMAC 传输位宽

Source Size	Destination Size	Source Data	Destination Data
byte	byte	0xB0 @0x0 0xB1 @0x1 0xB2 @0x2 0xB3 @0x3	0xB0 @0x0 0xB1 @0x1 0xB2 @0x2 0xB3 @0x3
byte	half-word(16bit)	0xB0 @0x0 0xB1 @0x1 0xB2 @0x2 0xB3 @0x3	0x00B0 @0x0 0x00B1 @0x2 0x00B2 @0x4 0x00B3 @0x6
byte	word(32bit)	0xB0 @0x0 0xB1 @0x1 0xB2 @0x2 0xB3 @0x3	0x000000B0 @0x0 0x000000B1 @0x4 0x000000B2 @0x8 0x000000B3 @0xC
half-word	byte	0xB1B0 @0x0 0xB3B2 @0x2 0xB4B4 @0x4 0xB7B6 @0x6	0xB0 @0x0 0xB2 @0x1 0xB4 @0x2 0xB6 @0x3
half-word	half-word	0xB1B0 @0x0 0xB3B2 @0x2 0xB4B4 @0x4 0xB7B6 @0x6	0xB1B0 @0x0 0xB3B2 @0x2 0xB4B4 @0x4 0xB7B6 @0x6
half-word	word	0xB1B0 @0x0 0xB3B2 @0x2 0xB4B4 @0x4 0xB7B6 @0x6	0x0000B1B0 @0x0 0x0000B3B2 @0x4 0x0000B5B4 @0x8 0x0000B7B6 @0xC
word	byte	0xB3B2B1B0 @0x0 0xB7B6B5B4 @0x4 0xBBBAB9B8 @0x8 0xBFBEBDBC @0xC	0xB0 @0x0 0xB4 @0x1 0xB8 @0x2 0xBC @0x3
word	half-word	0xB3B2B1B0 @0x0 0xB7B6B5B4 @0x4 0xBBBAB9B8 @0x8 0xBFBEBDBC @0xC	0xB1B0 @0x0 0xB5B4 @0x2 0xB9B8 @0x4 0xBDBC @0x6

续表下页...

表 5-3: DMAC 传输位宽（续）

Source Size	Destination Size	Source Data	Destination Data
word	word	0xB3B2B1B0 @0x0	0xB3B2B1B0 @0x0
		0xB7B6B5B4 @0x4	0xB7B6B5B4 @0x4
		0xBBBAB9B8 @0x8	0xBBBAB9B8 @0x8
		0xBFBEBDBC @0xC	0xBFBEBDBC @0xC

5.1.4.11 传输地址

传输的起始源地址和目标地址由 CPARx，CM0ARx 以及 CCRx_DIR 决定。如果使能了递增模式（CCRx_MINC 和 CCRx_PINC 独立配置），每完成一笔单元传输，则下次传输的地址是前一次传输的地址加上 1、2 或 4（与传输的位宽一致）。

在传输过程中，这些寄存器将保持初始编程的值。软件无法获得当前正在传输的地址。通常外设 FIFO 的传输地址配置为不递增，而存储器的传输地址配置为递增。

5.1.4.12 通道仲裁

DMAC 仲裁器管理不同通道间的优先级。当仲裁器为某个有效通道授予优先权后（硬件请求或软件触发），会发起该通道的单元传输或块传输。随后仲裁器会再次对有效通道进行仲裁，并选择优先级最高的通道。

仲裁器基于如下准则判断优先级：

1. 外设传输模式的通道优先于存储器传输模式的通道
2. 同为外设传输模式或存储器传输模式的，通道 CCRx_PL 低的优先级高
3. 传输模式与 CCRx_PL 均相同的，通道编号小的优先级高 (如通道 1 优先于通道 2)

在某一通道传输过程中，如果有另一更高优先级的通道发出了传输请求，则在当前通道的单元传输或块传输完成后，仲裁器会把传输切换到更高优先级的通道上。

5.1.4.13 块传输

块传输仅在外设传输模式下生效。CBSRx 定义了对于每一笔外设请求，DMAC 要连续完成多少次单元传输。例如 CBSRx 设为 4 时，每当外设发起一笔请求，DMAC 将完成连续 4 次单元传输，之后再给出应答信号，期间 CNDTRx 也将连续减 4。如果剩余待传输的 CNDTRx 小于 CBSRx，则仅传输剩余的 CNDTRx 次单元传输。

5.1.4.14 通知机制

DMAC 每个通道可独立产生中断和 PTC 触发信号，并可单独配置每种中断的使能。通道传输完成至少一半时，产生 HTIFx 中断和触发。通道传输全部完成后，产生 TCIFx 中断和触发。通道传输发生总线访问错误时，产生 TEIFx 中断和触发。以上三种中断任一种发生时，产生 GIFx 中断。通道中断可单独清除，或通过 CGIFx 一并清除。

5.1.4.15 通道配置流程

配置 DMAC 通道时需按照以下步骤操作：

1. 在 CPARx 寄存器中设置外设寄存器地址。
   在外设请求发生后，或在存储器模式下使能通道后，会将数据从该地址移至存储器或从存储器移至该地址。

2. 设置 CM0ARx 寄存器中的存储器地址。
   在外设请求发生后，或在存储器模式下使能通道后，会将数据写入存储器或从存储器读取数据。
3. 确保 CCRx_EN 为 0 时，将待传输的单元数写入 CNDTRx 寄存器。
   每次数据传输后，该值都会递减。
4. 在 CCRx 寄存器中配置下列参数：
   - 通道优先级
   - 数据传输方向
   - 循环模式
   - 外设和存储器递增模式
   - 外设和存储器数据大小
   - 传输完成一半和/或全部完成以及/或者出现传输错误时的中断使能
5. 将 CCRx_EN 置 1 以激活通道。
   通道在使能后可处理来自此通道所连接外设的请求，或者启动存储器到存储器传输。

5.1.4.16 传输完成处理

在非循环模式下，DMAC 某通道传输完成后，CNDTRx 自动归零，软件需将该通道的 CCRx_EN 写 0 以避免下次配置时误触发。如果有中断标志出现，软件应当在进行相应处理后清除中断标志。

循环模式下 DMAC 不会自动停止传输，当软件想要停止传输时，应将该通道的 CCRx_EN 写 0，并清除中断标志。

5.1.5 DMAC 寄存器

表 5-4: DMAC 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00		**0x00000000**	**ISR**	
[31]	r	1'h0	TEIF8	channel transfer error flag
[30]	r	1'h0	HTIF8	channel half transfer flag
[29]	r	1'h0	TCIF8	channel transfer complete flag
[28]	r	1'h0	GIF8	channel global interrupt flag
[27]	r	1'h0	TEIF7	channel transfer error flag
[26]	r	1'h0	HTIF7	channel half transfer flag
[25]	r	1'h0	TCIF7	channel transfer complete flag
[24]	r	1'h0	GIF7	channel global interrupt flag
[23]	r	1'h0	TEIF6	channel transfer error flag
[22]	r	1'h0	HTIF6	channel half transfer flag
[21]	r	1'h0	TCIF6	channel transfer complete flag
[20]	r	1'h0	GIF6	channel global interrupt flag
[19]	r	1'h0	TEIF5	channel transfer error flag
[18]	r	1'h0	HTIF5	channel half transfer flag
[17]	r	1'h0	TCIF5	channel transfer complete flag
[16]	r	1'h0	GIF5	channel global interrupt flag
[15]	r	1'h0	TEIF4	channel transfer error flag
[14]	r	1'h0	HTIF4	channel half transfer flag
[13]	r	1'h0	TCIF4	channel transfer complete flag

续表下页...

表 5-4: DMAC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[12]	r	1'h0	GIF4	channel global interrupt flag
[11]	r	1'h0	TEIF3	channel transfer error flag
[10]	r	1'h0	HTIF3	channel half transfer flag
[9]	r	1'h0	TCIF3	channel transfer complete flag
[8]	r	1'h0	GIF3	channel global interrupt flag
[7]	r	1'h0	TEIF2	channel transfer error flag
[6]	r	1'h0	HTIF2	channel half transfer flag
[5]	r	1'h0	TCIF2	channel transfer complete flag
[4]	r	1'h0	GIF2	channel global interrupt flag
[3]	r	1'h0	TEIF1	channel transfer error flag. Set when bus error detected. Cleared when write 1 to CTEIF or CGIF.
[2]	r	1'h0	HTIF1	channel half transfer flag. Set when half NDT are transferred. Cleared when write 1 to CHTIF or CGIF.
[1]	r	1'h0	TCIF1	channel transfer complete flag. Set when all NDT are transferred. Cleared when write 1 to CTCIF or CGIF.
[0]	r	1'h0	GIF1	channel global interrupt flag. Set when any of TEIF/HTIF/TCIF asserted. Cleared when TEIF/HTIF/TCIF all cleared.
0x04		**0x00000000**	**IFCR**	
[31]	w	1'h0	CTEIF8	CTEIF, transfer error flag clear
[30]	w	1'h0	CHTIF8	CHTIF, half transfer flag clear
[29]	w	1'h0	CTCIF8	CTCIF, transfer complete flag clear
[28]	w	1'h0	CGIF8	CGIF, global interrupt flag clear
[27]	w	1'h0	CTEIF7	CTEIF, transfer error flag clear
[26]	w	1'h0	CHTIF7	CHTIF, half transfer flag clear
[25]	w	1'h0	CTCIF7	CTCIF, transfer complete flag clear
[24]	w	1'h0	CGIF7	CGIF, global interrupt flag clear
[23]	w	1'h0	CTEIF6	CTEIF, transfer error flag clear
[22]	w	1'h0	CHTIF6	CHTIF, half transfer flag clear
[21]	w	1'h0	CTCIF6	CTCIF, transfer complete flag clear
[20]	w	1'h0	CGIF6	CGIF, global interrupt flag clear
[19]	w	1'h0	CTEIF5	CTEIF, transfer error flag clear
[18]	w	1'h0	CHTIF5	CHTIF, half transfer flag clear
[17]	w	1'h0	CTCIF5	CTCIF, transfer complete flag clear
[16]	w	1'h0	CGIF5	CGIF, global interrupt flag clear
[15]	w	1'h0	CTEIF4	CTEIF, transfer error flag clear
[14]	w	1'h0	CHTIF4	CHTIF, half transfer flag clear
[13]	w	1'h0	CTCIF4	CTCIF, transfer complete flag clear
[12]	w	1'h0	CGIF4	CGIF, global interrupt flag clear
[11]	w	1'h0	CTEIF3	CTEIF, transfer error flag clear
[10]	w	1'h0	CHTIF3	CHTIF, half transfer flag clear
[9]	w	1'h0	CTCIF3	CTCIF, transfer complete flag clear
[8]	w	1'h0	CGIF3	CGIF, global interrupt flag clear
[7]	w	1'h0	CTEIF2	CTEIF, transfer error flag clear
[6]	w	1'h0	CHTIF2	CHTIF, half transfer flag clear
[5]	w	1'h0	CTCIF2	CTCIF, transfer complete flag clear
[4]	w	1'h0	CGIF2	CGIF, global interrupt flag clear
[3]	w	1'h0	CTEIF1	CTEIF, transfer error flag clear. Write 1 to clear TEIF.
[2]	w	1'h0	CHTIF1	CHTIF, half transfer flag clear. Write 1 to clear HTIF.

续表下页...

表 5-4: DMAC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[1]	w	1'h0	CTCIF1	CTCIF, transfer complete flag clear. Write 1 to clear TCIF.
[0]	w	1'h0	CGIF1	CGIF, global interrupt flag clear. Write 1 to clear all TEIF/HTIF/TCIF.
0x08		**0x00000000**	**CCR1**	
[31:15]		17'h0	RSVD	
[14]	rw	1'h0	MEM2MEM	memory-to-memory mode 0: disabled 1: enabled
[13:12]	rw	2'h0	PL	priority level 00: low 01: medium 10: high 11: very high
[11:10]	rw	2'h0	MSIZE	memory size Defines the data size of each DMA transfer to the identified memory. In memory-to-memory mode, this field identifies the memory source if DIR = 1 and the memory destination if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral source if DIR = 1 and the peripheral destination if DIR = 0. 00: 8 bits 01: 16 bits 10: 32 bits 11: reserved
[9:8]	rw	2'h0	PSIZE	peripheral size Defines the data size of each DMA transfer to the identified peripheral. In memory-to-memory mode, this field identifies the memory destination if DIR = 1 and the memory source if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral destination if DIR = 1 and the peripheral source if DIR = 0. 00: 8 bits 01: 16 bits 10: 32 bits 11: reserved
[7]	rw	1'h0	MINC	memory increment mode Defines the increment mode for each DMA transfer to the identified memory. In memory-to-memory mode, this field identifies the memory source if DIR = 1 and the memory destination if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral source if DIR = 1 and the peripheral destination if DIR = 0. 0: disabled 1: enabled

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表 5-4: DMAC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[6]	rw	1'h0	PINC	peripheral increment mode Defines the increment mode for each DMA transfer to the identified peripheral. n memory-to-memory mode, this field identifies the memory destination if DIR = 1 and the memory source if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral destination if DIR = 1 and the peripheral source if DIR = 0. 0: disabled 1: enabled
[5]	rw	1'h0	CIRC	circular mode 0: disabled 1: enabled
[4]	rw	1'h0	DIR	data transfer direction This bit must be set only in memory-to-peripheral and peripheral-to-memory modes. 0: read from peripheral –Source attributes are defined by PSIZE and PINC, plus the CPARx register. This is still valid in a memory-to-memory mode. – Destination attributes are defined by MSIZE and MINC, plus the CM0ARx register. This is still valid in a peripheral-to-peripheral mode. 1: read from memory –Destination attributes are defined by PSIZE and PINC, plus the CPARx register. This is still valid in a memory-to-memory mode. –Source attributes are defined by MSIZE and MINC, plus the CM0ARx register. This is still valid in a peripheral-to-peripheral mode.
[3]	rw	1'h0	TEIE	transfer error interrupt enable 0: disabled 1: enabled
[2]	rw	1'h0	HTIE	half transfer interrupt enable 0: disabled 1: enabled
[1]	rw	1'h0	TCIE	transfer complete interrupt enable 0: disabled 1: enabled
[0]	rw	1'h0	EN	channel enable When a channel transfer error occurs, this bit is cleared by hardware. It can not be set again by software (channel x re-activated) until the TEIFx bit of the ISR register is cleared (by setting the CTEIFx bit of the IFCR register). 0: disabled 1: enabled
0x0C		**0x00000000**	**CNDTR1**	
[31:16]		16'h0	RSVD	

续表下页...

表 5-4: DMAC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[15:0]	rw	16'h0	NDT	number of data to transfer (0 to 216 - 1) This field is updated by hardware when the channel is enabled: – It is decremented after each single DMA 'read followed by write' transfer, indicating the remaining amount of data items to transfer. –It is kept at zero when the programmed amount of data to transfer is reached, if the channel is not in circular mode (CIRC = 0 in the CCRx register). –It is reloaded automatically by the previously programmed value, when the transfer is complete, if the channel is in circular mode (CIRC = 1). If this field is zero, no transfer can be served whatever the channel status (enabled or not).
0x10		**0x00000000**	**CPAR1**	
[31:0]	rw	32'h0	PA	peripheral address It contains the base address of the peripheral data register from/to which the data will be read/written. In memory-to-memory mode, this register identifies the memory destination address if DIR = 1 and the memory source address if DIR = 0. In peripheral-to-peripheral mode, this register identifies the peripheral destination address DIR = 1 and the peripheral source address if DIR = 0.
0x14		**0x00000000**	**CM0AR1**	
[31:0]	rw	32'h0	MA	memory address It contains the base address of the memory from/to which the data will be read/written. In memory-to-memory mode, this register identifies the memory source address if DIR = 1 and the memory destination address if DIR = 0. In peripheral-to-peripheral mode, this register identifies the peripheral source address DIR = 1 and the peripheral destination address if DIR = 0.
0x18		**0x00000000**	**CBSR1**	
[31:8]		24'h0	RSVD	
[7:0]	rw	8'h0	BS	burst size in non-m2m mode When BS>1, DMA will transfer for BS times for each request if left NDT is larger than BS, or else transfer for left NDT times. When BS=0 or 1, DMA will always do single transfer for each request. In memory-to-memory mode, BS is ignored.
0x1C		**0x00000000**	**CCR2**	
[31:15]		17'h0	RSVD	
[14]	rw	1'h0	MEM2MEM	memory-to-memory mode 0: disabled 1: enabled
[13:12]	rw	2'h0	PL	priority level 00: low 01: medium 10: high 11: very high

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表 5-4: DMAC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[11:10]	rw	2'h0	MSIZE	memory size Defines the data size of each DMA transfer to the identified memory. In memory-to-memory mode, this field identifies the memory source if DIR = 1 and the memory destination if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral source if DIR = 1 and the peripheral destination if DIR = 0. 00: 8 bits 01: 16 bits 10: 32 bits 11: reserved
[9:8]	rw	2'h0	PSIZE	peripheral size Defines the data size of each DMA transfer to the identified peripheral. In memory-to-memory mode, this field identifies the memory destination if DIR = 1 and the memory source if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral destination if DIR = 1 and the peripheral source if DIR = 0. 00: 8 bits 01: 16 bits 10: 32 bits 11: reserved
[7]	rw	1'h0	MINC	memory increment mode Defines the increment mode for each DMA transfer to the identified memory. In memory-to-memory mode, this field identifies the memory source if DIR = 1 and the memory destination if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral source if DIR = 1 and the peripheral destination if DIR = 0. 0: disabled 1: enabled
[6]	rw	1'h0	PINC	peripheral increment mode Defines the increment mode for each DMA transfer to the identified peripheral. n memory-to-memory mode, this field identifies the memory destination if DIR = 1 and the memory source if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral destination if DIR = 1 and the peripheral source if DIR = 0. 0: disabled 1: enabled
[5]	rw	1'h0	CIRC	circular mode 0: disabled 1: enabled

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表 5-4: DMAC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[4]	rw	1'h0	DIR	data transfer direction This bit must be set only in memory-to-peripheral and peripheral-to-memory modes. 0: read from peripheral –Source attributes are defined by PSIZE and PINC, plus the CPARx register. This is still valid in a memory-to-memory mode. – Destination attributes are defined by MSIZE and MINC, plus the CM0ARx register. This is still valid in a peripheral-to-peripheral mode. 1: read from memory –Destination attributes are defined by PSIZE and PINC, plus the CPARx register. This is still valid in a memory-to-memory mode. –Source attributes are defined by MSIZE and MINC, plus the CM0ARx register. This is still valid in a peripheral-to-peripheral mode.
[3]	rw	1'h0	TEIE	transfer error interrupt enable 0: disabled 1: enabled
[2]	rw	1'h0	HTIE	half transfer interrupt enable 0: disabled 1: enabled
[1]	rw	1'h0	TCIE	transfer complete interrupt enable 0: disabled 1: enabled
[0]	rw	1'h0	EN	channel enable When a channel transfer error occurs, this bit is cleared by hardware. It can not be set again by software (channel x re-activated) until the TEIFx bit of the ISR register is cleared (by setting the CTEIFx bit of the IFCR register). 0: disabled 1: enabled
0x20		**0x00000000**	**CNDTR2**	
[31:16]		16'h0	RSVD	
[15:0]	rw	16'h0	NDT	number of data to transfer (0 to 216 - 1) This field is updated by hardware when the channel is enabled: – It is decremented after each single DMA 'read followed by write' transfer, indicating the remaining amount of data items to transfer. –It is kept at zero when the programmed amount of data to transfer is reached, if the channel is not in circular mode (CIRC = 0 in the CCRx register). –It is reloaded automatically by the previously programmed value, when the transfer is complete, if the channel is in circular mode (CIRC = 1). If this field is zero, no transfer can be served whatever the channel status (enabled or not).
0x24		**0x00000000**	**CPAR2**	
[31:0]	rw	32'h0	PA	peripheral address It contains the base address of the peripheral data register from/to which the data will be read/written. In memory-to-memory mode, this register identifies the memory destination address if DIR = 1 and the memory source address if DIR = 0. In peripheral-to-peripheral mode, this register identifies the peripheral destination address DIR = 1 and the peripheral source address if DIR = 0.
0x28		**0x00000000**	**CM0AR2**	

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表 5-4: DMAC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:0]	rw	32'h0	MA	peripheral address It contains the base address of the memory from/to which the data will be read/written. In memory-to-memory mode, this register identifies the memory source address if DIR = 1 and the memory destination address if DIR = 0. In peripheral-to-peripheral mode, this register identifies the peripheral source address DIR = 1 and the peripheral destination address if DIR = 0.
0x2C		**0x00000000**	**CBSR2**	
[31:8]		24'h0	RSVD	
[7:0]	rw	8'h0	BS	burst size in non-m2m mode When BS>1, DMA will transfer for BS times for each request if left NDT is larger than BS, or else transfer for left NDT times. When BS=0 or 1, DMA will always do single transfer for each request. In memory-to-memory mode, BS is ignored.
0x30		**0x00000000**	**CCR3**	
[31:15]		17'h0	RSVD	
[14]	rw	1'h0	MEM2MEM	memory-to-memory mode 0: disabled 1: enabled
[13:12]	rw	2'h0	PL	priority level 00: low 01: medium 10: high 11: very high
[11:10]	rw	2'h0	MSIZE	memory size Defines the data size of each DMA transfer to the identified memory. In memory-to-memory mode, this field identifies the memory source if DIR = 1 and the memory destination if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral source if DIR = 1 and the peripheral destination if DIR = 0. 00: 8 bits 01: 16 bits 10: 32 bits 11: reserved
[9:8]	rw	2'h0	PSIZE	peripheral size Defines the data size of each DMA transfer to the identified peripheral. In memory-to-memory mode, this field identifies the memory destination if DIR = 1 and the memory source if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral destination if DIR = 1 and the peripheral source if DIR = 0. 00: 8 bits 01: 16 bits 10: 32 bits 11: reserved

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表 5-4: DMAC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[7]	rw	1'h0	MINC	memory increment mode Defines the increment mode for each DMA transfer to the identified memory. In memory-to-memory mode, this field identifies the memory source if DIR = 1 and the memory destination if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral source if DIR = 1 and the peripheral destination if DIR = 0. 0: disabled 1: enabled
[6]	rw	1'h0	PINC	peripheral increment mode Defines the increment mode for each DMA transfer to the identified peripheral. n memory-to-memory mode, this field identifies the memory destination if DIR = 1 and the memory source if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral destination if DIR = 1 and the peripheral source if DIR = 0. 0: disabled 1: enabled
[5]	rw	1'h0	CIRC	circular mode 0: disabled 1: enabled
[4]	rw	1'h0	DIR	data transfer direction This bit must be set only in memory-to-peripheral and peripheral-to-memory modes. 0: read from peripheral –Source attributes are defined by PSIZE and PINC, plus the CPARx register. This is still valid in a memory-to-memory mode. – Destination attributes are defined by MSIZE and MINC, plus the CM0ARx register. This is still valid in a peripheral-to-peripheral mode. 1: read from memory –Destination attributes are defined by PSIZE and PINC, plus the CPARx register. This is still valid in a memory-to-memory mode. –Source attributes are defined by MSIZE and MINC, plus the CM0ARx register. This is still valid in a peripheral-to-peripheral mode.
[3]	rw	1'h0	TEIE	transfer error interrupt enable 0: disabled 1: enabled
[2]	rw	1'h0	HTIE	half transfer interrupt enable 0: disabled 1: enabled
[1]	rw	1'h0	TCIE	transfer complete interrupt enable 0: disabled 1: enabled
[0]	rw	1'h0	EN	channel enable When a channel transfer error occurs, this bit is cleared by hardware. It can not be set again by software (channel x re-activated) until the TEIFx bit of the ISR register is cleared (by setting the CTEIFx bit of the IFCR register). 0: disabled 1: enabled

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表 5-4: DMAC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
0x34		**0x00000000**	**CNDTR3**	
[31:16]		16'h0	RSVD	
[15:0]	rw	16'h0	NDT	number of data to transfer (0 to 216 - 1) This field is updated by hardware when the channel is enabled: – It is decremented after each single DMA 'read followed by write' transfer, indicating the remaining amount of data items to transfer. –It is kept at zero when the programmed amount of data to transfer is reached, if the channel is not in circular mode (CIRC = 0 in the CCRx register). –It is reloaded automatically by the previously programmed value, when the transfer is complete, if the channel is in circular mode (CIRC = 1). If this field is zero, no transfer can be served whatever the channel status (enabled or not).
0x38		**0x00000000**	**CPAR3**	
[31:0]	rw	32'h0	PA	peripheral address It contains the base address of the peripheral data register from/to which the data will be read/written. In memory-to-memory mode, this register identifies the memory destination address if DIR = 1 and the memory source address if DIR = 0. In peripheral-to-peripheral mode, this register identifies the peripheral destination address DIR = 1 and the peripheral source address if DIR = 0.
0x3C		**0x00000000**	**CM0AR3**	
[31:0]	rw	32'h0	MA	peripheral address It contains the base address of the memory from/to which the data will be read/written. In memory-to-memory mode, this register identifies the memory source address if DIR = 1 and the memory destination address if DIR = 0. In peripheral-to-peripheral mode, this register identifies the peripheral source address DIR = 1 and the peripheral destination address if DIR = 0.
0x40		**0x00000000**	**CBSR3**	
[31:8]		24'h0	RSVD	
[7:0]	rw	8'h0	BS	burst size in non-m2m mode When BS>1, DMA will transfer for BS times for each request if left NDT is larger than BS, or else transfer for left NDT times. When BS=0 or 1, DMA will always do single transfer for each request. In memory-to-memory mode, BS is ignored.
0x44		**0x00000000**	**CCR4**	
[31:15]		17'h0	RSVD	
[14]	rw	1'h0	MEM2MEM	memory-to-memory mode 0: disabled 1: enabled
[13:12]	rw	2'h0	PL	priority level 00: low 01: medium 10: high 11: very high

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表 5-4: DMAC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[11:10]	rw	2'h0	MSIZE	memory size Defines the data size of each DMA transfer to the identified memory. In memory-to-memory mode, this field identifies the memory source if DIR = 1 and the memory destination if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral source if DIR = 1 and the peripheral destination if DIR = 0. 00: 8 bits 01: 16 bits 10: 32 bits 11: reserved
[9:8]	rw	2'h0	PSIZE	peripheral size Defines the data size of each DMA transfer to the identified peripheral. In memory-to-memory mode, this field identifies the memory destination if DIR = 1 and the memory source if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral destination if DIR = 1 and the peripheral source if DIR = 0. 00: 8 bits 01: 16 bits 10: 32 bits 11: reserved
[7]	rw	1'h0	MINC	memory increment mode Defines the increment mode for each DMA transfer to the identified memory. In memory-to-memory mode, this field identifies the memory source if DIR = 1 and the memory destination if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral source if DIR = 1 and the peripheral destination if DIR = 0. 0: disabled 1: enabled
[6]	rw	1'h0	PINC	peripheral increment mode Defines the increment mode for each DMA transfer to the identified peripheral. n memory-to-memory mode, this field identifies the memory destination if DIR = 1 and the memory source if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral destination if DIR = 1 and the peripheral source if DIR = 0. 0: disabled 1: enabled
[5]	rw	1'h0	CIRC	circular mode 0: disabled 1: enabled

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表 5-4: DMAC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[4]	rw	1'h0	DIR	data transfer direction This bit must be set only in memory-to-peripheral and peripheral-to-memory modes. 0: read from peripheral –Source attributes are defined by PSIZE and PINC, plus the CPARx register. This is still valid in a memory-to-memory mode. – Destination attributes are defined by MSIZE and MINC, plus the CM0ARx register. This is still valid in a peripheral-to-peripheral mode. 1: read from memory –Destination attributes are defined by PSIZE and PINC, plus the CPARx register. This is still valid in a memory-to-memory mode. –Source attributes are defined by MSIZE and MINC, plus the CM0ARx register. This is still valid in a peripheral-to-peripheral mode.
[3]	rw	1'h0	TEIE	transfer error interrupt enable 0: disabled 1: enabled
[2]	rw	1'h0	HTIE	half transfer interrupt enable 0: disabled 1: enabled
[1]	rw	1'h0	TCIE	transfer complete interrupt enable 0: disabled 1: enabled
[0]	rw	1'h0	EN	channel enable When a channel transfer error occurs, this bit is cleared by hardware. It can not be set again by software (channel x re-activated) until the TEIFx bit of the ISR register is cleared (by setting the CTEIFx bit of the IFCR register). 0: disabled 1: enabled
0x48		**0x00000000**	**CNDTR4**	
[31:16]		16'h0	RSVD	
[15:0]	rw	16'h0	NDT	number of data to transfer (0 to 216 - 1) This field is updated by hardware when the channel is enabled: – It is decremented after each single DMA 'read followed by write' transfer, indicating the remaining amount of data items to transfer. –It is kept at zero when the programmed amount of data to transfer is reached, if the channel is not in circular mode (CIRC = 0 in the CCRx register). –It is reloaded automatically by the previously programmed value, when the transfer is complete, if the channel is in circular mode (CIRC = 1). If this field is zero, no transfer can be served whatever the channel status (enabled or not).
0x4C		**0x00000000**	**CPAR4**	
[31:0]	rw	32'h0	PA	peripheral address It contains the base address of the peripheral data register from/to which the data will be read/written. In memory-to-memory mode, this register identifies the memory destination address if DIR = 1 and the memory source address if DIR = 0. In peripheral-to-peripheral mode, this register identifies the peripheral destination address DIR = 1 and the peripheral source address if DIR = 0.
0x50		**0x00000000**	**CM0AR4**	

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表 5-4: DMAC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:0]	rw	32'h0	MA	peripheral address It contains the base address of the memory from/to which the data will be read/written. In memory-to-memory mode, this register identifies the memory source address if DIR = 1 and the memory destination address if DIR = 0. In peripheral-to-peripheral mode, this register identifies the peripheral source address DIR = 1 and the peripheral destination address if DIR = 0.
0x54		**0x00000000**	**CBSR4**	
[31:8]		24'h0	RSVD	
[7:0]	rw	8'h0	BS	burst size in non-m2m mode When BS>1, DMA will transfer for BS times for each request if left NDT is larger than BS, or else transfer for left NDT times. When BS=0 or 1, DMA will always do single transfer for each request. In memory-to-memory mode, BS is ignored.
0x58		**0x00000000**	**CCR5**	
[31:15]		17'h0	RSVD	
[14]	rw	1'h0	MEM2MEM	memory-to-memory mode 0: disabled 1: enabled
[13:12]	rw	2'h0	PL	priority level 00: low 01: medium 10: high 11: very high
[11:10]	rw	2'h0	MSIZE	memory size Defines the data size of each DMA transfer to the identified memory. In memory-to-memory mode, this field identifies the memory source if DIR = 1 and the memory destination if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral source if DIR = 1 and the peripheral destination if DIR = 0. 00: 8 bits 01: 16 bits 10: 32 bits 11: reserved
[9:8]	rw	2'h0	PSIZE	peripheral size Defines the data size of each DMA transfer to the identified peripheral. In memory-to-memory mode, this field identifies the memory destination if DIR = 1 and the memory source if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral destination if DIR = 1 and the peripheral source if DIR = 0. 00: 8 bits 01: 16 bits 10: 32 bits 11: reserved

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表 5-4: DMAC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[7]	rw	1'h0	MINC	memory increment mode Defines the increment mode for each DMA transfer to the identified memory. In memory-to-memory mode, this field identifies the memory source if DIR = 1 and the memory destination if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral source if DIR = 1 and the peripheral destination if DIR = 0. 0: disabled 1: enabled
[6]	rw	1'h0	PINC	peripheral increment mode Defines the increment mode for each DMA transfer to the identified peripheral. n memory-to-memory mode, this field identifies the memory destination if DIR = 1 and the memory source if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral destination if DIR = 1 and the peripheral source if DIR = 0. 0: disabled 1: enabled
[5]	rw	1'h0	CIRC	circular mode 0: disabled 1: enabled
[4]	rw	1'h0	DIR	data transfer direction This bit must be set only in memory-to-peripheral and peripheral-to-memory modes. 0: read from peripheral –Source attributes are defined by PSIZE and PINC, plus the CPARx register. This is still valid in a memory-to-memory mode. – Destination attributes are defined by MSIZE and MINC, plus the CM0ARx register. This is still valid in a peripheral-to-peripheral mode. 1: read from memory –Destination attributes are defined by PSIZE and PINC, plus the CPARx register. This is still valid in a memory-to-memory mode. –Source attributes are defined by MSIZE and MINC, plus the CM0ARx register. This is still valid in a peripheral-to-peripheral mode.
[3]	rw	1'h0	TEIE	transfer error interrupt enable 0: disabled 1: enabled
[2]	rw	1'h0	HTIE	half transfer interrupt enable 0: disabled 1: enabled
[1]	rw	1'h0	TCIE	transfer complete interrupt enable 0: disabled 1: enabled
[0]	rw	1'h0	EN	channel enable When a channel transfer error occurs, this bit is cleared by hardware. It can not be set again by software (channel x re-activated) until the TEIFx bit of the ISR register is cleared (by setting the CTEIFx bit of the IFCR register). 0: disabled 1: enabled

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表 5-4: DMAC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
0x5C		**0x00000000**	**CNDTR5**	
[31:16]		16'h0	RSVD	
[15:0]	rw	16'h0	NDT	number of data to transfer (0 to 216 - 1) This field is updated by hardware when the channel is enabled: – It is decremented after each single DMA 'read followed by write' transfer, indicating the remaining amount of data items to transfer. –It is kept at zero when the programmed amount of data to transfer is reached, if the channel is not in circular mode (CIRC = 0 in the CCRx register). –It is reloaded automatically by the previously programmed value, when the transfer is complete, if the channel is in circular mode (CIRC = 1). If this field is zero, no transfer can be served whatever the channel status (enabled or not).
0x60		**0x00000000**	**CPAR5**	
[31:0]	rw	32'h0	PA	peripheral address It contains the base address of the peripheral data register from/to which the data will be read/written. In memory-to-memory mode, this register identifies the memory destination address if DIR = 1 and the memory source address if DIR = 0. In peripheral-to-peripheral mode, this register identifies the peripheral destination address DIR = 1 and the peripheral source address if DIR = 0.
0x64		**0x00000000**	**CM0AR5**	
[31:0]	rw	32'h0	MA	peripheral address It contains the base address of the memory from/to which the data will be read/written. In memory-to-memory mode, this register identifies the memory source address if DIR = 1 and the memory destination address if DIR = 0. In peripheral-to-peripheral mode, this register identifies the peripheral source address DIR = 1 and the peripheral destination address if DIR = 0.
0x68		**0x00000000**	**CBSR5**	
[31:8]		24'h0	RSVD	
[7:0]	rw	8'h0	BS	burst size in non-m2m mode When BS>1, DMA will transfer for BS times for each request if left NDT is larger than BS, or else transfer for left NDT times. When BS=0 or 1, DMA will always do single transfer for each request. In memory-to-memory mode, BS is ignored.
0x6C		**0x00000000**	**CCR6**	
[31:15]		17'h0	RSVD	
[14]	rw	1'h0	MEM2MEM	memory-to-memory mode 0: disabled 1: enabled
[13:12]	rw	2'h0	PL	priority level 00: low 01: medium 10: high 11: very high

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表 5-4: DMAC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[11:10]	rw	2'h0	MSIZE	memory size Defines the data size of each DMA transfer to the identified memory. In memory-to-memory mode, this field identifies the memory source if DIR = 1 and the memory destination if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral source if DIR = 1 and the peripheral destination if DIR = 0. 00: 8 bits 01: 16 bits 10: 32 bits 11: reserved
[9:8]	rw	2'h0	PSIZE	peripheral size Defines the data size of each DMA transfer to the identified peripheral. In memory-to-memory mode, this field identifies the memory destination if DIR = 1 and the memory source if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral destination if DIR = 1 and the peripheral source if DIR = 0. 00: 8 bits 01: 16 bits 10: 32 bits 11: reserved
[7]	rw	1'h0	MINC	memory increment mode Defines the increment mode for each DMA transfer to the identified memory. In memory-to-memory mode, this field identifies the memory source if DIR = 1 and the memory destination if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral source if DIR = 1 and the peripheral destination if DIR = 0. 0: disabled 1: enabled
[6]	rw	1'h0	PINC	peripheral increment mode Defines the increment mode for each DMA transfer to the identified peripheral. n memory-to-memory mode, this field identifies the memory destination if DIR = 1 and the memory source if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral destination if DIR = 1 and the peripheral source if DIR = 0. 0: disabled 1: enabled
[5]	rw	1'h0	CIRC	circular mode 0: disabled 1: enabled

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表 5-4: DMAC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[4]	rw	1'h0	DIR	data transfer direction This bit must be set only in memory-to-peripheral and peripheral-to-memory modes. 0: read from peripheral –Source attributes are defined by PSIZE and PINC, plus the CPARx register. This is still valid in a memory-to-memory mode. – Destination attributes are defined by MSIZE and MINC, plus the CM0ARx register. This is still valid in a peripheral-to-peripheral mode. 1: read from memory –Destination attributes are defined by PSIZE and PINC, plus the CPARx register. This is still valid in a memory-to-memory mode. –Source attributes are defined by MSIZE and MINC, plus the CM0ARx register. This is still valid in a peripheral-to-peripheral mode.
[3]	rw	1'h0	TEIE	transfer error interrupt enable 0: disabled 1: enabled
[2]	rw	1'h0	HTIE	half transfer interrupt enable 0: disabled 1: enabled
[1]	rw	1'h0	TCIE	transfer complete interrupt enable 0: disabled 1: enabled
[0]	rw	1'h0	EN	channel enable When a channel transfer error occurs, this bit is cleared by hardware. It can not be set again by software (channel x re-activated) until the TEIFx bit of the ISR register is cleared (by setting the CTEIFx bit of the IFCR register). 0: disabled 1: enabled
0x70		**0x00000000**	**CNDTR6**	
[31:16]		16'h0	RSVD	
[15:0]	rw	16'h0	NDT	number of data to transfer (0 to 216 - 1) This field is updated by hardware when the channel is enabled: – It is decremented after each single DMA 'read followed by write' transfer, indicating the remaining amount of data items to transfer. –It is kept at zero when the programmed amount of data to transfer is reached, if the channel is not in circular mode (CIRC = 0 in the CCRx register). –It is reloaded automatically by the previously programmed value, when the transfer is complete, if the channel is in circular mode (CIRC = 1). If this field is zero, no transfer can be served whatever the channel status (enabled or not).
0x74		**0x00000000**	**CPAR6**	
[31:0]	rw	32'h0	PA	peripheral address It contains the base address of the peripheral data register from/to which the data will be read/written. In memory-to-memory mode, this register identifies the memory destination address if DIR = 1 and the memory source address if DIR = 0. In peripheral-to-peripheral mode, this register identifies the peripheral destination address DIR = 1 and the peripheral source address if DIR = 0.
0x78		**0x00000000**	**CM0AR6**	

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表 5-4: DMAC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:0]	rw	32'h0	MA	peripheral address It contains the base address of the memory from/to which the data will be read/written. In memory-to-memory mode, this register identifies the memory source address if DIR = 1 and the memory destination address if DIR = 0. In peripheral-to-peripheral mode, this register identifies the peripheral source address DIR = 1 and the peripheral destination address if DIR = 0.
0x7C		**0x00000000**	**CBSR6**	
[31:8]		24'h0	RSVD	
[7:0]	rw	8'h0	BS	burst size in non-m2m mode When BS>1, DMA will transfer for BS times for each request if left NDT is larger than BS, or else transfer for left NDT times. When BS=0 or 1, DMA will always do single transfer for each request. In memory-to-memory mode, BS is ignored.
0x80		**0x00000000**	**CCR7**	
[31:15]		17'h0	RSVD	
[14]	rw	1'h0	MEM2MEM	memory-to-memory mode 0: disabled 1: enabled
[13:12]	rw	2'h0	PL	priority level 00: low 01: medium 10: high 11: very high
[11:10]	rw	2'h0	MSIZE	memory size Defines the data size of each DMA transfer to the identified memory. In memory-to-memory mode, this field identifies the memory source if DIR = 1 and the memory destination if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral source if DIR = 1 and the peripheral destination if DIR = 0. 00: 8 bits 01: 16 bits 10: 32 bits 11: reserved
[9:8]	rw	2'h0	PSIZE	peripheral size Defines the data size of each DMA transfer to the identified peripheral. In memory-to-memory mode, this field identifies the memory destination if DIR = 1 and the memory source if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral destination if DIR = 1 and the peripheral source if DIR = 0. 00: 8 bits 01: 16 bits 10: 32 bits 11: reserved

续表下页...

表 5-4: DMAC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[7]	rw	1'h0	MINC	memory increment mode Defines the increment mode for each DMA transfer to the identified memory. In memory-to-memory mode, this field identifies the memory source if DIR = 1 and the memory destination if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral source if DIR = 1 and the peripheral destination if DIR = 0. 0: disabled 1: enabled
[6]	rw	1'h0	PINC	peripheral increment mode Defines the increment mode for each DMA transfer to the identified peripheral. n memory-to-memory mode, this field identifies the memory destination if DIR = 1 and the memory source if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral destination if DIR = 1 and the peripheral source if DIR = 0. 0: disabled 1: enabled
[5]	rw	1'h0	CIRC	circular mode 0: disabled 1: enabled
[4]	rw	1'h0	DIR	data transfer direction This bit must be set only in memory-to-peripheral and peripheral-to-memory modes. 0: read from peripheral –Source attributes are defined by PSIZE and PINC, plus the CPARx register. This is still valid in a memory-to-memory mode. – Destination attributes are defined by MSIZE and MINC, plus the CM0ARx register. This is still valid in a peripheral-to-peripheral mode. 1: read from memory –Destination attributes are defined by PSIZE and PINC, plus the CPARx register. This is still valid in a memory-to-memory mode. –Source attributes are defined by MSIZE and MINC, plus the CM0ARx register. This is still valid in a peripheral-to-peripheral mode.
[3]	rw	1'h0	TEIE	transfer error interrupt enable 0: disabled 1: enabled
[2]	rw	1'h0	HTIE	half transfer interrupt enable 0: disabled 1: enabled
[1]	rw	1'h0	TCIE	transfer complete interrupt enable 0: disabled 1: enabled
[0]	rw	1'h0	EN	channel enable When a channel transfer error occurs, this bit is cleared by hardware. It can not be set again by software (channel x re-activated) until the TEIFx bit of the ISR register is cleared (by setting the CTEIFx bit of the IFCR register). 0: disabled 1: enabled

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表 5-4: DMAC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
0x84		**0x00000000**	**CNDTR7**	
[31:16]		16'h0	RSVD	
[15:0]	rw	16'h0	NDT	number of data to transfer (0 to 216 - 1) This field is updated by hardware when the channel is enabled: – It is decremented after each single DMA 'read followed by write' transfer, indicating the remaining amount of data items to transfer. –It is kept at zero when the programmed amount of data to transfer is reached, if the channel is not in circular mode (CIRC = 0 in the CCRx register). –It is reloaded automatically by the previously programmed value, when the transfer is complete, if the channel is in circular mode (CIRC = 1). If this field is zero, no transfer can be served whatever the channel status (enabled or not).
0x88		**0x00000000**	**CPAR7**	
[31:0]	rw	32'h0	PA	peripheral address It contains the base address of the peripheral data register from/to which the data will be read/written. In memory-to-memory mode, this register identifies the memory destination address if DIR = 1 and the memory source address if DIR = 0. In peripheral-to-peripheral mode, this register identifies the peripheral destination address DIR = 1 and the peripheral source address if DIR = 0.
0x8C		**0x00000000**	**CM0AR7**	
[31:0]	rw	32'h0	MA	peripheral address It contains the base address of the memory from/to which the data will be read/written. In memory-to-memory mode, this register identifies the memory source address if DIR = 1 and the memory destination address if DIR = 0. In peripheral-to-peripheral mode, this register identifies the peripheral source address DIR = 1 and the peripheral destination address if DIR = 0.
0x90		**0x00000000**	**CBSR7**	
[31:8]		24'h0	RSVD	
[7:0]	rw	8'h0	BS	burst size in non memory-to-memory mode When BS>1, DMA will transfer for BS times for each request if left NDT is larger than BS, or else transfer for left NDT times. When BS=0 or 1, DMA will always do single transfer for each request. In memory-to-memory mode, BS is ignored.
0x94		**0x00000000**	**CCR8**	
[31:15]		17'h0	RSVD	
[14]	rw	1'h0	MEM2MEM	memory-to-memory mode 0: disabled 1: enabled
[13:12]	rw	2'h0	PL	priority level 00: low 01: medium 10: high 11: very high

续表下页...

表 5-4: DMAC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[11:10]	rw	2'h0	MSIZE	memory size Defines the data size of each DMA transfer to the identified memory. In memory-to-memory mode, this field identifies the memory source if DIR = 1 and the memory destination if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral source if DIR = 1 and the peripheral destination if DIR = 0. 00: 8 bits 01: 16 bits 10: 32 bits 11: reserved
[9:8]	rw	2'h0	PSIZE	peripheral size Defines the data size of each DMA transfer to the identified peripheral. In memory-to-memory mode, this field identifies the memory destination if DIR = 1 and the memory source if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral destination if DIR = 1 and the peripheral source if DIR = 0. 00: 8 bits 01: 16 bits 10: 32 bits 11: reserved
[7]	rw	1'h0	MINC	memory increment mode Defines the increment mode for each DMA transfer to the identified memory. In memory-to-memory mode, this field identifies the memory source if DIR = 1 and the memory destination if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral source if DIR = 1 and the peripheral destination if DIR = 0. 0: disabled 1: enabled
[6]	rw	1'h0	PINC	peripheral increment mode Defines the increment mode for each DMA transfer to the identified peripheral. n memory-to-memory mode, this field identifies the memory destination if DIR = 1 and the memory source if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral destination if DIR = 1 and the peripheral source if DIR = 0. 0: disabled 1: enabled
[5]	rw	1'h0	CIRC	circular mode 0: disabled 1: enabled

续表下页...

表 5-4: DMAC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[4]	rw	1'h0	DIR	data transfer direction This bit must be set only in memory-to-peripheral and peripheral-to-memory modes. 0: read from peripheral –Source attributes are defined by PSIZE and PINC, plus the CPARx register. This is still valid in a memory-to-memory mode. – Destination attributes are defined by MSIZE and MINC, plus the CM0ARx register. This is still valid in a peripheral-to-peripheral mode. 1: read from memory –Destination attributes are defined by PSIZE and PINC, plus the CPARx register. This is still valid in a memory-to-memory mode. –Source attributes are defined by MSIZE and MINC, plus the CM0ARx register. This is still valid in a peripheral-to-peripheral mode.
[3]	rw	1'h0	TEIE	transfer error interrupt enable 0: disabled 1: enabled
[2]	rw	1'h0	HTIE	half transfer interrupt enable 0: disabled 1: enabled
[1]	rw	1'h0	TCIE	transfer complete interrupt enable 0: disabled 1: enabled
[0]	rw	1'h0	EN	channel enable When a channel transfer error occurs, this bit is cleared by hardware. It can not be set again by software (channel x re-activated) until the TEIFx bit of the ISR register is cleared (by setting the CTEIFx bit of the IFCR register). 0: disabled 1: enabled
0x98		**0x00000000**	**CNDTR8**	
[31:16]		16'h0	RSVD	
[15:0]	rw	16'h0	NDT	number of data to transfer (0 to 216 - 1) This field is updated by hardware when the channel is enabled: – It is decremented after each single DMA 'read followed by write' transfer, indicating the remaining amount of data items to transfer. –It is kept at zero when the programmed amount of data to transfer is reached, if the channel is not in circular mode (CIRC = 0 in the CCRx register). –It is reloaded automatically by the previously programmed value, when the transfer is complete, if the channel is in circular mode (CIRC = 1). If this field is zero, no transfer can be served whatever the channel status (enabled or not).
0x9C		**0x00000000**	**CPAR8**	
[31:0]	rw	32'h0	PA	peripheral address It contains the base address of the peripheral data register from/to which the data will be read/written. In memory-to-memory mode, this register identifies the memory destination address if DIR = 1 and the memory source address if DIR = 0. In peripheral-to-peripheral mode, this register identifies the peripheral destination address DIR = 1 and the peripheral source address if DIR = 0.
0xA0		**0x00000000**	**CM0AR8**	

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表 5-4: DMAC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:0]	rw	32'h0	MA	peripheral address It contains the base address of the memory from/to which the data will be read/written. In memory-to-memory mode, this register identifies the memory source address if DIR = 1 and the memory destination address if DIR = 0. In peripheral-to-peripheral mode, this register identifies the peripheral source address DIR = 1 and the peripheral destination address if DIR = 0.
0xA4		**0x00000000**	**CBSR8**	
[31:8]		24'h0	RSVD	
[7:0]	rw	8'h0	BS	burst size in non-m2m mode When BS>1, DMA will transfer for BS times for each request if left NDT is larger than BS, or else transfer for left NDT times. When BS=0 or 1, DMA will always do single transfer for each request. In memory-to-memory mode, BS is ignored.
0xA8		**0x00000000**	**CSELR1**	
[31:30]		2'h0	RSVD	
[29:24]	rw	6'h0	C4S	DMA channel 4 selection
[23:22]		2'h0	RSVD	
[21:16]	rw	6'h0	C3S	DMA channel 3 selection
[15:14]		2'h0	RSVD	
[13:8]	rw	6'h0	C2S	DMA channel 2 selection
[7:6]		2'h0	RSVD	
[5:0]	rw	6'h0	C1S	DMA channel 1 selection
0xAC		**0x00000000**	**CSELR2**	
[31:30]		2'h0	RSVD	
[29:24]	rw	6'h0	C8S	DMA channel 8 selection
[23:22]		2'h0	RSVD	
[21:16]	rw	6'h0	C7S	DMA channel 7 selection
[15:14]		2'h0	RSVD	
[13:8]	rw	6'h0	C6S	DMA channel 6 selection
[7:6]		2'h0	RSVD	
[5:0]	rw	6'h0	C5S	DMA channel 5 selection

6 连接外设

6.1 I2C

6.1.1 简介

I2C(Inter-Integrated Circuit) 接口同时支持主设备与从设备角色，可作为主设备与 I2C 外设通信，也可作为从设备响应外部的 I2C 主设备。I2C 内置 8 字节 FIFO，可以进行单笔读写，也可通过 DMA 进行批量数据读写。I2C 支持标准模式 (standard-mode)、快速模式 (fast-mode)、增强快速模式 (fast-mode plus) 以及高速模式 (high-speed-mode)，最高速率可达 3.4Mbps。

6.1.2 主要特性

可同时作为主设备与从设备

- 支持总线多主设备
- 支持标准模式 (最高 100kbps)
- 支持快速模式 (最高 400kbps)
- 支持增强快速模式 (最高 1Mbps)
- 支持高速模式 (最高 3.4Mbps)
- 作为主设备支持访问 7 比特或 10 比特寻址
- 作为从设备支持 7 比特寻址
- 可配置的总线时序
- 支持时钟延展 (clock stretching)
- 8 字节 FIFO，支持 DMA
- 可配置的数字防抖动电路
- 独立的功能时钟，支持系统时钟动态调节

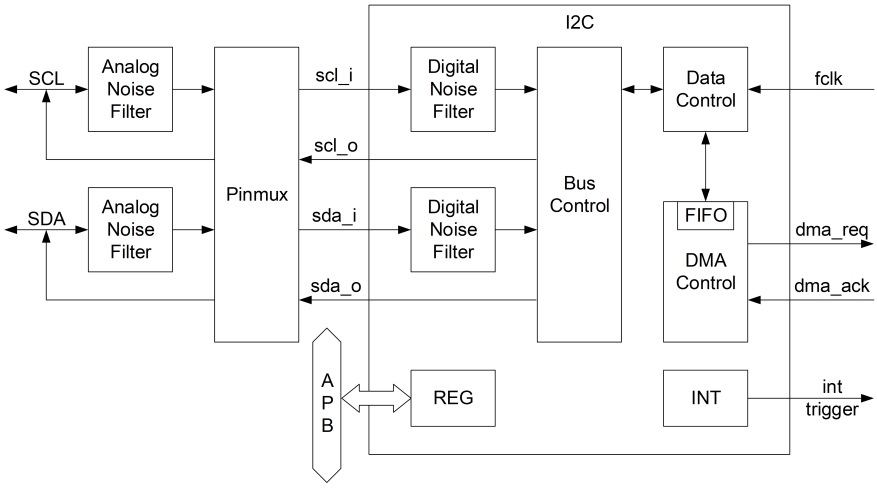

图 6-1: I2C 结构图

6.1.3 I2C 功能描述

6.1.3.1 两线传输

I2C 总线利用 SCL 与 SDA 两根线进行传输，其中 SCL 通常称为时钟线，SDA 通常称为数据线。两根线均为双向传输，且输出均为开漏模式，因此需要在芯片外部增加上拉电阻，阻值应根据最大传输速率决定。I2C 总线空闲时，SCL 与 SDA 均为上拉高电平。可通过 BMR_SCL 和 BMR_SDA 查询当前 I2C 总线信号电平。

6.1.3.2 输入滤波器

SCL 与 SDA 输入信号可经由模拟滤波器和数字滤波器滤除毛刺。模拟滤波器可滤除小于 50ns 的毛刺，在 PINMUX 模块中配置。数字滤波器可通过配置 CR_DNF 选择滤除毛刺的宽度上限，最大可配置为 7 个 fclk 周期 (约 146ns)。

6.1.3.3 传输速率

I2C 的传输速率主要由主设备决定，但当从设备支持时钟延展 (clock stretching) 时，也会受从设备影响。

I2C 接口时序基于 fclk 产生。该时钟来自芯片的外设时钟，独立于系统时钟，因此系统时钟频率的变化不会影响 I2C 的传输速率。

根据 I2C 协议，标准模式 (standard-mode) 比特率最高为 100kbps，快速模式 (fast-mode) 比特率最高为 400kbps，增强快速模式 (fast-mode plus) 比特率最高为 1Mbps，高速模式 (high-speed mode) 比特率最高为 3.4Mbps。

标准模式的基础比特率可由下列近似公式计算：

$$bit\_rate=Ffclk/(LCR\_SLV+max(LCR\_SLV,(WCR\_CNT\times 2+6))+7+CR\_DNF)$$

其中，Ffclk 为 fclk 的频率 (48MHz)。WCR_CNT 用于调整 SDA 与 SCL 边沿之间的偏移，以保证信号的建立与保持时间满足 I2C 协议，配置合理时不会影响比特率。

快速模式/增强快速模式的基础比特率可由下列近似公式计算：

$$bit\ rate=Ffclk/(LCR\_FLV+max(LCR\_FLV,(WCR\_CNT\times 2+6))+7+CR\_DNF)$$

6.1.3.4 传输序列

一次完整的 I2C 传输应基于下列传输序列进行：

1. 起始位。主设备发出，启动传输。
2. 7 比特从地址。主设备发出，用于选择从设备。
3. R/nW 比特。主设备发出，标志接收或发送方向。
4. ACK 比特。从设备发出，响应主设备请求。ACK=0 表示响应成功。ACK=1 则传输失败。
5. 8 比特数据。接收时由从设备发出，发送时由主设备发出。根据不同从设备的访问方式，可能代表寄存器地址或数据。
6. ACK 比特。接收时由主设备发出，发送时由从设备发出，是对之前 8 比特数据的响应。
7. 重复步骤 5-6 直至数据完成或出现 ACK=1。
8. 重复起始位 (回到步骤 1) 或停止位。主设备发出，重新启动传输或停止传输。

6.1.3.5 工作模式与状态

I2C 默认处于主模式，可以发起主动传输，但不监控总线上的地址传输。软件启动传输时，I2C 进入主发送或主接收状态。

若将 CR_SLVEN 置 1，则 I2C 进入主从模式，可以发起主动传输，同时监控总线上的地址传输。软件启动传输时，I2C 进入主发送或主接收状态。当监控到起始位之后的 7 位地址与 SAR_ADDR 相符时，I2C 根据 R/nW 比特进入从发送或从接收状态。

6.1.3.6 I2C 初始化流程

1. 配置 I2C 速率模式 CR_MODE，并根据速率配置相关时序寄存器 LCR、WCR 等
2. 配置 IER 使能所需中断
3. 使能 I2C，CR_SCLE=1，CR_IUE=1

6.1.3.7 主发送流程

1. 将从设备地址左移 1 位，拼上最低位 0，写入 DBR。
2. TCR=TCR_START;TCR|=TCR_TB。
3. 轮询 SR_TE 直到为 1，或等待发送完成 TE 中断。
4. SR_TE 写 1 清除标志。检查 SR_NACK，如果为 1 则发送停止位并中止传输。
5. 将待发送数据写入 DBR。
6. TCR=TCR_TB。
7. 轮询 SR_TE 直到为 1，或等待 TE 中断。
8. SR_TE 写 1 清除标志。检查 SR_NACK，如果为 1 则发送停止位并中止传输。
9. 重复步骤 5-8，如果是最后一笔数据则 TCR=TCR_TB|TCR_STOP，停止位会在发送完成后自动产生。

6.1.3.8 主接收流程

1. 将从设备地址左移 1 位，拼上最低位 1，写入 DBR。
2. TCR=TCR_START;TCR|=TCR_TB。
3. 轮询 SR_TE 直到为 1，或等待 TE 中断。
4. SR_TE 写 1 清除标志。检查 SR_NACK，如果为 1 则发送停止位并中止传输。
5. TCR=TCR_TB。
6. 轮询 SR_RF 直到为 1，或等待接收完成 RF 中断。
7. SR_RF 写 1 清除标志。从 DBR 中获取接收的数据。
8. 重复步骤 5-7，如果是最后一笔数据则 TCR=TCR_TB|TCR_NACK。
9. TCR=TCR_MA，发送停止位。
10. 轮询 SR_UB 直到为 0，停止位发送完毕，TCR=0。

6.1.3.9 从发送流程

1. 当地址检测中断 SAD 触发后，自动回复 ACK。
2. SR_SAD 写 1 清除标志。读取 SR_RWM，1 表示从发送，0 表示从接收。假设当前 SR_RWM 为 1，进入从发送状态。
3. 将待发送数据写入 DBR。

4. TCR=TCR_TB。
5. 轮询 SR_TE 直到为 1，或等待 TE 中断。
6. SR_TE 写 1 清除标志。检查 SR_NACK，如果为 1 则中止传输。
7. 重复步骤 3-6，直到检测到停止位中断 SSD。
8. SR_SSD 写 1 清除标志。

6.1.3.10 从接收流程

1. 当地址检测中断 SAD 触发后，自动回复 ACK。
2. SR_SAD 写 1 清除标志。读取 SR_RWM，1 表示从发送，0 表示从接收。假设当前 SR_RWM 为 0，进入从接收状态。
3. TCR=TCR_TB。
4. 轮询 SR_RF 直到为 1，或等待接收完成 RF 中断。
5. SR_RF 写 1 清除标志。从 DBR 中获取接收的数据。
6. 重复步骤 3-5，如果缓存将满则 TCR=TCR_TB|TCR_NACK，直到检测到停止位中断 SSD。
7. SR_SSD 写 1 清除标志。

6.1.3.11 DMA 传输

I2C 处于主发送或主接收状态时，可以开启 DMA 传输。DMA 仅作用于数据段，不能用于传输从设备地址和 R/nW 比特。I2C 支持单次 DMA 最大 511byte 数据连续传输。如果有更多的数据传输需求，可以再次启动 DMA。

DMA 启动以后，传输过程不需要 CPU 参与，由 I2C 与 DMAC 模块直接交互完成传输，并产生中断 DMADONE。I2C 模块内置 8 字节 FIFO，用于在 DMA 传输过程中缓存数据。如果出现 FIFO 溢出，会产生上溢中断 OF 或下溢中断 UF。如果主发送过程中收到从设备产生的 ACK=1，数据传输会中止，并产生中断 DMADONE。

DMA 传输的字节数通过写 DNR_NDT 配置。剩余待传输字节数可以通过读 DNR_NDT 获取。在中断 DMADONE 发生时，通过读取 DNR_NDT 以及 SR_NACK 可以获知 DMA 传输是否正常完成。

将 CR_LASTSTOP 置 1 可以在本次 DMA 传输完成后自动发送停止位。将 CR_LASTNACK 置 1 可以在本次 DMA 接收完成后自动回复 ACK=1。

使用 DMA 进行主发送或主接收的流程如下：

1. 将从设备地址左移 1 位，拼上最低位 R/nW，写入 DBR。
2. TCR=TCR_START;TCR|=TCR_TB。
3. 轮询 SR_TE 直到为 1，或等待发送完成 TE 中断。
4. SR_TE 写 1 清除标志。检查 SR_NACK，如果为 1 则发送停止位并中止传输。
5. 配置 DMAC 模块。通道外设选择为当前 I2C，数据宽度为单字节，外设地址为当前 I2C 的 FIFO 寄存器，并启动 DMAC 通道。
6. 配置 I2C 的 DMA。DNR_NDT 设为待传输字节数。如果 DMA 传输完成后需自动发送停止位，则将 CR_LASTSTOP 置 1。如果 DMA 传输完成后需自动回复 ACK=1，则将 CR_LASTNACK 置 1。CR_DMAEN 置 1 使能 DMA。
7. 等待 DMADONE 中断。
8. SR_DMADONE 写 1 清除标志。
9. 如果还需再次启动 DMA，重复步骤 5-8。
10. 轮询 SR_UB 直到为 0，停止位发送完毕。

6.1.3.12 总线异常恢复

由于电气干扰或设备异常，I2C 总线有时会出现卡死，表现为 I2C 发送或接收持续失败。当怀疑总线卡死时，可通过下述方法尝试恢复。

1. 复位 I2C 模块。CR_UR 置 1，等待 100us 后置 0。
2. 如果 BMR_SCL 和 BMR_SDA 均为 1，可将 CR_RSTREQ 置 1，并查询 CR_RSTREQ 直到变为 0。在此期间，I2C 会连续发送 RCCR_RSTCYC 个周期的时钟信号，从设备检测到这类总线信号后或可从异常中恢复。
3. 如果 BMR_SCL 或 BMR_SDA 持续为 0，怀疑上拉电阻失效或从设备挂死，需检查硬件电路或复位从设备。

6.1.4 I2C 寄存器

表 6-1: I2C 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00		**0x00000000**	**CR**	**Control register**
[31]	rw	1'h0	UR	Unit Reset. Software need first assert to reset then deassert to release. 0 = No reset. 1 = Reset I2C module.
[30]	rw	1'h0	RSTREQ	I2C will do bus reset upon this bit set. Will be cleared by HW automatically after RSTCYC cycles of SCL generated. 1 = request for i2c bus reset 0 = bus reset finished
[29]	rw	1'h0	BRGRST	Reset bus related state machine and signals. Will be cleared by HW automatically 1 = request for reset 0 = reset finished
[28:15]		14'h0	RSVD	
[14:12]	rw	3'h0	DNF	Digital noise filter These bits are used to configure the digital noise filter on SDA and SCL input. The digital filter will filter spikes with a length of up to DNF*Tfclk. 0: Digital filter disabled 1: Digital filter enabled and filtering capability up to 1 Tfclk ... 7: digital filter enabled and filtering capability up to 7 Tfclk Digital filter is added to analog filter. Digital filter will introduce delay on SCL and SDA processing, which is essential in hs-mode.
[11]	rw	1'h0	SLVEN	Slave mode Enable for SCL. 0 = Disable slave mode. Will not monitor slave address on I2C bus. 1 = Enable slave mode. Will monitor slave address on I2C bus.
[10]		1'h0	RSVD	
[9]	rw	1'h0	SCLPP	Push-pull mode Enable for SCL. 0 = open drain output for SCL. 1 = Push-pull output for SCL
[8]	rw	1'h0	MSDE	Master Stop Detected Enable: 0 = Master Stop Detect (MSD) status is not enabled. 1 = Master Stop Detect (MSD) status is enabled.
[7]		1'h0	RSVD	
[6]	rw	1'h0	LASTSTOP	Generate STOP for last DMA transfer
[5]	rw	1'h0	LASTNACK	Generate NACK for last DMA Read transfer

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表 6-1: I2C 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[4]	rw	1'h0	DMAEN	DMA Enable for both TX and RX 0 = DMA mode is NOT enabled 1 = DMA mode enabled
[3]	rw	1'h0	SCLE	SCL Enable: 0 = Disables the I2C from driving the SCL line. 1 = Enables the I2C clock output for master-mode operation.
[2]	rw	1'h0	IUE	I2C Unit Enable: 0 = Disables the unit and does not master any transactions or respond to any slave transactions. 1 = Enables the I2C (defaults to slave-receive mode). Software must guarantee the I2C bus is idle before setting this bit.
[1:0]	rw	2'h0	MODE	Bus Mode (Master operation): 2'b00: standard-mode 2'b01: fast-mode and fast-mode plus 2'b10: HS-mode (standard mode when not doing a high speed transfer) 2'b11: HS-mode (fast mode when not doing a high speed transfer) Bus Mode (Slave operation): 2'b0x: HS-mode is disabled. I2C unit uses Standard/Fast mode timing on the SDA pin. 2'b1x: HS-mode is enabled. I2C unit uses HS-mode timing on the SDA pin when a master code is received.
0x04		**0x00000000**	**TCR**	**Transfer Control register**
[31:8]		24'h0	RSVD	
[7]	w1s	1'h0	ABORTDMA	Abort DMA operation. Will be cleared by HW automatically
[6]	w1s	1'h0	RXREQ	Request DMA RX. Will be cleared by HW automatically
[5]	w1s	1'h0	TXREQ	Request DMA TX. Will be cleared by HW automatically
[4]	rw	1'h0	MA	Master Abort: Used by the I2C in master mode to generate a Stop without transmitting another data byte: 0 = The I2C transmits Stop on if TCR[STOP] is set. 1 = The I2C sends Stop without data transmission. When in master-transmit mode, after transmitting a data byte, the TCR[TB] bit is cleared. When no more data bytes need to be sent, setting master abort bit sends the Stop. The TCR[TB] bit must remain clear. In master-receive mode, when a NAK is sent without a Stop (TCR[STOP] bit was not set) and CPU does not send a repeated Start, setting this bit sends the Stop. Once again, the TCR[TB] bit must remain clear. Master Abort can be done immediately after the address phase (Master Transmit mode only).
[3]	rw	1'h0	NACK	The positive/negative acknowledge control bit, defines the type of acknowledge pulse sent by the I2C when in master receive mode: 0 = Send a positive acknowledge (ACK) pulse after receiving a data byte. 1 = Send a negative acknowledge (NACK) pulse after receiving a data byte. The I2C automatically sends an ACK pulse when responding to its slave address or when responding in slave-receive mode, regardless of the NACK control-bit setting.

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表 6-1: I2C 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[2]	rw	1'h0	STOP	Stop: Used to initiate a Stop condition after transferring the next data byte on the I2C bus when in master mode. In master-receive mode, the NACK control bit must be set in conjunction with the STOP bit. 0 = Do not send a Stop. 1 = Send a Stop.
[1]	rw	1'h0	START	Start: Used to initiate a Start condition to the I2C unit when in master mode. 0 = Do not send a Start pulse. 1 = Send a Start pulse.
[0]	rw	1'h0	TB	Transfer Byte: Used to send or receive a byte on the I2C bus: 0 = Cleared by I2C when the byte is sent/received. 1 = Send/receive a byte. CPU can monitor this bit to determine when the byte transfer has completed. In master or slave mode, after each byte transfer including acknowledge pulse, the I2C holds the SCL line low (inserting wait states) until TB is set.
0x08		**0x00000000**	**IER**	**Interrupt Enable register**
[31:16]		16'h0	RSVD	
[15]	rw	1'h0	UFIE	FIFO Underflow Interrupt Enable 0 = FIFO Underflow interrupt is not enabled 1 = FIFO Underflow interrupt is enabled
[14]	rw	1'h0	OFIE	FIFO Overflow Interrupt Enable 0 = FIFO Overflow interrupt is not enabled 1 = FIFO Overflow interrupt is enabled
[13]	rw	1'h0	DMADONEIE	DMA Transaction Done Interrupt Enable 0 = DMA Transaction done interrupt is not enabled. 1 = DMA Transaction done interrupt is enabled.
[12]	rw	1'h0	MSDIE	Master Stop Detected Interrupt Enable: 0 = Disable interrupt. 1 = Enables the I2C unit to interrupt upon detecting a Master Stop sent by the I2C unit.
[11]		1'h0	RSVD	
[10]	rw	1'h0	BEDIE	Bus Error Detected Interrupt Enable: 0 = Disable interrupt. 1 = Enables the I2C to interrupt for the following I2C bus errors: As a master transmitter, no ACK was detected after a byte was sent. As a slave receiver, the I2C generated a NACK pulse. Software is responsible for guaranteeing that misplaced Start and Stop conditions do not occur.
[9]	rw	1'h0	SADIE	Slave Address Detected Interrupt Enable: 0 = Disable interrupt. 1 = Enables the I2C to interrupt upon detecting a slave address match or a general call address.
[8]		1'h0	RSVD	
[7]	rw	1'h0	RFIE	DBR Receive Full Interrupt Enable: 0 = Disable interrupt. 1 = Enables the I2C to interrupt when the DBR has received a data byte from the I2C bus.

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表 6-1: I2C 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[6]	rw	1'h0	TEIE	DBR Transmit Empty Interrupt Enable: 0 = Disable interrupt. 1 = Enables the I2C to interrupt after transmitting a byte onto the I2C bus.
[5]	rw	1'h0	ALDIE	Arbitration Loss Detected Interrupt Enable: 0 = Disable interrupt. 1 = Enables the I2C to interrupt upon losing arbitration while in master mode.
[4]	rw	1'h0	SSDIE	Slave Stop Detected Interrupt Enable: 0 = Disable interrupt. 1 = Enables the I2C to interrupt when it detects a Stop condition while in slave mode.
[3:0]		4'h0	RSVD	
0x0C		**0x00000000**	**SR**	**Status register**
[31:16]		16'h0	RSVD	
[15]	rw1c	1'h0	UF	FIFO Underflow Flag. Asserted when FIFO is empty and a POP request generated without a PUSH. Cleared if write 1
[14]	rw1c	1'h0	OF	FIFO Overflow Flag. Asserted when FIFO is full and a PUSH request generated without a POP. Cleared if write 1
[13]	rw1c	1'h0	DMADONE	DMA Transaction Done. Asserted when both APB and I2C bus have finished transfer. Cleared if write 1
[12]	rw1c	1'h0	MSD	Master Stop Detected: 0 = No Master Stop Detected. 1 = This bit is set by the I2C unit when all of the following are true: This bit is enabled (CR[MSDE] = 1); I2C unit is configured as a master; I2C transmits a STOP signal
[11]	r	1'h0	EBB	Early Bus Busy 0 = I2C bus is idle or the I2C is using the bus (that is, unit busy). 1 = Set when the unit detects that the SCL or SDA line is low without a START condition. Bit will remain set until the I2C unit detects the bus is idle by detecting a STOP condition. Bit will also be set whenever the IBB bit is set.
[10]	rw1c	1'h0	BED	Bus Error Detected: 0 = No error detected. 1 = The I2C sets this bit when it detects one of the following error conditions: As a master transmitter, no ACK was detected on the interface after a byte was sent. As a slave receiver, the I2C generates a NACK pulse. When an error occurs, I2C bus transactions continue. Software must guarantee that misplaced Start and Stop conditions do not occur. Cleared if write 1
[9]	rw1c	1'h0	SAD	Slave Address Detected: 0 = No slave address was detected. 1 = The I2C detected a seven-bit address that matches the general call address or SAR. An interrupt is signalled when enabled in the CR. Cleared if write 1
[8]		1'h0	RSVD	

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表 6-1: I2C 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[7]	rw1c	1'h0	RF	DBR Receive Full: 0 = The DBR has not received a new data byte or the I2C is idle. 1 = The DBR register received a new data byte from the I2C bus. An interrupt is signalled when enabled in the CR. Cleared if write 1
[6]	rw1c	1'h0	TE	DBR Transmit Empty: 0 = The data byte is still being transmitted. 1 = The I2C has finished transmitting a data byte on the I2C bus. An interrupt is signalled when enabled in the CR. Cleared if write 1
[5]	rw1c	1'h0	ALD	Arbitration Loss Detected: Used during multi-master operation: 0 = Cleared when arbitration is won or never took place. 1 = Set when the I2C loses arbitration. Cleared if write 1
[4]	rw1c	1'h0	SSD	Slave Stop Detected: 0 = No Stop detected. 1 = Set when the I2C detects a Stop while in slave-receive or slave-transmit mode. Cleared if write 1
[3]	r	1'h0	IBB	I2C Bus Busy: 0 = I2C bus is idle or the I2C is using the bus (that is, unit busy). 1 = Set when the I2C bus is busy but local I2C is not involved in the transaction.
[2]	r	1'h0	UB	Unit Busy: 0 = I2C not busy. 1 = Set when local I2C is busy. This is defined as the time between the first Start and Stop.
[1]	r	1'h0	NACK	ACK/NACK Status: 0 = The I2C received or sent an ACK on the bus. 1 = The I2C received or sent a NACK.on the bus. This bit is used in slave-transmit mode to determine when the byte transferred is the last one. This bit is updated after each byte and ACK/NACK information is received.
[0]	r	1'h0	RWM	Read/write Mode: 0 = The I2C is in master-transmit or slave-receive mode. 1 = The I2C is in master-receive or slave-transmit mode. This is the R/nW bit of the slave address. It is cleared automatically by hardware after a Stop state.
0x10		**0x00000000**	**DBR**	**Data Buffer register**
[31:8]		24'h0	RSVD	

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表 6-1: I2C 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[7:0]	rw	8'h0	DATA	use the I2C Data Buffer register to transmit and receive data from the I2C bus. The DBR is accessed by software on one Side and by the I2C Shift register on the other. The DBR receives data coming into the I2C unit after a full byte is received and acknowledged. CPU writes data going out of the I2C to the DBR and sends it to the serial bus. When the I2C is in transmit mode (master or slave), CPU writes data to the DBR over the internal bus. CPU write data to the DBR when a master transaction is initiated or when the DBR transmit-empty interrupt is signalled. Data moves from the DBR to the Shift register when the transfer byte bit is set. The DBR transmit-empty interrupt is signalled (if enabled) when a byte is transferred on the I2C bus and the acknowledge cycle is complete. If the DBR is not written, and a Stop condition is not in place before the I2C bus is ready to transfer the next byte packet, the I2C unit inserts wait states until CPU writes the DBR and sets the transfer byte bit. When the I2C is in receive mode (master or slave), CPU reads DBR data over the internal bus. CPU reads data from the DBR when the DBR receive-full interrupt is signalled. The data moves from the Shift register to the DBR when the acknowledge cycle is complete. The I2C inserts wait states until the DBR is read. After the software reads the DBR, CR[NACK] are written by the software, allowing the next byte transfer to proceed to the I2C bus. In DMA mode, DBR is automatically filled from FIFO in master transmit mode, or fetched and stored in FIFO in master receive mode until DMA done or aborted.
0x14		**0x00000047**	**SAR**	**Slave Address Register**
[31:7]		25'h0	RSVD	
[6:0]	rw	7'h47	ADDR	The seven-bit address to which the I2C responds when in slave-receive mode
0x18		**0x081C72ED**	**LCR**	**Load Count Register**
[31:27]	rw	5'h1	HLVH	Decrementer Load value for High Speed Mode SCL (master mode) for high phase. Thigh=Tfclk*(HLVH+4+DNF)
[26:18]	rw	9'h7	HLVL	Decrementer Load value for High Speed Mode SCL (master mode) for low phase. Tlow=Tfclk*(HLVL+3+DNF). Data rate is generated as 1/(Thigh+Tlow), or Ffclk/(HLVH+HLVL+7+2*DNF). 3.2Mbps data rate is generated by default if fclk is 48MHz. HLVL also controls setup time and hold time for START and STOP condition in High Speed Mode(master mode). Thdsta=Tsusta=Tsusto=Tfclk*(HLVL+1)
[17:9]	rw	9'h39	FLV	Decrementer Load value for Fast Mode (or Fast Mode Plus) SCL (master mode) for both high and low phase. Data rate is generated as Ffclk/(FLV+max(FLV,CNT*2+6)+7+DNF) approximately. 400kbps data rate is generated by default if fclk is 48MHz. FLV also controls setup time and hold time for START and STOP condition in Fast Mode(master mode). Thdsta=Tsusta=Tsusto=Tfclk*FLV

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表 6-1: I2C 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[8:0]	rw	9'hED	SLV	Decrementer Load value for Standard Mode SCL (master mode) for both high & low phase. Data rate is generated as Ffclk/(SLV+max(SLV,CNT*2+6)+7+DNF) approximately. 100kbps data rate is generated by default if fclk is 48MHz. SLV also controls setup time and hold time for START and STOP condition in Standard Mode(master mode). Thdsta=Tsusta=Tsusto=Tfclk*SLV
0x1C		**0x0000000A**	**WCR**	**Wait Count Register**
[31:8]		24'h0	RSVD	
[7:0]	rw	8'hA	CNT	Controls the counter values defining the setup and hold times in standard and fast mode Tvddat=Thddat=Tfclk*(CNT+2) Tsudat=max(Tlow-Thddat,Thddat) Lower counter values may violate setup and hold times.
0x20		**0x00000009**	**RCCR**	**Bus Reset Cycle Counter Register**
[31:4]		28'h0	RSVD	
[3:0]	rw	4'h9	RSTCYC	The cycles of SCL during bus reset
0x24		**0x00000003**	**BMR**	**Bus Monitor Register**
[31:2]		30'h0	RSVD	
[1]	r	1'h1	SCL	value of the SCL pin. Software can check bus level when the I2C bus is hung and the I2C unit must be reset.
[0]	r	1'h1	SDA	value of the SDA pin.
0x28		**0x00000000**	**DNR**	**DMA number register**
[31:9]		23'h0	RSVD	
[8:0]	rw	9'h0	NDT	Write as number of data to transfer in byte. Read as left data number to transfer
0x30		**0x00000000**	**FIFO**	**FIFO Register**
[31:8]		24'h0	RSVD	
[7:0]	rw	8'h0	DATA	Write to push send data into FIFO. Read to pop received data from FIFO

6.2 SPI

6.2.1 简介

SPI 支持 3 种通信格式：SSP/SPI/Microwire。SSP/SPI 为全双工通信协议，控制器可以配置为 Master 或 Slave 模式。Microwire 为半双工通信协议，控制器仅可配置为 Master 模式。SPI 控制器内置发送/接收 FIFO。发送 FIFO 和接收 FIFO 共享同一个地址，读该地址时访问接受 FIFO，写该地址时访问发送 FIFO。FIFO 支持软件访问模式和 DMA 访问模式。

6.2.2 主要特性

- 支持 3 种通信格式：SSP/SPI/Microwire
- 支持 4 到 32Bit 的数据宽度
- SPI 格式下时钟极性和相位可通过寄存器 SPO 和 SPH 设置
- 片选信号极性可配
- FIFO 深度为 32Bits×16Entry

- 接收发送都支持 DMA 模式
- HPSYS 中的 SPI 最大时钟频率为 48MHz；LPSYS 中的 SPI 最大时钟频率为 24MHz

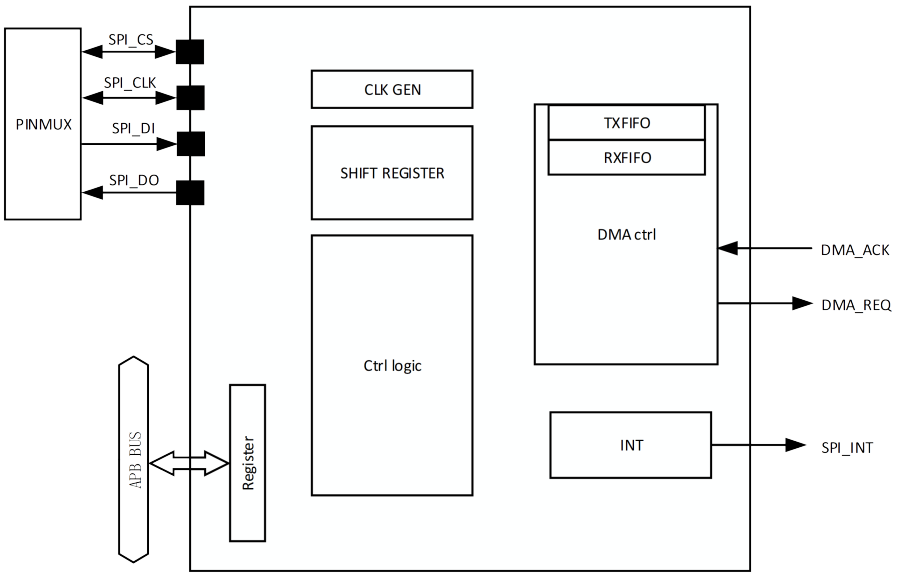

图 6-2: SPI 结构图

6.2.3 SPI 功能描述

6.2.3.1 通信协议设置

设置 FRF 可以选择通信协议：

- FRF=0：SPI 协议
- FRF=1：SSP 协议
- FRF=2：MicroWire 协议

6.2.3.2 主机/从机设置

SFRMDIR=0：主机模式，SFRMDIR=1：从机模式

6.2.3.3 时钟频率设置

SPI 的时钟由源时钟及源时钟分频时钟二选一得到。分频时钟的频率为源时钟频率/CLK_DIV。源时钟频率在 HPSYS 中为 48MHz，在 LPSYS 中为 24MHz。设置 SPI 时钟的流程是：

1. 设置 CLK_DIV 配置分频时钟分频比
2. 设置 CLK_SEL 选择时钟来源，CLK_SEL=0：选择分频时钟，CLK_SEL=1：选择源时钟
3. 设置 CLK_SSP_EN 为 1 以使能 SPI 时钟

6.2.3.4 数据宽度设置

支持 4-32bit 的数据宽度，设置 DSS 可以配置数据位宽，数据位宽 =DSS+1。

6.2.3.5 FIFO 访问

在 TNF 为 1 前提下，写 DATA：往 TXFIFO 中添加需要发送的数据

在 RNE 为 1 前提下，读 DATA：从 RXFIFO 中读取收到的数据

6.2.3.6 DMA 接口配置

将 RSRE 写 1 使能 RX 数据的 DMA 功能，在 RX FIFO 中的数据多于 RFT 时，SPI 会发出 DMA 请求。

将 TSRE 写 1 使能 TX 数据的 DMA 功能，在 RX FIFO 中的数据多于 RFT 时，SPI 会发出 DMA 请求。

6.2.3.7 四线模式通信流程

1. 设置 pinmux
2. 设置通信协议
3. 设置时钟频率
4. 设置数据位宽
5. 设置主从模式
6. 将 SSE 写 1，使能 SPI
7. 访问 FIFO 开始收发

6.2.4 SPI 寄存器

表 6-2: SPI 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00			**TOP_CTRL**	**Top Control Register**
[31:19]		13'h0	RSVD	
[18]	rw	1'b0	TTELP	TXD Three-state Enable On Last Phase 0 = TXDx is three-stated 1/2 clock cycle after the beginning of the LSB 1 = TXDx output signal is three-stated on the clock edge that ends the LSB
[17]	rw	1'b0	TTE	TXD Three-State Enable 0 = TXDx output signal is not three-stated 1 = TXD is three-stated when not transmitting data
[16]	rw	1'b0	SCFR	Slave Clock Free Running 0 = Clock input to SSPSCLKx is continuously running 1 = Clock input to SSPSCLKx is only active during data transfers.
[15]	rw	1'b0	IFS	Invert Frame Signal 0 = SSPSFRMx polarity is determined by the PSP polarity bits 1 = SSPSFRMx will be inverted from normal-SSPSFRMx (as defined by the PSP polarity bits). (Works in all frame formats: SPI, SSP, and PSP)
[14]	rw	1'b0	HOLD_FRAME_LOW	Hold Frame Low Control 1=After this field is set to 1 and the SSP is operating in master mode, the output frame clock ssp_sfrm_gpio will hold low. Used for SPI and NMW Format Rx FIFO Auto Full Control, which makes the frame clock is still low during there's no bit clock, or the data transfers before the stop clock will be discarded.
[13]	rw	1'b0	TRAIL	Trailing Byte 0 = Trailing bytes are handled by the <var Product Number> 1 = Trailing bytes are handled by DMA bursts

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表 6-2: SPI 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[12]		1'b0	Reserved	Reserved
[11]	rw	1'b0	SPH	Motorola SPI SSPSCLK phase setting 0 = SSPSCLKx is inactive until one cycle after the start of a frame and active until 1/2 cycle before the end of a frame 1 = SSPSCLKx is inactive until 1/2 cycle after the start of a frame and active until one cycle before the end of a frame
[10]	rw	1'b0	SPO	Motorola SPI SSPSCLK Polarity Setting 0 = The inactive or idle state of SSPSCLKx is low 1 = The inactive or idle state of SSPSCLKx is high
[9:5]	rw	5'h0	DSS	SSP Work data size, register bits value 0 31 indicated data size 1 32 bits, usually use data size 8bits, 16bits, 24bits, 32bits
[4]	rw	1'b0	SFRMDIR	SSP Frame (SSPSFRMx) Direction 0 = Master mode, SSPx port drives SSPSFRMx 1 = Slave mode, SSPx port receives SSPSFRMx
[3]	rw	1'b0	SCLKDIR	SSP Serial Bit Rate Clock (SSPSCLKx) Direction 0 = Master mode, SSPx port drives SSPSCLKx 1 = Slave mode, SSPx port receives SSPSCLKx
[2:1]	rw	2'h0	FRF	Frame Format 0x0 = Motorola* Serial Peripheral Interface (SPI) 0x1 = Texas Instruments* Synchronous Serial Protocol (SSP) 0x2 = National Semiconductor Microwire* 0x3 = Programmable Serial Protocol (PSP)
[0]	rw	1'b0	SSE	Synchronous Serial Port Enable 0 = SSPx port is disabled 1 = SSPx port is enabled
0x04			**FIFO_CTRL**	**FIFO Control Register**
[31:18]		14'h0	RSVD	
[17]	rw	1'h0	RXFIFO_AUTO_FULL_CTRL	Rx FIFO Auto Full Control =1After this field is set to 1 and the SSP is operating in master mode, the SSP FSM returns to IDLE state and stops the ssp_sclk_gpio. When Rx FIFO is full, the SSP FSM continues transferring data after the Rx FIFO is not full. This field is used to avoid an Rx FIFO overrun issue. 1= Enable Rx FIFO auto full control
[16]	rw	1'h0	FPCKE	FIFO Packing Enable 0 = FIFO packing mode disabled 1 = FIFO packing mode enabled
[15:14]	rw	2'h0	TXFIFO_WR_ENDIAN	apb_pwdata Write to Tx FIFO Endian 0x0 = txfifo_wdata[31:0] = apb_pwdata[31:0] 0x1 = fifo_wdata[31:0] = apb_pwdata[15:0], apb_pwdata[31:16] 0x2 = txfifo_wdata[31:0] = apb_pwdata[7:0], apb_pwdata[15:8], apb_pwdata[23:16], apb_pwdata[31:24] 0x3 = txfifo_wdata[31:0] = apb_pwdata[23:16], apb_pwdata[31:24], apb_pwdata[7:0], apb_pwdata[15:8]
[13:12]	rw	2'h0	RXFIFO_RD_ENDIAN	apb_prdata Read from Rx FIFO Endian 0x0 = apb_prdata[31:0] = rxfifo_wdata[31:0] 0x1 = apb_prdata[31:0] = rxfifo_wdata[15:0], rxfifo_wdata[31:16] 0x2 = apb_prdata[31:0]= rxfifo_wdata[7:0], rxfifo_wdata[15:8], rxfifo_wdata[23:16], rxfifo_wdata[31:24] 0x3 = apb_prdata[31:0]= rxfifo_wdata[23:16], rxfifo_wdata[31:24], rxfifo_wdata[7:0], rxfifo_wdata[15:8]
[11]	rw	1'h0	RSRE	Receive Service Request Enable 0 = DMA service request is disabled 1 = DMA service request is enabled

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表 6-2: SPI 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[10]	rw	1'h0	TSRE	Transmit Service Request Enable 0 = DMA service request is disabled 1 = DMA service request is enabled
[9:5]	rw	5'h0	RFT	RXFIFO Trigger Threshold This field sets the threshold level at which RXFIFO asserts interrupt. The level should be set to the preferred threshold value minus 1.
[4:0]	rw	5'h0	TFT	TXFIFO Trigger Threshold This field sets the threshold level at which TXFIFO asserts interrupt. The level should be set to the preferred threshold value minus 1.
0x08			**INTE**	**Interrupt Enable Register**
[31:7]		25'h0	RSVD	
[6]	rw	1'h0	EBCEI	Enable Bit Count Error Interrupt 0 = Interrupt due to a bit count error is disabled 1 = Interrupt due to a bit count error is enabled
[5]	rw	1'h0	TIM	Transmit FIFO Underrun Interrupt Mask 0 = TUR events generate an SSP interrupt 1 = TUR events do NOT generate an SSP interrupt
[4]	rw	1'h0	RIM	Receive FIFO Overrun Interrupt Mask 0 = ROR events generate an SSP interrupt 1 = ROR events do NOT generate an SSP interrupt
[3]	rw	1'h0	TIE	Transmit FIFO Interrupt Enable 0 = TXFIFO threshold-level-reached interrupt is disabled 1 = TXFIFO threshold-level-reached interrupt is enabled
[2]	rw	1'h0	RIE	Receive FIFO Interrupt Enable 0 = RXFIFO threshold-level-reached interrupt is disabled 1 = RXFIFO threshold-level-reached interrupt is enabled
[1]	rw	1'h0	TINTE	Receiver Time-out Interrupt Enable 0 = Receiver time-out interrupt is disabled 1 = Receiver time-out interrupt is enabled
[0]	rw	1'h0	PINTE	Peripheral Trailing Byte Interrupt Enable 0 = Peripheral trailing byte interrupt is disabled 1 = Peripheral trailing byte interrupt is enabled
0x0C			**TO**	**SPI Time Out Register**
[31:24]		8'h0	RSVD	
[23:0]	r	24'h0	TIMEOUT	Timeout Value TIMEOUT value is the value (0 to 2<super 24>-1) that defines the time-out interval. The time-out interval is given by the equation shown in the TIMEOUT Interval Equation.
0x10			**DATA**	**SPI DATA Register**
[31:0]	rw	32'h0	DATA	DATA This field is used for data to be written to the TXFIFO read from the RXFIFO.
0x14			**STATUS**	**Status Register**
[31:24]		8'h0	RSVD	

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表 6-2: SPI 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[23]	r	1'h0	OSS	Odd Sample Status 0 = RxFIFO entry has two samples 1 = RxFIFO entry has one sample Note that this bit needs to be looked at only when FIFO Packing is enabled (<FIFO Packing Enable> field in SSP FIFO Control Register is set). Otherwise, this bit is zero. When SSPx port is in Packed mode and the CPU is used instead of DMA to read the RxFIFO, the CPU should make sure that <Receive FIFO Not Empty> = 1 AND this field = 0 before it attempts to read the RxFIFO.
[22]	r	1'h0	TX_OSS	TX FIFO Odd Sample Status When SSPx port is in packed mode, the number of samples in the TX FIFO is: (<Transmit FIFO Level>*2 + this field), when <Transmit FIFO Not Full> = 1 32, when <Transmit FIFO Not Full> = 0. The TX FIFO cannot accept new data when <Transmit FIFO Not Full> = 1 and <Transmit FIFO Level> = 15 and this field = 1. (The TX FIFO has 31 samples). 0 = TxFIFO entry has an even number of samples 1 = TxFIFO entry has an odd number of samples Note that this bit needs to be read only when FIFO Packing is enabled (<FIFO Packing Enable> in the SSP FIFO Control Register is set). Otherwise, this bit is zero.
[21]	w1c	1'h0	BCE	Bit Count Error 0 = The SSPx port has not experienced a bit count error 1 = The SSPSFRMx signal was asserted when the bit counter was not zero
[20]	w1c	1'h0	ROR	Receive FIFO Overrun 0 = RXFIFO has not experienced an overrun 1 = Attempted data write to full RXFIFO, causes an interrupt request
[19]		1'b0	RSVD	
[18:15]	r	4'h0	RFL	Receive FIFO Level This field is the number of entries minus one in RXFIFO. When the value 0x1F is read, the RXFIFO is either empty or full, and software should read the <Receive FIFO Not Empty> field.
[14]	r	1'h0	RNE	Receive FIFO Not Empty 0 = RXFIFO is empty 1 = RXFIFO is not empty
[13]	r	1'h0	RFS	Receive FIFO Service Request 0 = RXFIFO level is at or below RFT threshold (RFT) or SSPx port is disabled 1 = RXFIFO level exceeds RFT threshold (RFT), causes an interrupt request
[12]	w1c	1'h0	TUR	Transmit FIFO Underrun 0 = The TXFIFO has not experienced an underrun 1 = A read from the TXFIFO was attempted when the TXFIFO was empty, causes an interrupt if it is enabled (<Transmit FIFO Underrun Interrupt Mask> in the SSP INT EN Register is 0)
[11]		1'b0	RSVD	
[10:7]	r	4'h0	TFL	Transmit FIFO Level This field is the number of entries in TXFIFO.When the value 0x0 is read, the TXFIFO is either empty or full, and software should read the <Transmit FIFO Not Full> field.
[6]	r	1'h0	TNF	Transmit FIFO Not Full 0 = TXFIFO is full 1 = TXFIFO is not full

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表 6-2: SPI 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[5]	r	1'h0	TFS	Transmit FIFO Service Request 0 = TX FIFO level exceeds the TFT threshold (TFT + 1) or SSPx port disabled 1 = TXFIFO level is at or below TFT threshold (TFT + 1), causes an interrupt request
[4]	w1c	1'h0	EOC	End Of Chain 0 = DMA has not signaled an end of chain condition 1 = DMA has signaled an end of chain condition
[3]	w1c	1'h0	TINT	Receiver Time-out Interrupt 0 = No receiver time-out is pending 1 = Receiver time-out pending, causes an interrupt request
[2]	w1c	1'h0	PINT	Peripheral Trailing Byte Interrupt 0 = No peripheral trailing byte interrupt is pending 1 = Peripheral trailing byte interrupt is pending
[1]	r	1'h0	CSS	Clock Synchronization Status 0 = The SSPx port is ready for slave clock operations 1 = The SSPx port is currently busy synchronizing slave mode signals
[0]	r	1'h0	BSY	SSP Busy 0 = SSPx port is idle or disabled 1 = SSPx port is currently transmitting or receiving framed data
0x24			**RWOT_CTRL**	**SSP RWOT Control Register**
[31:5]		27'h0	RSVD	
[4]	rw	1'h0	MASK_RWOT_LAST_SAMPLE	Mask last_sample_flag in RWOT Mode 1= Mask 0 = Unmask
[3]	rw	1'h0	CLR_RWOT_CYCLE	Clear SSP Internal rwot_counter This field clears the rwot_counter to 0. This field is self cleared by SSP after SSE = 1. 1 = Clear rwot_counter
[2]	rw	1'h0	SET_RWOT_CYCLE	Set RWOT Cycle This field is used to set the value of the SSP_RWOT_CCM register to the SSP internal rwot_counter. This field is self-cleared by SSP after SSE = 1. 1 = Set rwot_counter
[1]	rw	1'h0	CYCLE_RWOT_EN	Enable SSP RWOT Cycle Counter Mode 1 = Enable
[0]	rw	1'h0	RWOT	Receive Without Transmit 0 = Transmit/receive mode 1 = Receive without transmit mode
0x28			**RWOT_CCM**	**SSP RWOT Counter Cycles Match Register**
[31:0]	rw	32'h0	SSPRWOTCCM	It's just total ssp_sclk_gpio Cycles The value of this register defines the total number of ssp_sclk_gpio cycles when SSP works in master and RWOT mode. When the rwot_counter matches this value, SSP returns to IDLE state and does not output ssp_sclk_gpio anymore.
0x2C			**RWOT_CVWRn**	**SSP RWOT Counter Value Write for Red Request Register**
[31:0]	rw	32'h0	SSPRWOTCVWR	SSPRWOTCVWR This register prevents the risk of instability on rwot_counter value reading, it's only valid after SSP has been enabled Write 0 = No effect Write 1 = Capture value of rwot_counter Read: Returns the captured value of rwot_counter
0x3C			**CLK_CTRL**	**SSP CLK Control Register**
[31:9]		23'h0	RSVD	
[8]	rw	1'h0	CLK_SSP_EN	
[7]	rw	1'h0	CLK_SEL	0: select clk_div as clk_ssp 1: select clk_sys as clk_ssp
[6:0]	rw	7'h0	CLK_DIV	div ratio from clk_sys
0x54			**TRIWIRE_CTRL**	**SSP Three Wire Mode Control Register**

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表 6-2: SPI 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:3]		29'h0	RSVD	
[2]	rw	1'h0	SSP_WORK_WIDTH_DYN_CHANGE	SSP_WORK_WIDTH_DYN_CHNAGE 1=SP can dynamicly change SSP_TOP_CTRL[9:5] without disabling SSP_TOP_CTRL[0] and re-enabling SSP_TOP_CTRL[0]
[1]	rw	1'h0	TXD_OEN	TXD_OEN 1=TXD is input 0=TXD is output
[0]	rw	1'h0	SPI_TRI_WIRE_EN	SPI_THREE_WIRE_MODE_EN 1=enable

7 模拟外设

7.1 GPADC

7.1.1 简介

GPADC 是一个 12bit 精度 SARADC，支持 0-3.3V 输入电压，输出为 12bit 数据。输入电压可为单端或差分，输出数据可通过 APB 总线或 DMA 接口读取。

7.1.2 主要特性

- 输入电压范围：0~3.3V，12Bit 分辨率
- 支持单端模式和双端模式
- 支持 8 路单端模拟输入或 4 对差分模拟输入
- 支持单次测量模式和循环测量模式
- 每次测量可以划分为 8 个时隙，各时隙可以单独配置模拟输入通道
- 支持软件（写寄存器）和硬件（如计时器）触发方式
- 支持 DMA 通道
- 采样频率可配
- 转换完成后产生中断

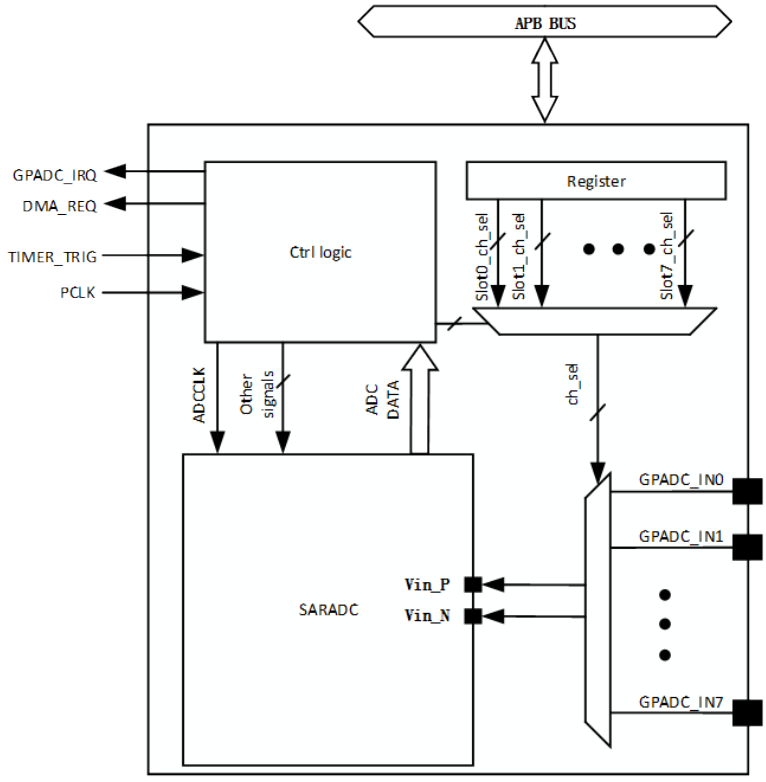

图 7-1: GPADC 框图

7.1.3 功能描述

7.1.3.1 GPADC 时钟产生

GPADC 时钟由 PCLK 分频产生，通过配置 ADC_CTRL_REG 的 DATA_SAMP_DLY 比特和 ADC_CTRL_REG2 中的 CONV_WIDTH 和 SAMP_WIDTH 比特设置 ADCCLK 频率，计算公式为：

$f_{ADCCLK}=f_{PCLK}/(DATA\_SAMP\_DLY+CONV\_WIDTH+SAMP\_WIDTH+2)$。

因为 ADCCLK 由 PCLK 分频产生，设置 ADCCLK 频率时需要注意确认 PCLK 频率。

7.1.3.2 时隙配置

每一轮 GPADC 采样，共有 8 个时隙按顺序依次工作，通过设置 ADC_SLOT*_REG 中的 SLOT_EN 比特每个时隙可单独使能或禁用；通过设置 ADC_SLOT*_REG 中的 PCHNL_SEL 和 NCHNL_SEL 比特，可独立配置各时隙的输入通道。

7.1.3.3 单端/差分模式

将寄存器 ADC_CFG_REG 中的 ANAU_GPADC_SE 比特置为 1，则 GPADC 为单端输入模式，只需设置各时隙对应配置寄存器中的 PCHNL_SEL 比特来选择输入通道。

将寄存器 ADC_CFG_REG 中的 ANAU_GPADC_SE 比特置为 0，则 GPADC 为差分输入模式，设置各时隙对应配置寄存器中的 PCHNL_SEL 和 NCHNL_SEL 比特来选择 Vin_P 和 Vin_N 对应的输入通道。

7.1.3.4 输入通道选择

GPADC 共有 8 路输入通道，通过设置 ADC_SLOT*_REG 中的 PCHNL_SEL 和 NCHNL_SEL 比特，可配置各时隙所要采样的输入通道。

如果为单端模式，只需设置 PCHNL_SEL 比特来选择输入通道。

7.1.3.5 采样模式

若 ADC_CTRL_REG 中的 ADC_OP_MODE 比特置 0，则 GPADC 处于单次采样模式，该模式下每次启动 GPADC 后，GPADC 将按照各时隙配置完成一轮采样，然后回到等待触发状态。

若 ADC_CTRL_REG 中的 ADC_OP_MODE 比特置 1，则 GPADC 处于连续采样模式，该模式下每次启动 GPADC 后，GPADC 将循环按照各时隙配置循环进行采样。将 ADC_CTRL_REG 的 ADC_STOP 比特置 1 可使 GPADC 回到等待触发状态。

7.1.3.6 启动 GPADC

- 写寄存器启动
  将寄存器 ADC_CTRL_REG 中的 ADC_START 比特置 1，可以启动 GPADC。
  触发 GPADC 后，如果 GPADC 处于单次采样模式，则完成一轮采样后，回到等待触发状态。如果 GPADC 处于连续采样模式，则需将 ADC_CTRL_REG 的 ADC_STOP 比特置 1 使 GPADC 回到等待触发状态。
- Timer 触发

GPADC 支持 TIMER 触发，使能 TIMER 触发功能需要将 ADC_CTRL_REG 中的 TIMER_TRIG_EN 比特置为 1。共有 8 个触发源，可通过寄存器 ADC_CTRL_REG 中的 TIMER_TRIG_SRC_SEL 比特选择触发源。对应关系如下表：

TIMER_TRIG_SRC_SEL	TRIG_SRC
0	GPTIM3 TRGO
1	GPTIM4 TRGO
2	GPTIM5 TRGO
3	BTIM3 TRGO
4	BTIM4 TRGO
5	GPTIM3 CH0 输出
6	GPTIM3 CH1 输出
7	GPTIM3 CH2 输出

触发 GPADC 后，如果 GPADC 处于单次采样模式，则完成一轮采样后，回到等待触发状态。如果 GPADC 处于连续采样模式，则需将 ADC_CTRL_REG 的 ADC_STOP 比特置 1 使 GPADC 回到等待触发状态。

7.1.3.7 数据访问

GPADC 转换得到的数据可以通过以下两种方式访问：

- 寄存器读取
  软件可以通过读寄存器直接读取 GPADC 转换结果。各时隙对应数据存放在寄存器 ADC_RDATA* 中，寄存器和各时隙数据的对应关系如下表：

ADC_RDATA0[31:0]	
SLOT1_RDATA	SLOT0_RDATA
ADC_RDATA1[31:0]	
SLOT3_RDATA	SLOT2_RDATA
ADC_RDATA2[31:0]	
SLOT5_RDATA	SLOT4_RDATA
ADC_RDATA3[31:0]	
SLOT7_RDATA	SLOT6_RDATA

在寄存器 ADC_RDATA* 中，各时隙对应的 GPADC 输出数据的 LSB 向右对齐到寄存器的 0 比特或者 16 比特。以 ADC_RDATA0 为例说明时隙数据在寄存器里的对齐方式，对齐方式如下表：

SLOT0_RDATA（ADC_RDATA0[31:16]）																SLOT0_RDATA（ADC_RDATA0[15:0]）															
0	0	0	0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	0	0	0	0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

- DMA 模式
  通过 LPSYS 中的 DMAC2 读取 GPADC 的转换结果。使用流程为：
  将寄存器 ADC_CTRL_REG 的 DMA_EN 比特置 1。
  将 DMA 的源地址设置为 0x50016034。ADC 数据在该地址的对齐方式是：

Bit[15：0]															
0	0	0	0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

其他 DMA 设置参考 DMAC2 章节。

7.1.3.8 通知机制

GPADC 在结束采样转换的时会产生中断，上报给 CPU。

该中断可以通过给寄存器 GPADC_IRQ 的 GPADC_IMR 比特置 1 来屏蔽。

该中断可以通过给寄存器 GPADC_IRQ 的 GPADC_ICR 比特置 1 来清中断。

7.1.3.9 配置启动流程

使用 GPADC 一般经过以下流程：

- 配置 PINMUX。
- 配置 GPADC 时钟频率，输入通路选择等信息。
- 将寄存器 ADC_CFG_REG1 中的 ANAU_GPADC_EN_BG 比特置 1 使能 Bandgap。
- 将寄存器 ADC_CFG_REG1 中的 ANAU_GPADC_LDOREF_EN 比特置 1 使能给 GPADC 提供参考电压的 LDO。
- 触发 GPADC。

过程需要满足一些电路稳定时间。

- Pinmux 配置后，PAD 连到输入通道的电压需要一定的稳定时间。
- 打开 bandgap 后，再打开提供参考电压的 LDO, LDO 需要 200us 稳定时间。
- 最后通过写寄存器触发或 Timer 触发启动 GPADC。

7.1.4 GPADC 寄存器

表 7-1: GPADC 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00			**ADC_CFG_REG1**	**ADC Analog Config Register 1**
[31:20]			RSVD	
[19]	rw	1'h0	ANAU_GPADC_LDOREF_EN	Enable LDO for ADC VREF
[18:15]			RSVD	
[14:12]	rw	3'h1	ANAU_GPADC_SEL_PCH	Select P-side input channel for GPADC, 0 for channel 0, 7 for channel 7, effective when force on
[11:9]	rw	3'h0	ANAU_GPADC_SEL_NCH	Select N-side input channel for GPADC, 0 for channel 0, 7 for channel 7, effective when force on
[8]			RSVD	
[7]	rw	1'h0	ANAU_GPADC_SE	Set GPADC in single-ended mode, signal range at P-input: 0 VREF
[6]	rw	1'h0	ANAU_GPADC_EN_V18	0：GPADC is powered with 3.3V supply, 1: GPADC is powered with 1.8V supply
[5:2]			RSVD	
[1]	rw	1'h0	ANAU_GPADC_EN_BG	Enable GPADC bandgap
[31:20]			RSVD	
0x04			**ADC_Slot0_REG**	**ADC Slot0 Config Register**
[31:14]			RSVD	
[13:11]	rw	3'h1	NCHNL_SEL	

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表 7-1: GPADC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[10:8]	rw	3'h0	PCHNL_SEL	
[7:1]			RSVD	
[0]	rw	1'h1	SLOT_EN	
0x08			**ADC_Slot1_REG**	**ADC Slot1 Config Register**
[31:14]			RSVD	
[13:11]	rw	3'h1	NCHNL_SEL	
[10:8]	rw	3'h0	PCHNL_SEL	
[7:1]			RSVD	
[0]	rw	1'h1	SLOT_EN	
0x0C			**ADC_Slot2_REG**	**ADC Slot2 Config Register**
[31:14]			RSVD	
[13:11]	rw	3'h1	NCHNL_SEL	
[10:8]	rw	3'h0	PCHNL_SEL	
[7:1]			RSVD	
[0]	rw	1'h1	SLOT_EN	
0x10			**ADC_Slot3_REG**	**ADC Slot3 Config Register**
[31:14]			RSVD	
[13:11]	rw	3'h1	NCHNL_SEL	
[10:8]	rw	3'h0	PCHNL_SEL	
[7:1]			RSVD	
[0]	rw	1'h1	SLOT_EN	
0x14			**ADC_Slot4_REG**	**ADC Slot4 Config Register**
[31:14]			RSVD	
[13:11]	rw	3'h1	NCHNL_SEL	
[10:8]	rw	3'h0	PCHNL_SEL	
[7:1]			RSVD	
[0]	rw	1'h1	SLOT_EN	
0x18			**ADC_Slot5_REG**	**ADC Slot5 Config Register**
[31:14]			RSVD	
[13:11]	rw	3'h1	NCHNL_SEL	
[10:8]	rw	3'h0	PCHNL_SEL	
[7:1]			RSVD	
[0]	rw	1'h1	SLOT_EN	
0x1C			**ADC_Slot6_REG**	**ADC Slot6 Config Register**
[31:14]			RSVD	
[13:11]	rw	3'h1	NCHNL_SEL	
[10:8]	rw	3'h0	PCHNL_SEL	
[7:1]			RSVD	
[0]	rw	1'h1	SLOT_EN	
0x20			**ADC_Slot7_REG**	**ADC Slot7 Config Register**
[31:19]			RSVD	
[13:11]	rw	3'h1	NCHNL_SEL	
[10:8]	rw	3'h0	PCHNL_SEL	
[7:1]			RSVD	
[0]	rw	1'h1	SLOT_EN	
0x24			**ADC_RDATA0**	**ADC Read Data0**
[31:28]			RSVD	
[27:16]	r	12'h0	SLOT1_RDATA	

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表 7-1: GPADC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[15:12]			RSVD	
[11:0]	r	12'h0	SLOT0_RDATA	
0x28			**ADC_RDATA1**	**ADC Read Data1**
[31:28]			RSVD	
[27:16]	r	12'h0	SLOT3_RDATA	
[15:12]			RSVD	
[11:0]	r	12'h0	SLOT2_RDATA	
0x2C			**ADC_RDATA2**	**ADC Read Data2**
[31:28]			RSVD	
[27:16]	r	12'h0	SLOT5_RDATA	
[15:12]			RSVD	
[11:0]	r	12'h0	SLOT4_RDATA	
0x30			**ADC_RDATA3**	**ADC Read Data3**
[31:28]			RSVD	
[27:16]	r	12'h0	SLOT7_RDATA	
[15:12]			RSVD	
[11:0]	r	12'h0	SLOT6_RDATA	
0x34			**ADC_DMA_RDATA**	**ADC Read Data For DMA**
[31:12]			RSVD	
[11:0]	r	12'h0	DMA_RDATA	
0x38			**ADC_CTRL_REG**	**ADC Control Register**
[31:21]			RSVD	
[20:17]	rw	4'h4	DATA_SAMP_DLY	
[16:15]			RSVD	
[14:12]	rw	3'h0	TIMER_TRIG_SRC_SEL	Timer trigger source select
[11]	rw	1'b0	FRC_EN_ADC	Manually enable GPADC core，or it will be enabled by setting ADC_START
[10]	rw	1'b0	CHNL_SEL_FRC_EN	Enable input channel setting in ADC_CFG_REG1
[9]	rw	1'b1	TIMER_TRIG_EN	Enable timer trigger function
[8]			RSVD	
[7]	rw	1'b1	DMA_EN	Enable DMA interface
[6:3]	rw	4'h6	INIT_TIME	GPADC will wait INIT_TIME ADCCLK cycles to start sample/conversion after being trigged
[2]	rw	1'b0	ADC_STOP	Write 1 to stop GPADC in continuous mode(need write 0 to clear)
[1]	w1s	1'b0	ADC_START	Write 1 to start GPADC,(don't need clear)
[0]	rw	1'b0	ADC_OP_MODE	0: single conversion mode 1: continuous conversion mode
0x3C		**0x0000_0130**	**ADC_CTRL_REG2**	**ADC Control Register2**
[31:24]	rw	8'h80	CONV_WIDTH	
[23:0]	rw	24'h8000	SAMP_WIDTH	
0x44		**0x0000_0000**	**GPADC_IRQ**	**GPADC IRQ Register**
[31:4]		28'h0	RSVD	
[3]	r	1'b0	GPADC_ISR	IRQ to CPU, = GPADC_IRSR&(! GPADC_IMR)
[2]	r	1'b0	GPADC_IRSR	IRQ before mask
[1]	rw	1'b0	GPADC_IMR	1: mask IRQ to CPU
[0]	w1s	1'b0	GPADC_ICR	1: clear GPADC_IRSR

8 定时器

8.1 ATIM

8.1.1 简介

ATIM (Advanced Timer) 基于一个 32 比特计数器，可实现计时、测量输入信号的脉冲长度 (输入捕获) 或者产生输出波形 (输出比较和 PWM) 等功能。ATIM 支持 6 路带死区保护的 PWM 互补输出，支持多路 PWM 同时换相，并有 2 路刹车输入可快速将输出切换至安全状态。计数器本身可以进行递增、递减或者递增/递减计数，计数时钟可选系统 PCLK、IO 输入信号或级联输入信号，并可进行 1~65536 倍的预分频。ATIM 共有 6 个通道，可以分别独立配置为输入捕获或输出模式。计数、输入捕获和输出比较的结果可以产生中断、DMA 请求或 PTC 事件。ATIM 包含主从模式接口，可以进行多级级联，实现多级计数或同步触发等功能。

8.1.2 主要特性

- 32 位递增、递减、递增/递减自动重装载计数器
- 16 位可编程 (可以实时修改) 预分频器，计数器时钟频率的分频系数为 1~65536 之间的任意数值
- 16 位可配置重复计数
- 支持单笔计数模式 (OPM)，当重复计数完成后自动停止计数器
- 6 个独立通道
  - 通道 1~3 可分别配置为输入或输出模式，其中每个通道可输出两路带死区保护的互补 PWM
  - 通道 4 可配置为输入或输出模式，可输出单路 PWM
  - 通道 5~6 可配置为输出比较模式
- 输入模式
  - 上升沿/下降沿捕获
  - PWM 脉宽和周期捕获 (需占用两个通道)
  - 可选 4 个输入端口之一或 1 个外部触发端口，支持防抖动滤波和预降频
- 输出模式
  - 强制输出高/低电平
  - 计数到比较值时输出高/低/翻转电平
  - PWM 输出，可配脉宽和周期
  - 多通道 PWM 组合输出，可产生有相互关系的多路 PWM
  - 单脉冲/重触发单脉冲模式输出
- 主从模式
  - 支持多计数器互连，可在作为主设备产生控制信号的同时，作为从设备被外部输入或其它主设备控制
  - 控制模式包括复位、触发、门控等
  - 支持多计数器同步启动、复位等
- 编码模式输入，控制计数器递增/递减计数
- 支持用于定位的霍尔传感器电路
- 2 路刹车输入，支持防抖动滤波，可将输出快速置于安全状态。刹车信号源包括：

- CPU 异常
- 比较器
- 外部输入
- 软件触发

• 如下事件发生时产生中断/DMA 请求/PTC 触发：
- 更新：计数器递增溢出/递减溢出，计数器初始化 (通过软件或者内部/外部触发)
- 触发事件 (计数器启动、停止、初始化或者由内部/外部触发计数)
- 输入捕获
- 输出比较
- 刹车
- 换相

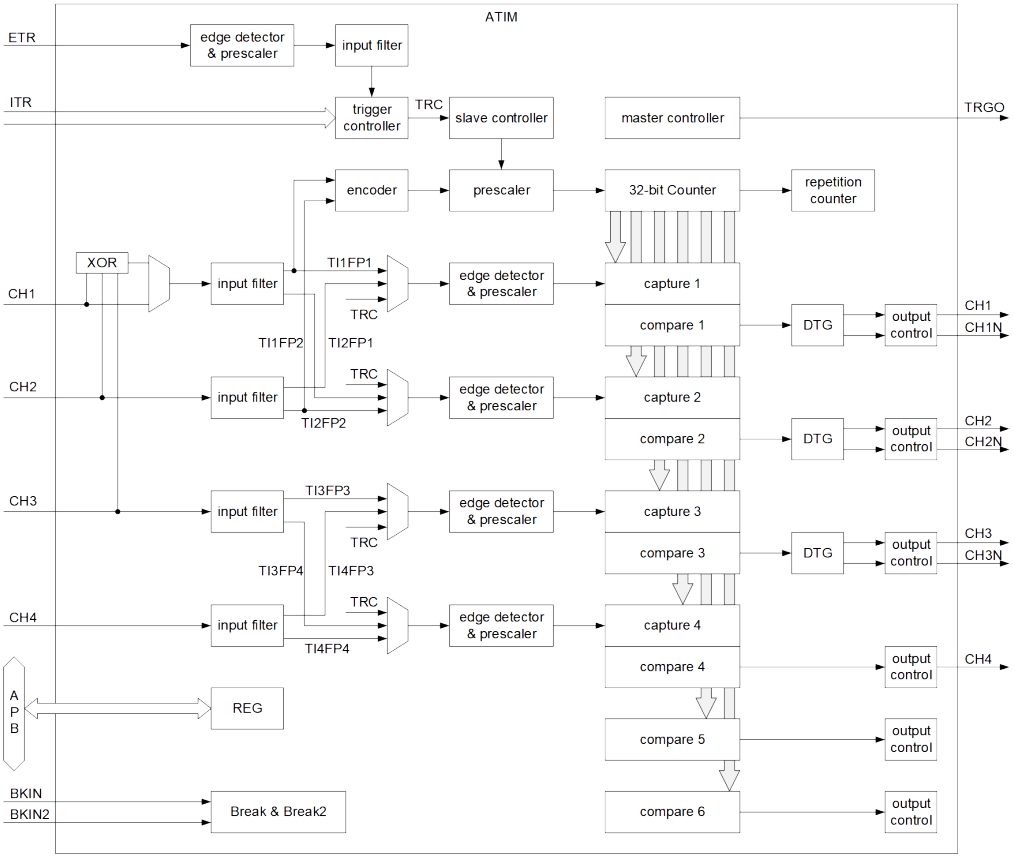


图 8-1: ATIM 结构图

8.1.3 ATIM 功能描述

8.1.3.1 计数器

ATIM 的各项功能均基于一个 32 比特的计数器。计数器基于事件计数，最基本的事件是一个 PCLK 时钟的翻转。根据不同配置，其它计数事件包括外部输入的翻转、其它定时器的输出翻转、正交编码器接口解码输出等。

计数事件经过预分频处理才会真正进入计数器。预分频的次数介于 1 到 65536 之间 (PSC+1)，即仅当发生了 (PSC+1) 次计数事件，计数器的值才真正改变一次。

计数器共有三种计数模式：递增，递减以及中心对齐。在递增计数模式下 (CR1_CMS=0 且 CR1_DIR=0)，计数器从 0 计数到自动重载值 ARR，然后重新从 0 开始计数并产生计数器上溢事件。在递减计数模式下 (CR1_CMS=0 且 CR1_DIR=1)，计数器从 ARR 开始递减计数到 0，然后重新从 ARR 开始计数并产生计数器下溢事件。在中心对齐模式下 (CR1_CMS 不为 0)，计数器从 0 开始计数到 ARR-1，产生计数器上溢事件，然后从 ARR 开始向下计数到 1 并产生计数器下溢事件，之后从 0 开始重新计数。

计数值可以通过 CNT 读出。计数的方向可以从 CR1_DIR 读出。

8.1.3.2 更新事件 (UEV)

更新事件用于标志一个计数单元的结束。最基本的更新事件产生于每次计数器上溢或下溢时 (未开启重复计数时)。软件将 EGR_UG 置 1 时，也将产生更新事件。更新事件可以产生中断、DMA 请求以及 PTC 触发，是定时器最基本的一项通知功能。

通过软件将 CR1_UDIS 置 1 可禁止产生更新事件。这可避免向预装载寄存器写入新值时更新影子寄存器。在 UDIS 位写入 0 之前不会产生任何更新事件。

如果 CR1_URS（更新请求选择）已置 1，则将 EGR_UG 置 1 会生成更新事件，但不会将 UIF 标志置 1（因此，不会发送任何中断或 DMA 请求）。这样一来，如果在发生捕获事件时将计数器清零，将不会同时产生更新中断和捕获中断。

发生更新事件时，将重新装载 RCR，ARR 以及 PSC 寄存器，且将更新标志 SR_UIF 置 1（CR1_URS=0 时）。该功能可以保证修改这些计数器的基本参数不影响当前计数单元，在下一个计数周期才生效。

8.1.3.3 重复计数

如果配置了重复计数器 (RCR>0)，每次计数器上溢或下溢时重复计数器会递减，并仅当重复计数器为 0 时才产生更新事件。更新事件发生时，重复计数器会重新装载 RCR 的值。

重复计数器的当前值不能读出。

8.1.3.4 影子寄存器

对 RCR，ARR 以及 PSC 寄存器的修改不会直接体现在当前计数单元中，而是等到更新事件发生时才真正更新进去。在更新事件发生前，计数器真正使用的是影子寄存器中的值。这样即使在计数中动态改变这些寄存器的值，也不会影响到当前计数单元的完整性，对于 PWM 输出等应用场景很有意义。

如果 CR1_APRE 为 0，ARR 寄存器将在配置后实时生效，不用等到更新事件发生。

输出比较寄存器 CCRx 也有影子寄存器。当 CCMRx_OCxPE 为 0 时，配置的 CCRx 会立即生效，否则要等到更新事件发生时才生效。

8.1.3.5 主从模式

定时器可同时处于主模式与从模式。主模式是指该定时器可以输出 TRGO 信号至芯片上其它定时器的 ITR 输入，用于控制其它定时器的计数行为。从模式是指该定时器的计数行为受外部输入 ETR，其它定时器输出至该定时器的 ITR 信号，或定时器的通道输入 CHx 的控制。

多个定时器可通过主从模式实现定时器同步，以实现多级分频、同时启动、门控计数等功能。

主模式可在不同事件发生时输出 TRGO 信号，如更新、使能、输入捕获、输出比较等，由 CR2_MMS 选择。

从模式可以选择计数器复位、触发启动、计数使能、计数事件等行为，由 SMCR_SMS 选择。从模式依赖的触发信号 TRGI 可灵活配置，可以在 ETR，ITR 以及通道输入中选择，并可选择信号极性，进行预分频、滤波等操作。

- 定时器处于复位从模式 (SMCR_SMS=0100) 时，当 TRGI 发生变化时，计数器及其预分频器重新初始化。如果 CR1_URS 为 0，则会生成更新事件 UEV，然后所有预装载寄存器 ARR 和 CCRx 都将更新。
- 定时器处于门控从模式 (SMCR_SMS=0101) 时，当 TRGI 满足高电平或低电平要求时才进行计数，否则计数器不变。
- 定时器处于触发从模式 (SMCR_SMS=0110) 时，软件不需配置 CR1_CEN 开启计数，而是当 TRGI 满足特定触发要求时自动启动计数器。
- 定时器处于外部时钟从模式 (SMCR_SMS=0111) 时，计数事件修改为 TRGI 的上升沿，仅当 TRGI 发生翻转时才进行计数。
- 定时器处于复位触发从模式 (SMCR_SMS=1000) 时，TRGI 满足特定触发要求时复位计数器并自动重新开启。

8.1.3.6 通道输入输出

定时器的部分通道可以独立配置为输入捕获模式 (CCMRx_CCxS!=0) 或输出模式 (CCMRx_CCxS=0)。

在输入捕获模式下，通道在对应的触发信号有效时，将计数器的值记录进 CCRx，并产生中断等通知信号。该触发信号可在 ETR，ITR 以及通道输入 CHx 中选择，并可选择信号极性，进行预分频、滤波等操作。通道产生的通知信号包括中断、DMA 请求、PTC 触发等。输入捕获模式可实现记录外部信号改变的时刻、测量 PWM 周期和占空比等功能。

在输出模式下，通道将比较计数器的值与 CCRx 的大小，在通道输出 CHx/CHxN 上产生固定电平，或产生基于本通道以及其它通道比较结果的 PWM 输出信号，并产生中断等通知信号。产生 PWM 信号的脉冲个数、频率、占空比、相位等参数均可调节。多个通道还可以联合产生特定关系的 PWM 组合，如带死区保护的 6 路互补 PWM 等。通道产生的通知信号包括中断、DMA 请求、PTC 触发等。

在输出模式下，一旦出现紧急情况，可以通过断路输入信号 BKIN 和 BKIN2 紧急关闭输出使能，或将输出置于预设电平，以保护定时器连接的外部电路。

8.1.3.7 输入捕获模式

在输入捕获模式下，当通道相应的触发信号检测到跳变沿后，将使用 CCRx 来锁存计数器的值。发生捕获事件时，会将相应的 SR_CCxIF 标志置 1，并可发送中断、DMA 请求（如果已使能）或 PTC 触发信号。如果发生捕获事件时 SR_CCxIF 标志已处于高位，则会将重复捕获标志 SR_CCxOF 置 1。可通过软件将 SR_CCxIF 清零，方法是向 SR_CCxIF 写入 0，或读取存储在 CCRx 中的已捕获数据。向 SR_CCxOF 写入 0 后会将其清零。

以下示例说明了如何在 CH1 输入出现上升沿时将计数器的值捕获到 CCR1 中，具体操作步骤如下：

1. 选择有效输入：通道 1 要连接到 CH1 输入，因此向 CCMR1_CC1S 写入 01。
2. 根据连接到定时器的信号，对所需的输入滤波带宽进行配置。
   假设 CH1 信号边沿变化时，最多在 5 个 PCLK 周期内发生抖动，需将滤波带宽设置为大于 5 个 PCLK 周期。将 CCMR1_IC1F 设置为 0011(0x3)，则在检测到连续 8 个采样点（以 PCLK 频率采样）均为新电平后，可以确认 CH1 的跳变沿。

3. 将 CCER_CC1P 和 CCER_CC1NP 写 0，选择 CH1 上的有效转换边沿为上升沿。
4. 对输入预分频器进行编程。
   在本例中我们希望每次有效转换时都执行捕获操作，因此禁用预分频器（CCMR1_IC1PS 写 00）。
5. CCER_CC1E 置 1，使能通道 1，允许将计数器的值捕获到 CCR1 中。
6. 如果需要，可将 DIER_CC1IE 置 1 来使能相关中断请求，或将 DIER_CC1DE 置 1 来使能 DMA 请求。

配置完成后，通道将在 CH1 输入出现上升沿时执行下列操作：

1. CCR1 寄存器记录计数器的值。
2. SR_CCxIF 标志置 1（中断标志）。如果至少发生了两次连续捕获，但 SR_CCxIF 未被清零，这样 SR_CCxOF 捕获溢出标志会被置 1。
3. 根据 CCER_CC1IE 生成中断。
4. 根据 DIER_CC1DE 生成 DMA 请求。

要处理重复捕获，建议在读出 SR_CCxOF 之前读取数据。这样可避免丢失在读取 SR_CCxOF 之后与读取数据之前可能出现的重复捕获信息。

通过软件将 EGR_CCxG 置 1 可立即产生一次捕获，并生成通道捕获中断和 DMA 请求。

8.1.3.8 PWM 输入捕获

PWM 输入捕获是输入捕获的一种扩展应用，可用于测量 PWM 输入信号的周期和占空比。为实现该功能，需要将两个通道都配置为输入捕获模式，触发信号分别映射成输入 PWM 的正边沿和负边沿，并开启计数器复位的从模式。

以下示例说明了如何用通道 1 和通道 2 测量从 CH1 输入的 PWM 的周期和占空比，具体操作步骤如下：

1. 选择通道 1 的有效输入为 CH1 输入，因此向 CCMR1_CC1S 写入 01。
2. 选择通道 1 输入信号的有效极性（用于在 CCR1 中捕获和计数器清零），将 CCER_CC1P 和 CCER_CC1NP 写 0，选择 CH1 上的有效转换边沿为上升沿。
3. 选择通道 2 的有效输入也为 CH1 输入，向 CCMR1_CC2S 写入 10(0x2)。
4. 选择通道 2 输入信号的有效极性（用于 CCR2 捕获），将 CCER_CC2P 写 1，CCER_CC1NP 写 0，选择 CH1 上的有效转换边沿为下降沿。
5. 设置从模式控制信号为 CH1，向 SMCR_TS 写入 101(0x5)，选择 TI1FP1。
6. 将从模式控制器配置为复位模式，向 SMCR_SMS 写入 0100(0x4)。
7. 使能通道 1 和通道 2，将 CCER_CC1E 和 CCER_CC2E 置 1。

配置完成后，在每个 CH1 的上升沿，计数器的值被记录在 CCR1 中，同时计数器被复位并重新开始计数；在每个 CH1 的下降沿，计数器的值被记录在 CCR2 中。将 CCR1 的值乘以 PCLK 的周期，可以算出 PWM 的周期。将 CCR2 的值乘以 PCLK 的周期，可以算出 PWM 高电平持续的时间，从而得到 PWM 的占空比。

8.1.3.9 输出比较模式

在输出比较模式下，当计数值与 CCRx 满足一定关系时，可以在对应 CHx 及 CHxN 上产生特定输出，通常用于控制输出波形，或指示已经过某一时间段。

具体而言，通道将在 CCRx 与计数器之间相匹配时执行下列操作：

1. 将为相应的 CHx 和 CHxN 输出分配一个可编程值，该值由比较模式寄存器 CCMRx_OCxM 和输出极性寄存器 CCER_CCxP/CCxNP 定义。匹配时，输出引脚既可保持其电平（CCMRx_OCxM=0000），也可设置为有效电平 (CCMRx_OCxM=0001)、无效电平 (CCMRx_OCxM=0010) 或进行翻转 (CCMRx_OCxM=0011)。
2. 将中断状态寄存器标志 SR_CCxIF 置 1。
3. 根据 CCER_CC1IE 生成中断。
4. 根据 DIER_CC1DE 和 CR2_CCDS 生成 DMA 请求。

配置 CCMRx_OCxPE，可将 CCRx 寄存器配置为带或不带影子寄存器。当 CCMRx_OCxPE 为 0 时，软件修改 CCRx 实时生效，可通过在每次中断中修改下一次匹配的 CCRx 来实现自定义波形的输出。

将 BDTR_MOE 设为 1 后 CH 和 CHxN 输出才生效。

8.1.3.10 基础 PWM 输出

利用输出比较模式，定时器可以产生周期、占空比、相位可控的多路 PWM 输出。PWM 输出的周期由 ARR 决定，占空比由 CCRx 决定。PWM 输出有多种模式，由每个通道的 CCMRx_OCxM 各自独立选择。最基本的单路 PWM 输出只需要占用一个通道，采用基础的 PWM 模式即可实现。复杂的 PWM 信号，或 PWM 组合则需要占用多个通道，并需仔细分配每个通道的 PWM 模式以及 CCRx。

在基础的 PWM 模式下，计数器值 CNT 与 CCRx 进行比较，并根据计数器的当前计数方向产生包含有效电平或无效电平的比较输出信号 OCxREF。有效电平的极性可通过 CCER_CCxP 配置，并根据 CCER_CCxE 和 BDTR_MOE 等寄存器使能 CHx 输出。将 BDTR_MOE 设为 1 后 PWM 输出才生效。

如在递增计数模式下，配置 CCMR1_OC1M 和 CCMR1_OC2M 为 0110(0x6)，则 PWM 输出如图8-9。其中计数值 CNT 小于 CCR1/2 时，输出高电平，否则输出低电平。

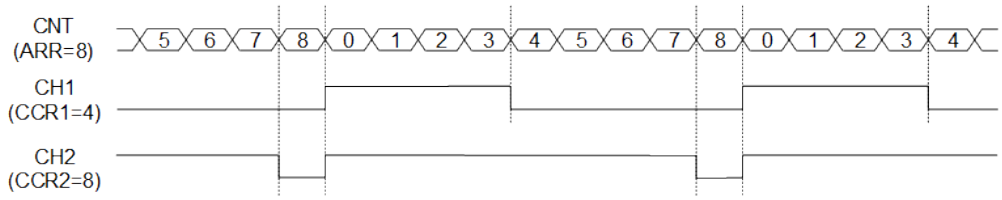


图 8-2: 递增计数模式下的 PWM 输出

如在中心对齐计数模式下，配置 CCMR1_OC1M 和 CCMR1_OC2M 为 0110(0x6)，则 PWM 输出如图8-10。其中递增阶段计数值 CNT 小于 CCR1/2 时，输出高电平，否则输出低电平；递减阶段计数值 CNT 大于 CCR1/2 时，输出低电平，否则输出高电平。

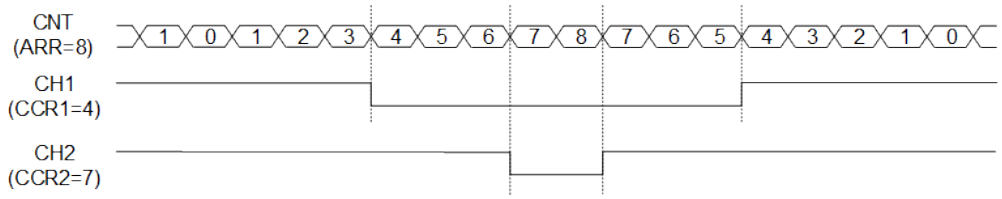


图 8-3: 中心对齐计数模式下的 PWM 输出

8.1.3.11 不对称 PWM 输出

在不对称 PWM 模式下，生成的两个 PWM 信号之间存在可编程相移。该模式仅限于计数器处于中心对齐模式时。生成的两个 PWM 信号频率相同，由 ARR 的值确定，而占空比和相移则各由一对 CCRx 寄存器确定。每一路输出 PWM 占用两个 CCRx 寄存器，分别控制递增计数和递减计数期间的行为，这样 PWM 的上升沿和下降沿时间点可以分别配置。CCR1 和 CCR2 共同控制 CH1/2 的输出，CCR3 和 CCR4 共同控制 CH3/4 的输出。

CH1/2 以及 CH3/4 可以独立选择不同的不对称 PWM 模式，配置 CCMRx_OCxM 为 1110(0xe) 或 1111(0xf)。

如配置 CCMR1_OC1M 和 CCMR2_OC3M 为 1110(0xe)，则 PWM 输出如图8-11。其中递增阶段 (0->ARR-1) 计数值 CNT 小于 CCR1/3 时，输出高电平，否则输出低电平；递减阶段 (ARR->1) 计数值 CNT 大于 CCR2/4 时，输出低电平，否则输出高电平。

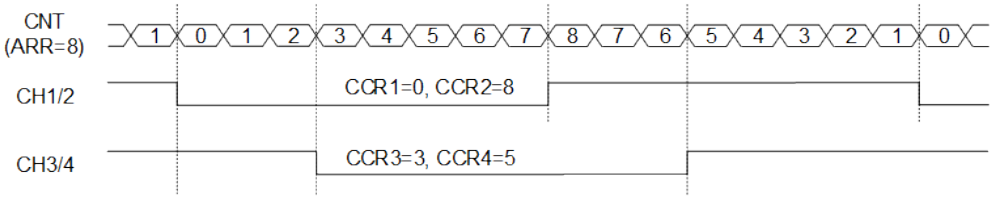


图 8-4: 不对称 PWM 输出

8.1.3.12 组合 PWM 输出

在组合 PWM 模式下，生成的两个 PWM 信号之间存在可编程延时和相移。计数器处于递增、递减或中心对齐模式均可，生成的两个 PWM 信号频率相同，由 ARR 的值确定，而占空比和相移则各由一对 CCRx 寄存器确定。每一路输出 PWM 占用两个 CCRx 寄存器，是由两路基础 PWM 输出波形的逻辑与运算或者逻辑或运算组合而成。CCR1 和 CCR2 共同控制 CH1/2 的输出，CCR3 和 CCR4 共同控制 CH3/4 的输出。

CH1/2 以及 CH3/4 可以独立选择不同的组合 PWM 模式，配置 CCMRx_OCxM 为 1100(0xc) 或 1101(0xd)。当 CH1 或 CH3 配置为组合 PWM 模式 1100(0xc) 时，CH2 或 CH4 必须配置为 0111(0x7) 或 1101(0xd) 或 1111(0xf)。当 CH1 或 CH3 配置为组合 PWM 模式 1101(0xd) 时，CH2 或 CH4 必须配置为 0110(0x6) 或 1100(0xc) 或 1110(0xe)。

如配置 CCMR1_OC1M 为 1101(0xd)，CCMR1_OC2M 为 0110(0x6)，CCMR2_OC3M 为 1100(0xc)，CCMR2_OC4M 为 0111(0x7)，则 PWM 输出如图8-12。其中计数值 CNT 小于 CCR1/4 时，OC1REF/OC4REF 为低电平，否则为高电平；计数值 CNT 小于 CCR2/3 时，OC2REF/OC3REF 为高电平，否则为低电平。CH1 输出是 OC1REF 和 OC2REF 的逻辑与运算。CH3 输出是 OC3REF 和 OC4REF 的逻辑或运算。

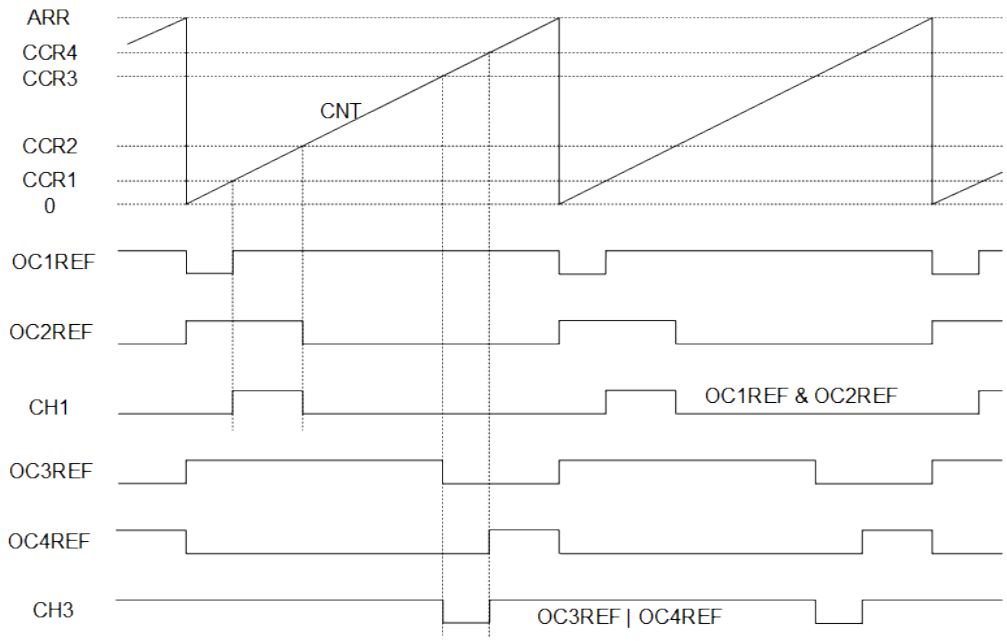


图 8-5: 组合 PWM 输出

8.1.3.13 带死区的互补 PWM 输出

ATIM 可以输出两路相位相反的互补 PWM 信号 CHx 与 CHxN，并在两路信号跳变的边沿插入一定延时。这段延时通常称为死区，用户必须根据与输出相连接的器件及其特性（如电平转换器的固有延迟、开关器件产生的延迟等）来调整死区时间。

ATIM 的通道 1/2/3 每个均可输出一组互补 PWM 信号，最多可同时输出 3 组共 6 路互补信号。其中每路输出可以通过 CCER_CCxP 和 CCER_CCxNP 独立选择输出极性。将 BDTR_MOE 以及对应通道的 CCER_CCxE 和 CCER_CCxNE 配置成 1 使能互补输出。

互补输出的示例如图8-6。CHx 的上升沿相对该通道产生的参考输出 OCxREF 的上升沿有一个死区时间的延时，而 CHxN 的上升沿相对该通道的 OCxREF 的下降沿有一个死区时间的延时。

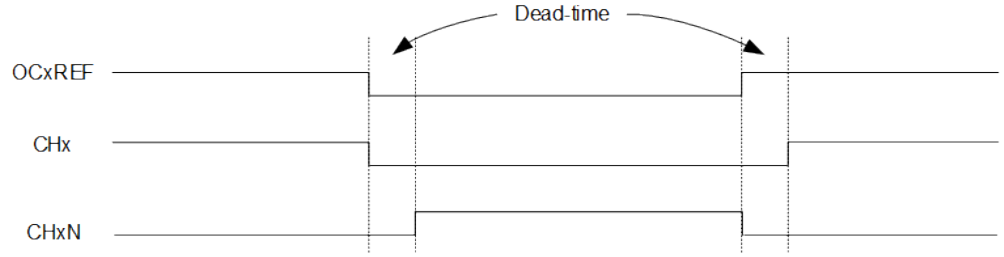


图 8-6: 带死区的互补 PWM 输出

死区时间在一定范围内可调节。当 BDTR_DTPSC 为 0 时，死区时间为 BDTR_DTG 乘以 PCLK 周期。当 BDTR_DTPSC 为 1 时，死区时间为 BDTR_DTG 乘以 16 倍 PCLK 周期。假如 PCLK 为 120MHz，死区时间可调范围为 0~136us。

8.1.3.14 紧急断路

断路功能的目的是保护由 ATIM 产生的 PWM 信号所驱动的功率开关。两个断路输入 BKIN 和 BKIN2 通常连接到功率级和三相逆变器的故障输出。激活时，断路电路会关闭 PWM 输出，并将其强制为预定义的安全状态。也可选择一些芯片内部事件来触发输出关断。BKIN 可以在死区持续时间后将输出强制为预定义的电平（有效或无效）。BKIN 能够将输出强制为无效状态。

断路期间的输出使能信号和输出电平取决于多个控制位：BDTR_MOE 允许通过软件使能/禁止输出；BDTR_OSSI 定义定时器将输出控制在无效状态下，还是释放控制权给 GPIO 控制器（通常使其处于高阻态模式）；CR2_OISx/OISxN 将输出设置为关断电平（有效或无效）。

ATIM 复位后，断路功能处于禁止状态，BDTR_MOE 处于低电平。将 BDTR_BKE/BKE2 置 1，可使能断路功能。可通过配置 BDTR_BKP/BKP2 选择断路输入的极性。也可由软件配置 EGR_BG/B2G 产生断路事件，不依赖于 BDTR_BKE/BKE2 的值。

断路电路内部还实施了写保护，用以保护应用的安全。通过该功能，用户可冻结多个参数配置，如死区持续时间、输出极性和禁止时的状态、PWM 模式、断路使能和极性等。该功能通过写 AF1_LOCK 寄存器实现，从 3 种保护级别中进行选择。

8.1.3.15 6 步 PWM

6 步 PWM 需要在 PWM 输出过程中的某一时刻同时切换各通道的 PWM 模式，可以通过 ATIM 的换向事件 (COM) 实现。当通道使用互补输出时，CCMRx_OCxM、CCER_CCxE 和 CCER_CCxNE 有预装载机制。用户可以预先编程下一步骤的配置，当发生换向事件时，预装载寄存器将传输到影子寄存器，同时更改所有通道的配置。COM 可由软件通过将 EGR_COM 置 1 生成，也可以由硬件在输入触发信号的上升沿生成。发生换向事件时，SR_COMIF 将会置 1。这时，如果 DIER_COMIE 为 1，将产生中断；如果 DIER_COMDE 为 1，将产生 DMA 请求。

8.1.3.16 单脉冲模式

将 CR1_OPM 写 1 可以使能单脉冲模式。该模式下计数器启动以后一旦发生更新事件，就会自动停止计数。该模式可以用于单次计数，或在一个激励信号的触发下启动，并在一段可编程的延时后产生一个脉宽可编程的脉冲。

例如，希望实现这样的功能，在 CH2 输入引脚检测到上升沿时，经过一定时间延迟，在 CH1 上产生单个一定宽度的正脉冲。配置方法如下：

1. CCMR1_CC2S=01，以将 TI2FP2 映射到通道 2。
2. CCER_CCxP 和 CCER_CCxNP 写 0，TI2FP2 反应 CH2 上升沿的变化。
3. SMCR_TS=110(0x6)，将 TI2FP2 配置为从模式控制器的触发 TRGI。
4. SMCR_SMS=110(0x6)，将从模式控制器配置为触发模式，触发后开启计数。
5. 根据需要的时间延迟与脉冲宽度配置 ARR 与 CCR1，定义时间延迟与脉冲宽度。
6. CCMR1_OC1M=0111(0x7)，配置为正脉冲 PWM。
7. CR1_OPM=1，一次触发只产生一个脉冲。
8. EGR_UG=1，手动刷新 ARR 与 CCR1 寄存器。

从模式为触发模式时不需要手动使能 CR1_CEN，一旦检测到触发信号生效，计数器就会自动使能。

8.1.3.17 编码器接口模式

编码器接口模式下，通道 1 和通道 2 可以用于连接外部正交编码器，将外部编码器的信号转化为定时器的计数值变化，从而获知外部编码器的工作状态。

如果计数器仅在 CH1 边沿处计数，SMCR_SMS 配置为 0001；如果计数器仅在 CH2 边沿处计数，SMCR_SMS 配置为 0010(0x2)；如果计数器在 CH1 和 CH2 边沿处均计数，SMCR_SMS 配置为 0011(0x3)。CCER_CC1P/CC2P 用于选择 CH1 和 CH2 极性。如果需要，还可对输入滤波器进行编程。两个输入的信号转换序列会产生计数脉冲和方向信号，根据该信号转换序列，计数器相应递增或递减计数，同时硬件对 CR1_DIR 进行相应修改。

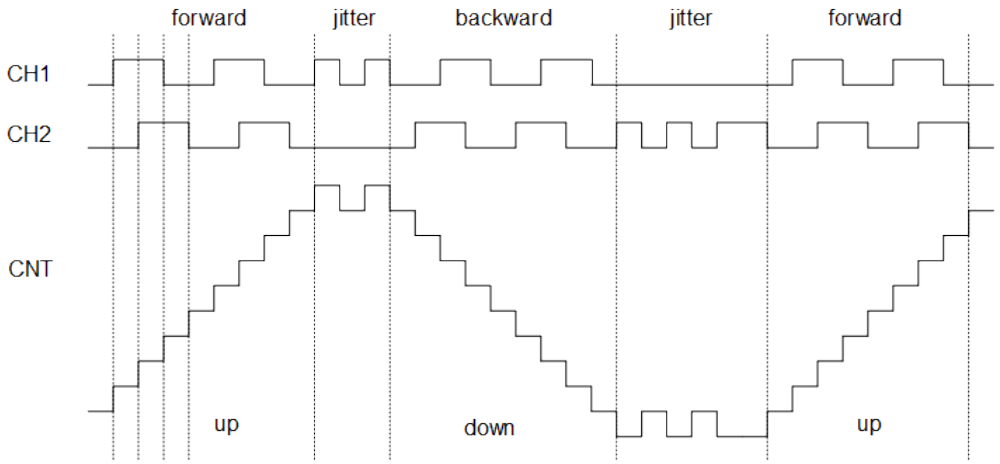
编码器接口模式下，计数器的计数事件是正交编码器接口的解码输出。计数器仅在 0 到 ARR 之间进行连续计数（根据计数的具体方向，从 0 递增计数到 ARR，或从 ARR 递减计数到 0）。因此，在启动前必须先配置 ARR。同样，捕获、比较、重复计数器和触发输出功能继续正常工作。在此模式下，计数器会根据正交编码器的速度和方向自动进行修改，因此，其内容始终表示编码器的位置。计数方向对应于所连传感器的旋转方向。下表汇总了可能的组合（假设 CH1 和 CH2 不同时切换）。

SMCR_SMS	条件	CH1 上升沿	CH1 上升沿	CH2 上升沿	CH2 上升沿
0001 或 0011	CH2=0	递增	递减	/	/
	CH2=1	递减	递增	/	/
0010 或 0011	CH1=0	/	/	递减	递增
	CH1=1	/	/	递增	递减

下图示意了计数器如何根据正交编码器的信号变化进行计数的，配置如下：

CCMR1_CC1S=01（CH1 映射到通道 1 上），CCMR2_CC2S=01（CH2 映射到通道 2 上），

CCER_CC1P/CC1NP/CC2P/CC2NP=0，SMCR_SMS=0011(0x3)，CR1_CEN=1。



8.1.3.18 定时器同步

多个定时器可通过主从模式连接在一起，实现定时器同步，以完成多级分频、同时启动、门控计数等功能。

将主模式定时器的 TRGO 设置为更新事件 (CR2_MMS=010)，连接至另一个设置为外部时钟从模式 (SMCR_SMS = 0111) 的定时器，可以实现定时器级联计数。此时主模式定时器相当于从模式定时器的预分频，计数总位宽等

于两个定时器各自的位宽相加。

将主模式定时器的 TRGO 设置为计数使能 (CR2_MMS=001)，连接至另一个设置为触发从模式 (SMCR_SMS=0110) 的定时器，可以实现定时器同步启动，从而对齐多个定时器的开启时机。

将主模式定时器的 TRGO 设置为比较输出 (CR2_MMS=100)，连接至另一个设置为门控从模式 (SMCR_SMS=0101) 的定时器，可以实现门控 PWM 输出。主模式定时器可以对从模式定时器输出的 PWM 载波进行调制输出。

8.1.3.19 通知机制

ATIM 能够产生中断、DMA 请求、PTC 触发等多种通知机制。能够触发通知的事件主要包括更新事件、触发事件、比较器匹配、输入捕获、断路输入、换向事件等。DIER 寄存器可以控制各种事件是否产生中断和 DMA 请求。各事件状态可在 SR 寄存器中查询。

8.1.4 ATIM 寄存器

表 8-1: ATIM 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00		**0x00000000**	**CR1**	**TIM control register 1**
[31:12]		20'h0	RSVD	
[11]	rw	1'h0	UIFREMAP	UIF status bit remapping 0: No remapping. UIF status bit is not copied to CNT register bit 31 1: Remapping enabled. UIF status bit is copied to CNT register bit 31.
[10:8]		3'h0	RSVD	
[7]	rw	1'h0	ARPE	Auto-reload preload enable 0: ARR register is not buffered 1: ARR register is buffered
[6:5]	rw	2'h0	CMS	Center-aligned mode selection 00: Edge-aligned mode. The counter counts up or down depending on the direction bit (DIR). 01: Center-aligned mode 1. The counter counts up and down alternatively. Output compare interrupt flags of channels configured in output (CCxS=00 in CCMRx register) are set only when the counter is counting down. 10: Center-aligned mode 2. The counter counts up and down alternatively. Output compare interrupt flags of channels configured in output (CCxS=00 in CCMRx register) are set only when the counter is counting up. 11: Center-aligned mode 3. The counter counts up and down alternatively. Output compare interrupt flags of channels configured in output (CCxS=00 in CCMRx register) are set both when the counter is counting up or down.
[4]	rw	1'h0	DIR	Direction 0: Counter used as upcounter 1: Counter used as downcounter
[3]	rw	1'h0	OPM	One-pulse mode 0: Counter is not stopped at update event 1: Counter stops counting at the next update event (clearing the bit CEN)

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表 8-1: ATIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[2]	rw	1'h0	URS	Update request source This bit is set and cleared by software to select the UEV event sources. 0: Any of the following events generate an update interrupt or DMA request if enabled. These events can be: –Counter overflow/underflow –Setting the UG bit –Update generation through the slave mode controller 1: Only counter overflow/underflow generates an update interrupt or DMA request if enabled.
[1]	rw	1'h0	UDIS	Update disable This bit is set and cleared by software to enable/disable UEV event generation. 0: UEV enabled. The Update (UEV) event is generated by one of the following events: –Counter overflow/underflow –Setting the UG bit –Update generation through the slave mode controller Buffered registers are then loaded with their preload values. 1: UEV disabled. The Update event is not generated, shadow registers keep their value (ARR, PSC, CCRx). However the counter and the prescaler are reinitialized if the UG bit is set or if a hardware reset is received from the slave mode controller.
[0]	rw	1'h0	CEN	Counter enable 0: Counter disabled 1: Counter enabled External clock, gated mode and encoder mode can work only if the CEN bit has been previously set by software. However trigger mode can set the CEN bit automatically by hardware. CEN is cleared automatically in one-pulse mode, when an update event occurs.
0x04		**0x00000000**	**CR2**	**TIM control register 2**
[31:19]		13'h0	RSVD	
[18]	rw	1'h0	OIS6	Output Idle state 6 (OC6 output)
[17]		1'h0	RSVD	
[16]	rw	1'h0	OIS5	Output Idle state 5 (OC5 output)
[15]		1'h0	RSVD	
[14]	rw	1'h0	OIS4	Output Idle state 4 (OC4 output)
[13]	rw	1'h0	OIS3N	Output Idle state 3 (OC3N output)
[12]	rw	1'h0	OIS3	Output Idle state 3 (OC3 output)
[11]	rw	1'h0	OIS2N	Output Idle state 2 (OC2N output)
[10]	rw	1'h0	OIS2	Output Idle state 2 (OC2 output)
[9]	rw	1'h0	OIS1N	Output Idle state 1 (OC1N output) 0: OC1N=0 after a dead-time when MOE=0 1: OC1N=1 after a dead-time when MOE=0 This bit, as well as other OISxN, can not be modified as long as LOCK level 1, 2 or 3 has been programmed
[8]	rw	1'h0	OIS1	Output Idle state 1 (OC1 output) 0: OC1=0 (after a dead-time if OC1N is implemented) when MOE=0 1: OC1=1 (after a dead-time if OC1N is implemented) when MOE=0 This bit, as well as other OISx, can not be modified as long as LOCK level 1, 2 or 3 has been programmed

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表 8-1: ATIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[7]	rw	1'h0	TI1S	TI1 selection 0: The CH1 pin is connected to TI1 input 1: The CH1, CH2 and CH3 pins are connected to the TI1 input (XOR combination)
[6:4]	rw	3'h0	MMS	Master mode selection These bits allow to select the information to be sent in master mode to slave timers for synchronization (TRGO). The combination is as follows: 000: Reset - the UG bit from the EGR register is used as trigger output (TRGO). If the reset is generated by the trigger input (slave mode controller configured in reset mode) then the signal on TRGO is delayed compared to the actual reset. 001: Enable - the Counter enable signal, CNT_EN, is used as trigger output (TRGO). It is useful to start several timers at the same time or to control a window in which a slave timer is enabled. The Counter Enable signal is generated by a logic OR between CEN control bit and the trigger input when configured in gated mode. When the Counter Enable signal is controlled by the trigger input, there is a delay on TRGO, except if the master/slave mode is selected. 010: Update - The update event is selected as trigger output (TRGO). For instance a master timer can then be used as a prescaler for a slave timer. 011: Compare Pulse - The trigger output send a positive pulse when the CC1IF flag is to be set (even if it was already high), as soon as a capture or a compare match occurred. (TRGO) 100: Compare - OC1REFC signal is used as trigger output (TRGO) 101: Compare - OC2REFC signal is used as trigger output (TRGO) 110: Compare - OC3REFC signal is used as trigger output (TRGO) 111: Compare - OC4REFC signal is used as trigger output (TRGO)
[3]	rw	1'h0	CCDS	Capture/compare DMA selection 0: CCx DMA request sent when CCx event occurs 1: CCx DMA requests sent when update event occurs
[2]	rw	1'h0	CCUS	Capture/compare control update selection 0: When capture/compare control bits are preloaded (CCPC=1), they are updated by setting the COMG bit only 1: When capture/compare control bits are preloaded (CCPC=1), they are updated by setting the COMG bit or when an edge occurs on TRGI after Trigger selection This bit acts only on channels that have a complementary output.
[1]		1'h0	RSVD	
[0]	rw	1'h0	CCPC	Capture/compare preloaded control 0: CCxE, CCxNE and OCxM bits are not preloaded 1: CCxE, CCxNE and OCxM bits are preloaded, after having been written, they are updated only when a commutation event (COM) occurs (COMG bit set or edge detected on TRGI after Trigger selection, depending on the CCUS bit). This bit acts only on channels that have a complementary output.
0x08		**0x00000000**	**SMCR**	**TIM slave mode control register**
[31:20]		12'h0	RSVD	

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表 8-1: ATIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[19:16]	rw	4'h0	SMS	Slave mode selection When external signals are selected the active edge of the trigger signal (TRGI) is linked to the polarity selected on the external input. 0000: Slave mode disabled. 0001: Encoder mode 1 - Counter counts up/down on TI1FP1 edge depending on TI2FP2 level. 0010: Encoder mode 2 - Counter counts up/down on TI2FP2 edge depending on TI1FP1 level. 0011: Encoder mode 3 - Counter counts up/down on both TI1FP1 and TI2FP2 edges depending on the level of the other input. 0100: Reset Mode - Rising edge of the selected trigger input (TRGI) reinitializes the counter and generates an update of the registers. 0101: Gated Mode - The counter clock is enabled when the trigger input (TRGI) is high. The counter stops (but is not reset) as soon as the trigger becomes low. Both start and stop of the counter are controlled. 0110: Trigger Mode - The counter starts at a rising edge of the trigger TRGI (but it is not reset). Only the start of the counter is controlled. 0111: External Clock Mode 1 - Rising edges of the selected trigger (TRGI) clock the counter. 1000: Combined reset + trigger mode - Rising edge of the selected trigger input (TRGI) reinitializes the counter, generates an update of the registers and starts the counter.
[15]	rw	1'h0	ETP	External trigger polarity This bit selects whether ETR or ETR is used for trigger operations 0: ETR is non-inverted, active at high level or rising edge 1: ETR is inverted, active at low level or falling edge
[14]	rw	1'h0	ECE	External clock enable This bit enables External clock mode 2. 0: External clock mode 2 disabled 1: External clock mode 2 enabled. The counter is clocked by any active edge on the ETRF signal.
[13:12]	rw	2'h0	ETPS	External trigger prescaler External trigger signal ETRP frequency must be at most 1/4 of CK_INT frequency. A prescaler can be enabled to reduce ETRP frequency. It is useful when inputting fast external clocks. 00: Prescaler OFF 01: ETRP frequency divided by 2 10: ETRP frequency divided by 4 11: ETRP frequency divided by 8

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表 8-1: ATIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[11:8]	rw	4'h0	ETF	External trigger filter This bit-field then defines the frequency used to sample ETRP signal and the length of the digital filter applied to ETRP. The digital filter is made of an event counter in which N consecutive events are needed to validate a transition on the output: 0000: No filter, sampling is done at fCLK 0001: fSAMPLING=fCLK, N=2 0010: fSAMPLING=fCLK, N=4 0011: fSAMPLING=fCLK, N=8 0100: fSAMPLING=fCLK/2, N=6 0101: fSAMPLING=fCLK/2, N=8 0110: fSAMPLING=fCLK/4, N=6 0111: fSAMPLING=fCLK/4, N=8 1000: fSAMPLING=fCLK/8, N=6 1001: fSAMPLING=fCLK/8, N=8 1010: fSAMPLING=fCLK/16, N=5 1011: fSAMPLING=fCLK/16, N=6 1100: fSAMPLING=fCLK/16, N=8 1101: fSAMPLING=fCLK/32, N=5 1110: fSAMPLING=fCLK/32, N=6 1111: fSAMPLING=fCLK/32, N=8
[7]	rw	1'h0	MSM	Master/Slave mode 0: No action 1: The effect of an event on the trigger input (TRGI) is delayed to allow a perfect synchronization between the current timer and its slaves (through TRGO). It is useful if we want to synchronize several timers on a single external event.
[6:4]	rw	3'h0	TS	Trigger selection This bit-field selects the trigger input to be used to synchronize the counter. 000: Internal Trigger 0 (ITR0) 001: Internal Trigger 1 (ITR1) 010: Internal Trigger 2 (ITR2) 011: Internal Trigger 3 (ITR3) 100: TI1 Edge Detector (TI1F_ED) 101: Filtered Timer Input 1 (TI1FP1) 110: Filtered Timer Input 2 (TI2FP2) 111: External Trigger input (ETRF)
[3:0]		4'h0	RSVD	
0x0C		**0x00000000**	**DIER**	**TIM DMA/Interrupt enable register**
[31:18]		14'h0	RSVD	
[17]	rw	1'h0	CC6IE	Capture/Compare 6 interrupt enable 0: CC6 interrupt disabled. 1: CC6 interrupt enabled
[16]	rw	1'h0	CC5IE	Capture/Compare 5 interrupt enable 0: CC5 interrupt disabled. 1: CC5 interrupt enabled
[15]		1'h0	RSVD	
[14]	rw	1'h0	TDE	Trigger DMA request enable 0: Trigger DMA request disabled. 1: Trigger DMA request enabled.

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表 8-1: ATIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[13]	rw	1'h0	COMDE	COM DMA request enable 0: COM DMA request disabled 1: COM DMA request enabled
[12]	rw	1'h0	CC4DE	Capture/Compare 4 DMA request enable 0: CC4 DMA request disabled. 1: CC4 DMA request enabled
[11]	rw	1'h0	CC3DE	Capture/Compare 3 DMA request enable 0: CC3 DMA request disabled. 1: CC3 DMA request enabled.
[10]	rw	1'h0	CC2DE	Capture/Compare 2 DMA request enable 0: CC2 DMA request disabled. 1: CC2 DMA request enabled.
[9]	rw	1'h0	CC1DE	Capture/Compare 1 DMA request enable 0: CC1 DMA request disabled. 1: CC1 DMA request enabled.
[8]	rw	1'h0	UDE	Update DMA request enable 0: Update DMA request disabled. 1: Update DMA request enabled
[7]	rw	1'h0	BIE	Break interrupt enable 0: Break interrupt disabled 1: Break interrupt enabled
[6]	rw	1'h0	TIE	Trigger interrupt enable 0: Trigger interrupt disabled. 1: Trigger interrupt enabled
[5]	rw	1'h0	COMIE	COM interrupt enable 0: COM interrupt disabled 1: COM interrupt enabled
[4]	rw	1'h0	CC4IE	Capture/Compare 4 interrupt enable 0: CC4 interrupt disabled. 1: CC4 interrupt enabled
[3]	rw	1'h0	CC3IE	Capture/Compare 3 interrupt enable 0: CC3 interrupt disabled. 1: CC3 interrupt enabled
[2]	rw	1'h0	CC2IE	Capture/Compare 2 interrupt enable 0: CC2 interrupt disabled. 1: CC2 interrupt enabled.
[1]	rw	1'h0	CC1IE	Capture/Compare 1 interrupt enable 0: CC1 interrupt disabled. 1: CC1 interrupt enabled
[0]	rw	1'h0	UIE	Update interrupt enable 0: Update interrupt disabled. 1: Update interrupt enabled
0x10		**0x00000000**	**SR**	**TIM status register**
[31:18]		14'h0	RSVD	
[17]	rw0c	1'h0	CC6IF	Compare 6 interrupt flag
[16]	rw0c	1'h0	CC5IF	Compare 5 interrupt flag
[15]		1'h0	RSVD	
[14]		1'h0	RSVD	

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表 8-1: ATIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[13]	rw0c	1'h0	SBIF	System Break interrupt flag This flag is set by hardware as soon as the system break input goes active. It can be cleared by software if the system break input is not active. This flag must be reset to re-start PWM operation. 0: No break event occurred. 1: An active level has been detected on the system break input. An interrupt is generated if BIE=1 in the DIER register.
[12]	rw0c	1'h0	CC4OF	Capture/Compare 4 overcapture flag
[11]	rw0c	1'h0	CC3OF	Capture/Compare 3 overcapture flag
[10]	rw0c	1'h0	CC2OF	Capture/Compare 2 overcapture flag
[9]	rw0c	1'h0	CC1OF	Capture/Compare 1 overcapture flag This flag is set by hardware only when the corresponding channel is configured in input capture mode. It is cleared by software by writing it to '0'. 0: No overcapture has been detected. 1: The counter value has been captured in CCR1 register while CC1IF flag was already set
[8]	rw0c	1'h0	B2IF	Break 2 interrupt flag This flag is set by hardware as soon as the break 2 input goes active. It can be cleared by software if the break 2 input is not active. 0: No break event occurred. 1: An active level has been detected on the break 2 input. An interrupt is generated if BIE=1 in the DIER register.
[7]	rw0c	1'h0	BIF	Break interrupt flag This flag is set by hardware as soon as the break input goes active. It can be cleared by software if the break input is not active. 0: No break event occurred. 1: An active level has been detected on the break input. An interrupt is generated if BIE=1 in the DIER register.
[6]	rw0c	1'h0	TIF	Trigger interrupt flag This flag is set by hardware on trigger event. It is set when the counter starts or stops when gated mode is selected. It is cleared by software. 0: No trigger event occurred. 1: Trigger interrupt pending.
[5]	rw0c	1'h0	COMIF	COM interrupt flag This flag is set by hardware on COM event (when Capture/compare Control bits - CCxE, CCxNE, OCxM - have been updated). It is cleared by software. 0: No COM event occurred. 1: COM interrupt pending.
[4]	rw0c	1'h0	CC4IF	Capture/Compare 4 interrupt flag
[3]	rw0c	1'h0	CC3IF	Capture/Compare 3 interrupt flag
[2]	rw0c	1'h0	CC2IF	Capture/Compare 2 interrupt flag

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表 8-1: ATIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[1]	rw0c	1'h0	CC1IF	Capture/Compare 1 interrupt flag If channel CC1 is configured as output: This flag is set by hardware when the counter matches the compare value and in retriggerable one pulse mode. It is cleared by software. 0: No match. 1: The content of the counter CNT has matched the content of the CCR1 register. If channel CC1 is configured as input: This bit is set by hardware on a capture. It is cleared by software or by reading the CCR1 register. 0: No input capture occurred. 1: The counter value has been captured in CCR1 register.
[0]	rw0c	1'h0	UIF	Update interrupt flag This bit is set by hardware on an update event. It is cleared by software. 0: No update occurred 1: Update interrupt pending. This bit is set by hardware when the registers are updated: - At overflow or underflow regarding the repetition counter value (update if repetition counter = 0) and if UDIS=0 in the CR1 register. - When CNT is reinitialized by software using the UG bit in EGR register, if URS=0 and UDIS=0 in the CR1 register. - When CNT is reinitialized by a trigger event, if URS=0 and UDIS=0 in the CR1 register.
0x14		**0x00000000**	**EGR**	**Event generation register**
[31:9]		23'h0	RSVD	
[8]	w	1'h0	B2G	Break 2 generation This bit is set by software in order to generate an event, it is automatically cleared by hardware. 0: No action 1: A break 2 event is generated. MOE bit is cleared and B2IF flag is set. Related interrupt can occur if enabled.
[7]	w	1'h0	BG	Break generation This bit is set by software in order to generate an event, it is automatically cleared by hardware. 0: No action 1: A break event is generated. MOE bit is cleared and BIF flag is set. Related interrupt or DMA transfer can occur if enabled.
[6]	w	1'h0	TG	Trigger generation This bit is set by software in order to generate an event, it is automatically cleared by hardware. 0: No action 1: The TIF flag is set in SR register. Related interrupt or DMA transfer can occur if enabled.
[5]	w	1'h0	COMG	Capture/Compare control update generation This bit can be set by software, it is automatically cleared by hardware 0: No action 1: When CCPC bit is set, it allows to update CCxE, CCxNE and OCxM bits This bit acts only on channels having a complementary output.
[4]	w	1'h0	CC4G	Capture/compare 4 generation
[3]	w	1'h0	CC3G	Capture/compare 3 generation
[2]	w	1'h0	CC2G	Capture/compare 2 generation

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表 8-1: ATIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[1]	w	1'h0	CC1G	Capture/compare 1 generation This bit is set by software in order to generate an event, it is automatically cleared by hardware. 0: No action 1: A capture/compare event is generated on channel 1: If channel CC1 is configured as output: CC1IF flag is set, Corresponding interrupt or DMA request is sent if enabled. If channel CC1 is configured as input: The current value of the counter is captured in CCR1 register. The CC1IF flag is set, the corresponding interrupt or DMA request is sent if enabled. The CC1OF flag is set if the CC1IF flag was already high.
[0]	w	1'h0	UG	Update generation This bit can be set by software, it is automatically cleared by hardware. 0: No action 1: Re-initialize the counter and generates an update of the registers. The prescaler counter is cleared too (anyway the prescaler ratio is not affected). The counter is cleared if the center-aligned mode is selected or if DIR=0 (upcounting), else it takes the auto-reload value (ARR) if DIR=1 (downcounting).
0x18		**0x00000000**	**CCMR1**	**TIM capture/compare mode register 1**
[31:28]	rw	4'h0	OC2M	Output compare 2 mode
[27]	rw	1'h0	OC2PE	Output compare 2 preload enable
[26:25]		2'h0	RSVD	
[24]	rw	1'h0	OC2CE	Output compare 2 clear enable

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表 8-1: ATIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[23:20]	rw	4'h0	OC1M	Output compare 1 mode These bits define the behavior of the output reference signal OC1REF from which OC1 and OC1N are derived. OC1REF is active high whereas OC1 and OC1N active level depends on CC1P and CC1NP bits. 0000: Frozen - The comparison between the output compare register CCR1 and the counter CNT has no effect on the outputs. 0001: Set channel 1 to active level on match. OC1REF signal is forced high when the counter CNT matches the capture/compare register 1 (CCR1). 0010: Set channel 1 to inactive level on match. OC1REF signal is forced low when the counter CNT matches the capture/compare register 1 (CCR1). 0011: Toggle - OC1REF toggles when CNT=CCR1. 0100: Force inactive level - OC1REF is forced low. 0101: Force active level - OC1REF is forced high. 0110: PWM mode 1 - In upcounting, channel 1 is active as long as CNT<CCR1 else inactive. In downcounting, channel 1 is inactive (OC1REF=0) as long as CNT>CCR1 else active (OC1REF=1). 0111: PWM mode 2 - In upcounting, channel 1 is inactive as long as CNT<CCR1 else active. In downcounting, channel 1 is active as long as CNT>CCR1 else inactive. 1000: Retriggerable OPM mode 1 - In up-counting mode, the channel is active until a trigger event is detected (on TRGI signal). Then, a comparison is performed as in PWM mode 1 and the channels becomes inactive again at the next update. In down-counting mode, the channel is inactive until a trigger event is detected (on TRGI signal). Then, a comparison is performed as in PWM mode 1 and the channels becomes inactive again at the next update. 1001: Retriggerable OPM mode 2 - In up-counting mode, the channel is inactive until a trigger event is detected (on TRGI signal). Then, a comparison is performed as in PWM mode 2 and the channels becomes inactive again at the next update. In down-counting mode, the channel is active until a trigger event is detected (on TRGI signal). Then, a comparison is performed as in PWM mode 1 and the channels becomes active again at the next update. 1010: Reserved, 1011: Reserved, 1100: Combined PWM mode 1 - OC1REF has the same behavior as in PWM mode 1. OC1REFC is the logical OR between OC1REF and OC2REF. 1101: Combined PWM mode 2 - OC1REF has the same behavior as in PWM mode 2. OC1REFC is the logical AND between OC1REF and OC2REF. 1110: Asymmetric PWM mode 1 - OC1REF has the same behavior as in PWM mode 1. OC1REFC outputs OC1REF when the counter is counting up, OC2REF when it is counting down. 1111: Asymmetric PWM mode 2 - OC1REF has the same behavior as in PWM mode 2. OC1REFC outputs OC1REF when the counter is counting up, OC2REF when it is counting down. These bits can not be modified as long as LOCK level 3 has been programmed and CC1S=00 (the channel is configured in output). On channels having a complementary output, this bit field is preloaded. If the CCPC bit is set in the CR2 register then the OC1M active bits take the new value from the preloaded bits only when a COM event is generated.

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表 8-1: ATIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[19]	rw	1'h0	OC1PE	Output compare 1 preload enable 0: Preload register on CCR1 disabled. CCR1 can be written at anytime, the new value is taken in account immediately. 1: Preload register on CCR1 enabled. Read/Write operations access the preload register. CCR1 preload value is loaded in the active register at each update event. These bits can not be modified as long as LOCK level 3 has been programmed and CC1S=’00’(the channel is configured in output).
[18:17]		2'h0	RSVD	
[16]	rw	1'h0	OC1CE	Output compare 1 clear enable 0: OC1Ref is not affected by the ETRF input 1: OC1Ref is cleared as soon as a High level is detected on ETRF input
[15:12]	rw	4'h0	IC2F	Input capture 2 filter
[11:10]	rw	2'h0	IC2PSC	Input capture 2 prescaler
[9:8]	rw	2'h0	CC2S	Capture/Compare 2 selection This bit-field defines the direction of the channel (input/output) as well as the used input. 00: CC2 channel is configured as output 01: CC2 channel is configured as input, IC2 is mapped on TI2 10: CC2 channel is configured as input, IC2 is mapped on TI1 11: CC2 channel is configured as input, IC2 is mapped on TRC. This mode is working only if an internal trigger input is selected through the TS bit (SMCR register)
[7:4]	rw	4'h0	IC1F	Input capture 1 filter This bit-field defines the frequency used to sample TI1 input and the length of the digital filter applied to TI1. The digital filter is made of an event counter in which N consecutive events are needed to validate a transition on the output: 0000: No filter, sampling is done at fCLK 0001: fSAMPLING=fCLK, N=2 0010: fSAMPLING=fCLK, N=4 0011: fSAMPLING=fCLK, N=8 0100: fSAMPLING=fCLK/2, N=6 0101: fSAMPLING=fCLK/2, N=8 0110: fSAMPLING=fCLK/4, N=6 0111: fSAMPLING=fCLK/4, N=8 1000: fSAMPLING=fCLK/8, N=6 1001: fSAMPLING=fCLK/8, N=8 1010: fSAMPLING=fCLK/16, N=5 1011: fSAMPLING=fCLK/16, N=6 1100: fSAMPLING=fCLK/16, N=8 1101: fSAMPLING=fCLK/32, N=5 1110: fSAMPLING=fCLK/32, N=6 1111: fSAMPLING=fCLK/32, N=8

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表 8-1: ATIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[3:2]	rw	2'h0	IC1PSC	Input capture 1 prescaler This bit-field defines the ratio of the prescaler acting on CC1 input (IC1). The prescaler is reset as soon as CC1E=0 (CCER register). 00: no prescaler, capture is done each time an edge is detected on the capture input 01: capture is done once every 2 events 10: capture is done once every 4 events 11: capture is done once every 8 events
[1:0]	rw	2'h0	CC1S	Capture/Compare 1 selection This bit-field defines the direction of the channel (input/output) as well as the used input. 00: CC1 channel is configured as output 01: CC1 channel is configured as input, IC1 is mapped on TI1 10: CC1 channel is configured as input, IC1 is mapped on TI2 11: CC1 channel is configured as input, IC1 is mapped on TRC. This mode is working only if an internal trigger input is selected through TS bit (SMCR register)
0x1C		**0x00000000**	**CCMR2**	**TIM capture/compare mode register 2**
[31:28]	rw	4'h0	OC4M	Output compare 4 mode
[27]	rw	1'h0	OC4PE	Output compare 4 preload enable
[26:25]		2'h0	RSVD	
[24]	rw	1'h0	OC4CE	Output compare 4 clear enable
[23:20]	rw	4'h0	OC3M	Output compare 3 mode
[19]	rw	1'h0	OC3PE	Output compare 3 preload enable
[18:17]		2'h0	RSVD	
[16]	rw	1'h0	OC3CE	Output compare 3 clear enable
[15:12]	rw	4'h0	IC4F	Input capture 4 filter
[11:10]	rw	2'h0	IC4PSC	Input capture 4 prescaler
[9:8]	rw	2'h0	CC4S	Capture/Compare 4 selection This bit-field defines the direction of the channel (input/output) as well as the used input. 00: CC4 channel is configured as output 01: CC4 channel is configured as input, IC4 is mapped on TI4 10: CC4 channel is configured as input, IC4 is mapped on TI3 11: CC4 channel is configured as input, IC4 is mapped on TRC. This mode is working only if an internal trigger input is selected through TS bit (SMCR register)
[7:4]	rw	4'h0	IC3F	Input capture 3 filter
[3:2]	rw	2'h0	IC3PSC	Input capture 3 prescaler
[1:0]	rw	2'h0	CC3S	Capture/Compare 3 selection This bit-field defines the direction of the channel (input/output) as well as the used input. 00: CC3 channel is configured as output 01: CC3 channel is configured as input, IC3 is mapped on TI3 10: CC3 channel is configured as input, IC3 is mapped on TI4 11: CC3 channel is configured as input, IC3 is mapped on TRC. This mode is working only if an internal trigger input is selected through TS bit (SMCR register)
0x20		**0x00000000**	**CCER**	**Capture/Compare enable register**

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表 8-1: ATIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:22]		10'h0	RSVD	
[21]	rw	1'h0	CC6P	Capture/Compare 6 output Polarity.
[20]	rw	1'h0	CC6E	Capture/Compare 6 output enable.
[19]		1'h0	RSVD	
[18]		1'h0	RSVD	
[17]	rw	1'h0	CC5P	Capture/Compare 5 output Polarity.
[16]	rw	1'h0	CC5E	Capture/Compare 5 output enable.
[15]	rw	1'h0	CC4NP	Capture/Compare 4 complementary output polarity
[14]		1'h0	RSVD	
[13]	rw	1'h0	CC4P	Capture/Compare 4 output Polarity.
[12]	rw	1'h0	CC4E	Capture/Compare 4 output enable.
[11]	rw	1'h0	CC3NP	Capture/Compare 3 complementary output polarity
[10]	rw	1'h0	CC3NE	Capture/Compare 3 complementary output enable
[9]	rw	1'h0	CC3P	Capture/Compare 3 output Polarity.
[8]	rw	1'h0	CC3E	Capture/Compare 3 output enable.
[7]	rw	1'h0	CC2NP	Capture/Compare 2 complementary output polarity
[6]	rw	1'h0	CC2NE	Capture/Compare 2 complementary output enable
[5]	rw	1'h0	CC2P	Capture/Compare 2 output Polarity.
[4]	rw	1'h0	CC2E	Capture/Compare 2 output enable.
[3]	rw	1'h0	CC1NP	Capture/Compare 1 complementary output polarity CC1 channel configured as output: 0: OC1N active high. 1: OC1N active low. CC1 channel configured as input: This bit is used in conjunction with CC1P to define the polarity of TI1FP1 and TI2FP1. Refer to CC1P description. On channels having a complementary output, this bit is preloaded. If the CCPC bit is set in the CR2 register then the CC1NP active bit takes the new value from the preloaded bit only when a Commutation event is generated. This bit as well as other CCxNP is not writable as soon as LOCK level 2 or 3 has been programmed and CC1S=00 (channel configured as output).
[2]	rw	1'h0	CC1NE	Capture/Compare 1 complementary output enable 0: Off - OC1N is not active. OC1N level is then function of MOE, OSSI, OSSR, OIS1, OIS1N and CC1E bits. 1: On - OC1N signal is output on the corresponding output pin depending on MOE, OSSI, OSSR, OIS1, OIS1N and CC1E bits. On channels having a complementary output, this bit is preloaded. If the CCPC bit is set in the CR2 register then the CC1NE active bit takes the new value from the preloaded bit only when a Commutation event is generated.

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表 8-1: ATIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[1]	rw	1'h0	CC1P	Capture/Compare 1 output Polarity. CC1 channel configured as output: 0: OC1 active high 1: OC1 active low CC1 channel configured as input: CC1NP/CC1P bits select TI1FP1 and TI2FP1 polarity for trigger or capture operations. 00: noninverted/rising edge. Circuit is sensitive to TIxFP1 rising edge (capture, trigger in reset, external clock or trigger mode), TIxFP1 is not inverted (trigger in gated mode, encoder mode). 01: inverted/falling edge. Circuit is sensitive to TIxFP1 falling edge (capture, trigger in reset, external clock or trigger mode), TIxFP1 is inverted (trigger in gated mode, encoder mode). 10: reserved, do not use this configuration. 11: noninverted/both edges. Circuit is sensitive to both TIxFP1 rising and falling edges (capture, trigger in reset, external clock or trigger mode), TIxFP1 is not inverted (trigger in gated mode). This configuration must not be used for encoder mode. On channels having a complementary output, this bit is preloaded. If the CCPC bit is set in the CR2 register then the CC1P active bit takes the new value from the preloaded bit only when a Commutation event is generated. This bit as well as other CCxP is not writable as soon as LOCK level 2 or 3 has been programmed.
[0]	rw	1'h0	CC1E	Capture/Compare 1 output enable CC1 channel configured as output: 0: Off - OC1 is not active. OC1 level is then function of MOE, OSSI, OSSR, OIS1, OIS1N and CC1NE bits. 1: On - OC1 signal is output on the corresponding output pin depending on MOE, OSSI, OSSR, OIS1, OIS1N and CC1NE bits. CC1 channel configured as input: This bit determines if a capture of the counter value can actually be done into the input capture/compare register 1 (CCR1) or not. 0: Capture disabled. 1: Capture enabled. On channels having a complementary output, this bit is preloaded. If the CCPC bit is set in the CR2 register then the CC1E active bit takes the new value from the preloaded bit only when a Commutation event is generated.
0x24		**0x00000000**	**CNT**	**Counter**
[31:0]	rw	32'h0	CNT	bit 30 to 0 is the lower bits of counter value bit 31 depends on IUFREMAP in CR1. If UIFREMAP = 1 this bit is a read-only copy of the UIF bit of the ISR register If UIFREMAP = 0 this bit is counter value bit 31
0x28		**0x00000000**	**PSC**	**Prescaler**
[31:16]		16'h0	RSVD	
[15:0]	rw	16'h0	PSC	Prescaler value The counter clock frequency is fCLK/(PSC+1). PSC contains the value to be loaded in the active prescaler register at each update event (including when the counter is cleared through UG bit of EGR register or through trigger controller when configured in "reset mode").
0x2C		**0x00000000**	**ARR**	**Auto-reload register**

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表 8-1: ATIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:0]	rw	32'h0	ARR	Auto-reload value ARR is the value to be loaded in the actual auto-reload register.
0x30		**0x00000000**	**RCR**	**Repetition counter register**
[31:16]		16'h0	RSVD	
[15:0]	rw	16'h0	REP	Repetition counter value These bits allow the user to set-up the update rate of the compare registers when preload registers are enable, as well as the update interrupt generation rate, if this interrupt is enable. Each time the REP_CNT related downcounter reaches zero, an update event is generated and it restarts counting from REP value. As REP_CNT is reloaded with REP value only at the repetition update event, any write to the RCR register is not taken in account until the next repetition update event. It means in PWM mode (REP+1) corresponds to the number of PWM periods in edge-aligned mode or the number of half PWM period in center-aligned mode..
0x34		**0x00000000**	**CCR1**	**Capture/Compare register 1**
[31:0]	rw	32'h0	CCR1	Capture/Compare 1 value If channel CC1 is configured as output: CCR1 is the value to be loaded in the actual capture/compare 1 register (preload value).It is loaded permanently if the preload feature is not selected in the CCMR1 register (bit OC1PE). Else the preload value is copied in the active capture/compare 1 register when an update event occurs. The active capture/compare register contains the value to be compared to the counter CNT and signaled on OC1 output. If channel CC1is configured as input: CCR1 is the counter value transferred by the last input capture 1 event (IC1).
0x38		**0x00000000**	**CCR2**	**Capture/Compare register 2**
[31:0]	rw	32'h0	CCR2	Capture/Compare 2 value If channel CC2 is configured as output: CCR2 is the value to be loaded in the actual capture/compare 2 register (preload value).It is loaded permanently if the preload feature is not selected in the CCMR1 register (bit OC2PE). Else the preload value is copied in the active capture/compare 2 register when an update event occurs. The active capture/compare register contains the value to be compared to the counter CNT and signalled on OC2 output. If channel CC2 is configured as input: CCR2 is the counter value transferred by the last input capture 2 event (IC2).
0x3C		**0x00000000**	**CCR3**	**Capture/Compare register 3**
[31:0]	rw	32'h0	CCR3	Capture/Compare value If channel CC3 is configured as output: CCR3 is the value to be loaded in the actual capture/compare 3 register (preload value).It is loaded permanently if the preload feature is not selected in the CCMR2 register (bit OC3PE). Else the preload value is copied in the active capture/compare 3 register when an update event occurs. The active capture/compare register contains the value to be compared to the counter CNT and signalled on OC3 output. If channel CC3is configured as input: CCR3 is the counter value transferred by the last input capture 3 event (IC3).
0x40		**0x00000000**	**CCR4**	**Capture/Compare register 4**

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表 8-1: ATIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:0]	rw	32'h0	CCR4	Capture/Compare value 1. if CC4 channel is configured as output (CC4S bits): CCR4 is the value to be loaded in the actual capture/compare 4 register (preload value).It is loaded permanently if the preload feature is not selected in the CCMR2 register (bit OC4PE). Else the preload value is copied in the active capture/compare 4 register when an update event occurs. The active capture/compare register contains the value to be compared to the counter CNT and signalled on OC4 output. 2. if CC4 channel is configured as input (CC4S bits in CCMR4 register): CCR4 is the counter value transferred by the last input capture 4 event (IC4).
0x44		**0x00000000**	**BDTR**	**TIM break and dead-time register**
[31]	rw	1'h0	OSSR	Off-state selection for Run mode This bit is used when MOE=1 on channels having a complementary output which are configured as outputs. OSSR is not implemented if no complementary output is implemented in the timer. 0: When inactive, OC/OCN outputs are disabled (the timer releases the output control, forces a Hi-Z state). 1: When inactive, OC/OCN outputs are enabled with their inactive level as soon as CCxE=1 or CCxNE=1 (the output is still controlled by the timer). This bit can not be modified as soon as the LOCK level 2 has been programmed.
[30]	rw	1'h0	OSSI	Off-state selection for Idle mode This bit is used when MOE=0 due to a break event or by a software write, on channels configured as outputs. 0: When inactive, OC/OCN outputs are disabled (the timer releases the output control, imposes a Hi-Z state). 1: When inactive, OC/OCN outputs are first forced with their inactive level then forced to their idle level after the deadtime. The timer maintains its control over the output. This bit can not be modified as soon as the LOCK level 2 has been programmed.
[29]	rw	1'h0	BK2BID	Break2 bidirectional
[28]	rw	1'h0	BKBID	Break Bidirectional 0: Break input BRK in input mode 1: Break input BRK in bidirectional mode In the bidirectional mode (BKBID bit set to 1), the break input is configured both in input mode and in open drain output mode. Any active break event asserts a low logic level on the Break input to indicate an internal break event to external devices. This bit cannot be modified as long as LOCK level 1 has been programmed (LOCK bits in BDTR register).
[27]	rw	1'h0	BK2DSRM	Break2 Disarm
[26]	rw	1'h0	BKDSRM	Break Disarm 0: Break input BRK is armed 1: Break input BRK is disarmed This bit is cleared by hardware when no break source is active. The BKDSRM bit must be set by software to release the bidirectional output control (open-drain output in Hi-Z state) and then be polled it until it is reset by hardware, indicating that the fault condition has disappeared.

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表 8-1: ATIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[25]	rw	1'h0	BK2P	BK2P: Break 2 polarity 0: Break input BRK2 is active low 1: Break input BRK2 is active high This bit cannot be modified as long as LOCK level 1 has been programmed.
[24]	rw	1'h0	BK2E	Break 2 enable This bit enables the complete break 2 protection. 0: Break2 function disabled 1: Break2 function enabled This bit cannot be modified as long as LOCK level 1 has been programmed.
[23:20]	rw	4'h0	BK2F	Break 2 filter This bit-field defines the frequency used to sample BRK2 input and the length of the digital filter applied to BRK2. The digital filter is made of an event counter in which N consecutive events are needed to validate a transition on the output: 0000: No filter, BRK2 acts asynchronously 0001: fSAMPLING=fCLK, N=2 0010: fSAMPLING=fCLK, N=4 0011: fSAMPLING=fCLK, N=8 0100: fSAMPLING=fCLK/2, N=6 0101: fSAMPLING=fCLK/2, N=8 0110: fSAMPLING=fCLK/4, N=6 0111: fSAMPLING=fCLK/4, N=8 1000: fSAMPLING=fCLK/8, N=6 1001: fSAMPLING=fCLK/8, N=8 1010: fSAMPLING=fCLK/16, N=5 1011: fSAMPLING=fCLK/16, N=6 1100: fSAMPLING=fCLK/16, N=8 1101: fSAMPLING=fCLK/32, N=5 1110: fSAMPLING=fCLK/32, N=6 1111: fSAMPLING=fCLK/32, N=8 This bit cannot be modified as long as LOCK level 1 has been programmed.

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表 8-1: ATIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[19:16]	rw	4'h0	BKF	Break filter This bit-field defines the frequency used to sample BRK input and the length of the digital filter applied to BRK. The digital filter is made of an event counter in which N consecutive events are needed to validate a transition on the output: 0000: No filter, BRK acts asynchronously 0001: fSAMPLING=fCLK, N=2 0010: fSAMPLING=fCLK, N=4 0011: fSAMPLING=fCLK, N=8 0100: fSAMPLING=fCLK/2, N=6 0101: fSAMPLING=fCLK/2, N=8 0110: fSAMPLING=fCLK/4, N=6 0111: fSAMPLING=fCLK/4, N=8 1000: fSAMPLING=fCLK/8, N=6 1001: fSAMPLING=fCLK/8, N=8 1010: fSAMPLING=fCLK/16, N=5 1011: fSAMPLING=fCLK/16, N=6 1100: fSAMPLING=fCLK/16, N=8 1101: fSAMPLING=fCLK/32, N=5 1110: fSAMPLING=fCLK/32, N=6 1111: fSAMPLING=fCLK/32, N=8 This bit cannot be modified as long as LOCK level 1 has been programmed.
[15]	rw	1'h0	MOE	Main output enable This bit is cleared asynchronously by hardware as soon as one of the break inputs is active (BRK or BRK2). It is set by software or automatically depending on the AOE bit. It is acting only on the channels which are configured in output. 0: In response to a break 2 event. OC and OCN outputs are disabled In response to a break event or if MOE is written to 0: OC and OCN outputs are disabled or forced to idle state depending on the OSSI bit. 1: OC and OCN outputs are enabled if their respective enable bits are set (CCxE, CCxNE in CCER register).
[14]	rw	1'h0	AOE	Automatic output enable 0: MOE can be set only by software 1: MOE can be set by software or automatically at the next update event (if none of the break inputs BRK and BRK2 is active) This bit cannot be modified as long as LOCK level 1 has been programmed.
[13]	rw	1'h0	BKP	Break polarity 0: Break input BRK is active low 1: Break input BRK is active high This bit cannot be modified as long as LOCK level 1 has been programmed.
[12]	rw	1'h0	BKE	Break enable This bit enables the complete break protection. 0: Break function disabled 1: Break function enabled This bit cannot be modified as long as LOCK level 1 has been programmed.
[11]	rw	1'h0	DTPSC	Dead-time prescaler This bit-field enables dead-time prescaler. 0: dead-time is tCLK*(DTG+1) if DTG is not zero 1: dead-time is tCLK*(DTG+1)*16 if DTG is not zero This bit cannot be modified as long as LOCK level 1 has been programmed.

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表 8-1: ATIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[10]		1'h0	RSVD	
[9:0]	rw	10'h0	DTG	Dead-time generator setup This bit-field, together with DTPSC, defines the duration of the dead-time inserted between the complementary outputs. If DTG=0, dead-time is disabled. Example if tCLK=8.33ns (120MHz), dead-time possible values are: 16.67ns to 8533.33 ns by 8.33 ns steps if DTPSC=0, 266.67ns to 136.53 us by 133.33 ns steps if DTPSC=1 This bit cannot be modified as long as LOCK level 1 has been programmed.
0x54		**0x00000000**	**CCMR3**	**TIM capture/compare mode register 3**
[31:28]	rw	4'h0	OC6M	Output compare 6 mode
[27]	rw	1'h0	OC6PE	Output compare 6 preload enable
[26:25]		2'h0	RSVD	
[24]	rw	1'h0	OC6CE	Output compare 6 clear enable
[23:20]	rw	4'h0	OC5M	Output compare 5 mode
[19]	rw	1'h0	OC5PE	Output compare 5 preload enable
[18:17]		2'h0	RSVD	
[16]	rw	1'h0	OC5CE	Output compare 5 clear enable
[15]	rw	1'h0	GC5C3	Group Channel 5 and Channel 3 Distortion on Channel 3 output: 0: No effect of OC5REF on OC3REFC 1: OC3REFC is the logical AND of OC3REFC and OC5REF This bit can either have immediate effect or be preloaded and taken into account after an update event (if preload feature is selected in TIMxCCMR2).
[14]	rw	1'h0	GC5C2	Group Channel 5 and Channel 2 Distortion on Channel 2 output: 0: No effect of OC5REF on OC2REFC 1: OC2REFC is the logical AND of OC2REFC and OC5REF This bit can either have immediate effect or be preloaded and taken into account after an update event (if preload feature is selected in TIMxCCMR1).
[13]	rw	1'h0	GC5C1	Group Channel 5 and Channel 1 Distortion on Channel 1 output: 0: No effect of OC5REF on OC1REFC5 1: OC1REFC is the logical AND of OC1REFC and OC5REF This bit can either have immediate effect or be preloaded and taken into account after an update event (if preload feature is selected in TIMxCCMR1).
[12:0]		13'h0	RSVD	
0x58		**0x00000000**	**CCR5**	**Capture/Compare register 5**
[31:0]	rw	32'h0	CCR5	Capture/Compare 5 value CCR5 is the value to be loaded in the actual capture/compare 5 register (preload value). It is loaded permanently if the preload feature is not selected in the CCMR3 register (bit OC5PE). Else the preload value is copied in the active capture/compare 5 register when an update event occurs. The active capture/compare register contains the value to be compared to the counter CNT and signaled on OC5 output.
0x5C		**0x00000000**	**CCR6**	**Capture/Compare register 6**

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表 8-1: ATIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:0]	rw	32'h0	CCR6	Capture/Compare 6 value CCR6 is the value to be loaded in the actual capture/compare 6 register (preload value). It is loaded permanently if the preload feature is not selected in the CCMR3 register (bit OC6PE). Else the preload value is copied in the active capture/compare 6 register when an update event occurs. The active capture/compare register contains the value to be compared to the counter CNT and signaled on OC6 output.
0x60		**0x00000001**	**AF1**	**Alternate function option register**
[31:30]	rw	2'h0	LOCK	Lock configuration These bits offer a write protection against software errors. 00: LOCK OFF - No bit is write protected. 01: LOCK Level 1 = OISx and OISxN bits in CR2 register, BK2BID, BKBID, BK2DSRM, BKDSRM, BK2P, BK2E, BK2F[3:0], BKF[3:0], AOE, BKP, BKE, OSSI, OSSR, DTPSC and DTG bits in BDTR register, AF1 register and AF2 register can no longer be written. 10: LOCK Level 2 = LOCK Level 1 + CC Polarity bits (CCxP/CCxNP bits in CCER register, as long as the related channel is configured in output through the CCxS bits) as well as OSSR and OSSI bits can no longer be written. 11: LOCK Level 3 = LOCK Level 2 + CC Control bits (OCxM and OCxPE bits in CCMRx registers, as long as the related channel is configured in output through the CCxS bits) can no longer be written. The LOCK bits can be written to non-zero only once after reset.
[29:16]		14'h0	RSVD	
[15:14]	rw	2'h0	ETRSEL	ETR source selection 00: ETR input is connected to I/O 01: LPCOMP output1 (if LPCOMP integrated) 10: LPCOMP output2 (if LPCOMP integrated) 11: ETR input is connected to I/O This bit cannot be modified as long as LOCK level 1 has been programmed.
[13:12]		2'h0	RSVD	
[11]	rw	1'h0	BKCMP2P	BRK LPCOMP output2 polarity This bit selects the LPCOMP output2 sensitivity (if LPCOMP integrated). It must be programmed together with the BKP polarity bit. 0: LPCOMP output2 is active high 1: LPCOMP output2 is active low This bit cannot be modified as long as LOCK level 1 has been programmed.
[10]	rw	1'h0	BKCMP1P	BRK LPCOMP output1 polarity This bit selects the LPCOMP output1 sensitivity (if LPCOMP integrated). It must be programmed together with the BKP polarity bit. 0: LPCOMP output1 is active high 1: LPCOMP output1 is active low This bit cannot be modified as long as LOCK level 1 has been programmed.
[9]	rw	1'h0	BKINP	BRK BKIN input polarity This bit selects the BKIN input sensitivity. It must be programmed together with the BKP polarity bit. 0: BKIN input is active high 1: BKIN input is active low This bit cannot be modified as long as LOCK level 1 has been programmed.
[8:3]		6'h0	RSVD	

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表 8-1: ATIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[2]	rw	1'h0	BKCMP2E	BRK LPCOMP output2 enable This bit enables the LPCOMP output2 (if LPCOMP integrated) for the timer's BRK input. LPCOMP output2 is 'ORed' with the other BRK sources. 0: LPCOMP output2 disabled 1: LPCOMP output2 enabled This bit cannot be modified as long as LOCK level 1 has been programmed.
[1]	rw	1'h0	BKCMP1E	BRK LPCOMP output1 enable This bit enables the LPCOMP output1 (if LPCOMP integrated) for the timer's BRK input. LPCOMP output1 is 'ORed' with the other BRK sources. 0: LPCOMP output1 disabled 1: LPCOMP output1 enabled This bit cannot be modified as long as LOCK level 1 has been programmed.
[0]	rw	1'h0	BKINE	BRK BKIN input enable This bit enables the BKIN input. BKIN input is 'ORed' with the other BRK sources. 0: BKIN input disabled 1: BKIN input enabled This bit cannot be modified as long as LOCK level 1 has been programmed.
0x64		**0x00000001**	**AF2**	**Alternate function option register 2**
[31:12]		20'h0	RSVD	
[11]	rw	1'h0	BK2CMP2P	BRK2 LPCOMP output2 polarity This bit selects the LPCOMP output2 sensitivity (if LPCOMP integrated). It must be programmed together with the BK2P polarity bit. 0: LPCOMP output2 is active high 1: LPCOMP output2 is active low This bit cannot be modified as long as LOCK level 1 has been programmed.
[10]	rw	1'h0	BK2CMP1P	BRK2 LPCOMP output1 polarity This bit selects the LPCOMP output1 sensitivity (if LPCOMP integrated). It must be programmed together with the BK2P polarity bit. 0: LPCOMP output1 is active high 1: LPCOMP output1 is active low This bit cannot be modified as long as LOCK level 1 has been programmed.
[9]	rw	1'h0	BK2INP	BRK2 BKIN2 input polarity This bit selects the BKIN2 input sensitivity. It must be programmed together with the BK2P polarity bit. 0: BKIN2 input is active low 1: BKIN2 input is active high This bit cannot be modified as long as LOCK level 1 has been programmed.
[8:3]		6'h0	RSVD	
[2]	rw	1'h0	BK2CMP2E	BRK2 LPCOMP output2 enable This bit enables the LPCOMP output2 (if LPCOMP integrated) for the timer's BRK2 input. LPCOMP output2 is 'ORed' with the other BRK2 sources. 0: LPCOMP output2 disabled 1: LPCOMP output2 enabled This bit cannot be modified as long as LOCK level 1 has been programmed.

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表 8-1: ATIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[1]	rw	1'h0	BK2CMP1E	BRK2 LPCOMP output1 enable This bit enables the LPCOMP output1 (if LPCOMP integrated) for the timer's BRK2 input. LPCOMP output1 is 'ORed' with the other BRK2 sources. 0: LPCOMP output1 disabled 1: LPCOMP output1 enabled This bit cannot be modified as long as LOCK level 1 has been programmed.
[0]	rw	1'h0	BK2INE	BRK2 BKIN input enable This bit enables the BKIN2 input. BKIN2 input is 'ORed' with the other BRK2 sources. 0: BKIN2 input disabled 1: BKIN2 input enabled This bit cannot be modified as long as LOCK level 1 has been programmed.

8.2 BTIM

8.2.1 简介

BTIM (Basic Timer) 基于一个 32 比特递增计数器，可实现计时功能。计数时钟为系统 PCLK 或级联输入信号，并可进行 1~65536 倍的预分频。计时结果可以产生中断、DMA 请求或 PTC 触发。BTIM 包含主从模式接口，可以进行多级级联，实现多级计数或同步触发等功能。

8.2.2 主要特性

- 32 位递增自动重装载计数器
- 16 位可编程预分频器，计数器时钟频率的分频系数为 1~65536 之间的任意数值
- 支持单笔计数模式 (OPM)，计数完成后自动停止计数器
- 主从模式
  - 支持与其它定时器互连，可在作为主设备产生控制信号的同时，作为从设备被外部输入或其它主设备控制
  - 控制模式包括复位、触发、门控等
  - 支持多定时器同步启动、复位等
- 计数器溢出或初始化时产生中断/DMA

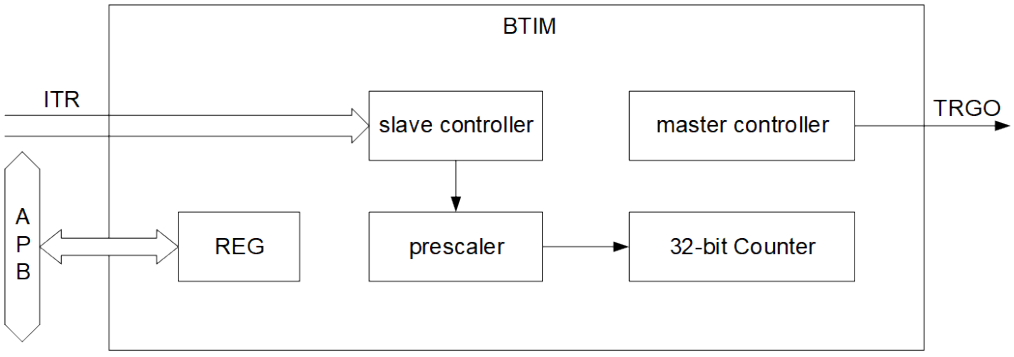

图 8-7: BTIM 结构图

8.2.3 BTIM 功能描述

8.2.3.1 计数器

BTIM 的各项功能均基于一个 32 比特的计数器。计数器基于事件计数，最基本的事件是一个 PCLK 时钟的翻转。根据不同配置，其它计数事件包括外部输入的翻转、其它定时器的输出翻转等。

计数事件经过预分频处理才会真正进入计数器。预分频的次数介于 1 到 65536 之间 (PSC+1)，即仅当发生了 (PSC+1) 次计数事件，计数器的值才真正改变一次。

计数器固定为递增计数模式，计数器从 0 计数到自动重载值 ARR，然后重新从 0 开始计数并产生计数器上溢事件。计数值可以通过 CNT 读出。

8.2.3.2 更新事件 (UEV)

更新事件用于标志一个计数单元的结束。最基本的更新事件产生于每次计数器上溢时。软件将 EGR_UG 置 1 时，也将产生更新事件。更新事件可以产生中断、DMA 请求以及 PTC 触发，是定时器最基本的一项通知功能。

通过软件将 CR1_UDIS 置 1 可禁止产生更新事件。这可避免向预装载寄存器写入新值时更新影子寄存器。在 UDIS 位写入 0 之前不会产生任何更新事件。

如果 CR1_URS（更新请求选择）已置 1，则将 EGR_UG 置 1 会生成更新事件，但不会将 UIF 标志置 1（因此，不会发送任何中断或 DMA 请求）。这样一来，如果在发生捕获事件时将计数器清零，将不会同时产生更新中断和捕获中断。

发生更新事件时，将重新装载 ARR 以及 PSC 寄存器，且将更新标志 SR_UIF 置 1（CR1_URS=0 时）。该功能可以保证修改这些计数器的基本参数不影响当前计数单元，在下一个计数周期才生效。

8.2.3.3 影子寄存器

对 ARR 以及 PSC 寄存器的修改不会直接体现在当前计数单元中，而是等到更新事件发生时才真正更新进去。在更新事件发生前，计数器真正使用的是影子寄存器中的值。这样即使在计数中动态改变这些寄存器的值，也不会影响到当前计数单元的完整性。

如果 CR1_APRE 为 0，ARR 寄存器将在配置后实时生效，不用等到更新事件发生。

8.2.3.4 主从模式

定时器可同时处于主模式与从模式。主模式是指该定时器可以输出 TRGO 信号至芯片上其它定时器的 ITR 输入，用于控制其它定时器的计数行为。从模式是指该定时器的计数行为受其它定时器输出至该定时器的 ITR 信号控制。

多个定时器可通过主从模式实现定时器同步，以实现多级分频、同时启动、门控计数等功能。

主模式可在不同事件发生时输出 TRGO 信号，如更新、使能等，由 CR2_MMS 选择。

从模式可以通过 SMCR_SMS 选择计数器复位、触发启动、计数事件等行为，同时可以选择门控模式。从模式依赖的触发信号 TRGI 和门控信号可在 ITR 中独立选择，并可选择门控信号极性。

定时器处于复位从模式 (SMCR_SMS=001) 时，当 TRGI 发生变化时，计数器及其预分频器重新初始化。如果 CR1_URS 为 0，则会生成更新事件 UEV，ARR 被更新。

定时器处于触发从模式 (SMCR_SMS=010) 时，软件不需配置 CR1_CEN 开启计数，而是在 TRGI 上升沿自动启动计数器。定时器处于复位触发从模式 (SMCR_SMS=011) 时，在 TRGI 的上升沿复位计数器并自动重新开启。

定时器处于外部时钟从模式 (SMCR_SMS=100) 时，计数事件修改为 TRGI 的上升沿，仅当 TRGI 发生翻转时才进行计数。

定时器开启门控从模式 (SMCR_GM=1) 时，当 TRGI 满足高电平或低电平要求 (SMCR_GTP) 时才进行计数，否则计数器不变。

8.2.3.5 单脉冲模式

将 CR1_OPM 写 1 可以使能单脉冲模式。该模式下计数器启动以后一旦发生更新事件，就会自动停止计数。该模式可以用于单次计数。

8.2.3.6 定时器同步

多个定时器可通过主从模式连接在一起，实现定时器同步，以完成多级分频、同时启动、门控计数等功能。

将主模式定时器的 TRGO 设置为更新事件，连接至另一个设置为外部时钟从模式的定时器，可以实现定时器级联计数。此时主模式定时器相当于从模式定时器的预分频，计数总位宽等于两个定时器各自的位宽相加。

将主模式定时器的 TRGO 设置为计数使能，并设置从模式为触发从模式，同时连接至另一个设置为触发从模式的定时器，可以实现多个定时器同步触发启动，从而对齐多个定时器的开启时机。该场景下主模式定时器还需将 SMCR_MSM 设为 1。

8.2.3.7 通知机制

BTIM 能够产生中断、DMA 请求、PTC 触发等多种通知机制。能够触发通知的事件为更新事件。DIER 寄存器可以控制各种事件是否产生中断和 DMA 请求。各事件状态可在 SR 寄存器中查询。

8.2.4 BTIM 寄存器

表 8-2: BTIM 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00		**0x00000000**	**CR1**	**TIM control register 1**
[31:8]		24'h0	RSVD	
[7]	rw	1'h0	ARPE	Auto-reload preload enable 0: ARR register is not buffered 1: ARR register is buffered
[6:4]		3'h0	RSVD	
[3]	rw	1'h0	OPM	One-pulse mode 0: Counter is not stopped at update event 1: Counter stops counting at the next update event (clearing the bit CEN)

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表 8-2: BTIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[2]	rw	1'h0	URS	Update request source This bit is set and cleared by software to select the UEV event sources. 0: Any of the following events generate an update interrupt or DMA request if enabled. These events can be: -Counter overflow -Setting the UG bit -Update generation through the slave mode controller 1: Only counter overflow generates an update interrupt or DMA request if enabled.
[1]	rw	1'h0	UDIS	Update disable This bit is set and cleared by software to enable/disable UEV event generation. 0: UEV enabled. The Update (UEV) event is generated by one of the following events: -Counter overflow -Setting the UG bit -Update generation through the slave mode controller Buffered registers are then loaded with their preload values. 1: UEV disabled. The Update event is not generated, shadow registers keep their value (ARR, PSC). However the counter and the prescaler are reinitialized if the UG bit is set or if a hardware reset is received from the slave mode controller.
[0]	rw	1'h0	CEN	Counter enable 0: Counter disabled 1: Counter enabled Note: Gated mode can work only if the CEN bit has been previously set by software. However trigger mode can set the CEN bit automatically by hardware. CEN is cleared automatically in one-pulse mode, when an update event occurs.
0x04		**0x00000000**	**CR2**	**TIM control register 2**
[31:6]		26'h0	RSVD	
[5:4]	rw	2'h0	MMS	Master mode selection These bits allow to select the information to be sent in master mode to slave timers for synchronization (TRGO). The combination is as follows: 00: Reset - the UG bit from the EGR register is used as trigger output (TRGO). If the reset is generated by the trigger input (slave mode controller configured in reset mode) then the signal on TRGO is delayed compared to the actual reset. 01: Enable - the Counter enable signal, CNT_EN, is used as trigger output (TRGO). It is useful to start several timers at the same time or to control a window in which a slave timer is enabled. The Counter Enable signal is generated by a logic OR between CEN control bit and the trigger input when configured in gated mode. When the Counter Enable signal is controlled by the trigger input, there is a delay on TRGO, except if the master/slave mode is selected (see the MSM bit description in SMCR register). 10: Update - The update event is selected as trigger output (TRGO). For instance a master timer can then be used as a prescaler for a slave timer. 11: Gating - The delayed gating trigger is selected as trigger output (TRGO).
[3:0]		4'h0	RSVD	
0x08		**0x00000000**	**SMCR**	**TIM slave mode control register**
[31:24]		8'h0	RSVD	

续表下页...

表 8-2: BTIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[23]	rw	1'h0	GM	Gated Mode. The counter clock is enabled when the selected trigger input (TRGI) is active (according to gating trigger polarity). The counter stops (but is not reset) as soon as the trigger becomes inactive. Both start and stop of the counter are controlled. Gated mode and slave mode can be enabled simutanuously with different trigger selection.
[22]	rw	1'h0	GTP	Gating trigger polarity invert 0: active at high level 1: active at low level
[21:20]	rw	2'h0	GTS	Gating trigger selection in gated mode This bit-field selects the trigger input to be used to enable the counter gating. 00: Internal Trigger 0 (ITR0) 01: Internal Trigger 1 (ITR1) 10: Internal Trigger 2 (ITR2) 11: Internal Trigger 3 (ITR3)
[19]		1'h0	RSVD	
[18:16]	rw	3'h0	SMS	Slave mode selection When external signals are selected the active edge of the trigger signal (TRGI) is linked to the polarity selected on the external input. 000: Slave mode disabled. 001: Reset Mode - Rising edge of the selected trigger input (TRGI) reinitializes the counter and generates an update of the registers. 010: Trigger Mode - The counter starts at a rising edge of the trigger TRGI (but it is not reset). Only the start of the counter is controlled. 011: Combined reset + trigger mode - Rising edge of the selected trigger input (TRGI) reinitializes the counter, generates an update of the registers and starts the counter. 100: External Clock Mode - Rising edges of the selected trigger (TRGI) clock the counter.
[15:8]		8'h0	RSVD	
[7]	rw	1'h0	MSM	Master/Slave mode. This bit should be asserted on master timer if synchronization if needed. 0: No action 1: The effect of an event on the trigger input (TRGI) is delayed to allow a perfect synchronization between the current timer and its slaves (through TRGO). It is useful if we want to synchronize several timers on a single external event.
[6]		1'h0	RSVD	
[5:4]	rw	2'h0	TS	Trigger selection This bit-field selects the trigger input to be used to synchronize the counter. 00: Internal Trigger 0 (ITR0) 01: Internal Trigger 1 (ITR1) 10: Internal Trigger 2 (ITR2) 11: Internal Trigger 3 (ITR3)
[3:0]		4'h0	RSVD	
0x0C		**0x00000000**	**DIER**	**TIM DMA/Interrupt enable register**
[31:9]		23'h0	RSVD	
[8]	rw	1'h0	UDE	Update DMA request enable 0: Update DMA request disabled. 1: Update DMA request enabled
[7:1]		7'h0	RSVD	

续表下页...

表 8-2: BTIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[0]	rw	1'h0	UIE	Update interrupt enable 0: Update interrupt disabled. 1: Update interrupt enabled
0x10		**0x00000000**	**SR**	**TIM status register**
[31:1]		31'h0	RSVD	
[0]	rw0c	1'h0	UIF	Update interrupt flag This bit is set by hardware on an update event. It is cleared by software. 0: No update occurred 1: Update interrupt pending. This bit is set by hardware when the registers are updated: At overflow and if UDIS=0 in the CR1 register. When CNT is reinitialized by software using the UG bit in EGR register, if URS=0 and UDIS=0 in the CR1 register. When CNT is reinitialized by a trigger event (refer to the synchro control register description), if URS=0 and UDIS=0 in the CR1 register.
0x14		**0x00000000**	**EGR**	**Event generation register**
[31:1]		31'h0	RSVD	
[0]	w1s	1'h0	UG	Update generation This bit can be set by software, it is automatically cleared by hardware. 0: No action 1: Re-initialize the counter and generates an update of the registers. Note that the prescaler counter is cleared too (anyway the prescaler ratio is not affected). The counter is cleared if the center-aligned mode is selected or if DIR=0 (upcounting), else it takes the auto-reload value (ARR) if DIR=1 (downcounting).
0x24		**0x00000000**	**CNT**	**Counter**
[31:0]	rw	32'h0	CNT	counter value
0x28		**0x00000000**	**PSC**	**Prescaler**
[31:16]		16'h0	RSVD	
[15:0]	rw	16'h0	PSC	Prescaler value The counter clock frequency is equal to fCLK / (PSC[15:0] + 1). PSC contains the value to be loaded in the active prescaler register at each update event (including when the counter is cleared through UG bit of EGR register or through trigger controller when configured in "reset mode").
0x2C		**0x00000000**	**ARR**	**Auto-reload register**
[31:0]	rw	32'h0	ARR	Auto-reload value ARR is the value to be loaded in the actual auto-reload register. The counter is blocked while the auto-reload value is null.

8.3 GPTIM

8.3.1 简介

GPTIM (General Purpose Timer) 基于一个 16 比特计数器，可实现计时、测量输入信号的脉冲长度 (输入捕获) 或者产生输出波形 (输出比较和 PWM) 等功能。计数器本身可以进行递增、递减或者递增/递减计数，计数时钟可选系统 PCLK，IO 输入信号或级联输入信号，并可进行 1~65536 倍的预分频。GPTIM 共有 4 个通道，可以分别独立配置为输入捕获或输出模式。计数、输入捕获和输出比较的结果可以产生中断、DMA 请求或 PTC 触发。GPTIM 包含主从模式接口，可以进行多级级联，实现多级计数或同步触发等功能。

8.3.2 主要特性

- 16 位递增、递减、递增/递减自动重装载计数器，最大计数 65535
- 16 位可编程 (可以实时修改) 预分频器，计数器时钟频率的分频系数为 1~65536 之间的任意数值
- 8 位可配置重复计数
- 支持单笔计数模式 (OPM)，当重复计数完成后自动停止计数器
- 4 个独立通道，可分别配置为输入或输出模式
- 输入模式
  - 上升沿/下降沿捕获
  - PWM 脉宽和周期捕获 (需占用两个通道)
  - 可选 4 个输入端口之一或 1 个外部触发端口，支持防抖动滤波和预降频
- 输出模式
  - 强制输出高/低电平
  - 计数到比较值时输出高/低/翻转电平
  - PWM 输出，可配脉宽和周期
  - 多通道 PWM 组合输出，可产生有相互关系的多路 PWM
  - 单脉冲/重触发单脉冲模式输出
- 主从模式
  - 支持多定时器互连，可在作为主设备产生控制信号的同时，作为从设备被外部输入或其它主设备控制
  - 控制模式包括复位、触发、门控等
  - 支持多定时器同步启动、复位等
- 编码模式输入，控制计数器递增/递减计数
- 如下事件发生时产生中断/DMA 请求/PTC 触发：
  - 更新：计数器递增溢出/递减溢出，计数器初始化 (通过软件或者内部/外部触发)
  - 触发事件 (计数器启动、停止、初始化或者由内部/外部触发计数)
  - 输入捕获
  - 输出比较

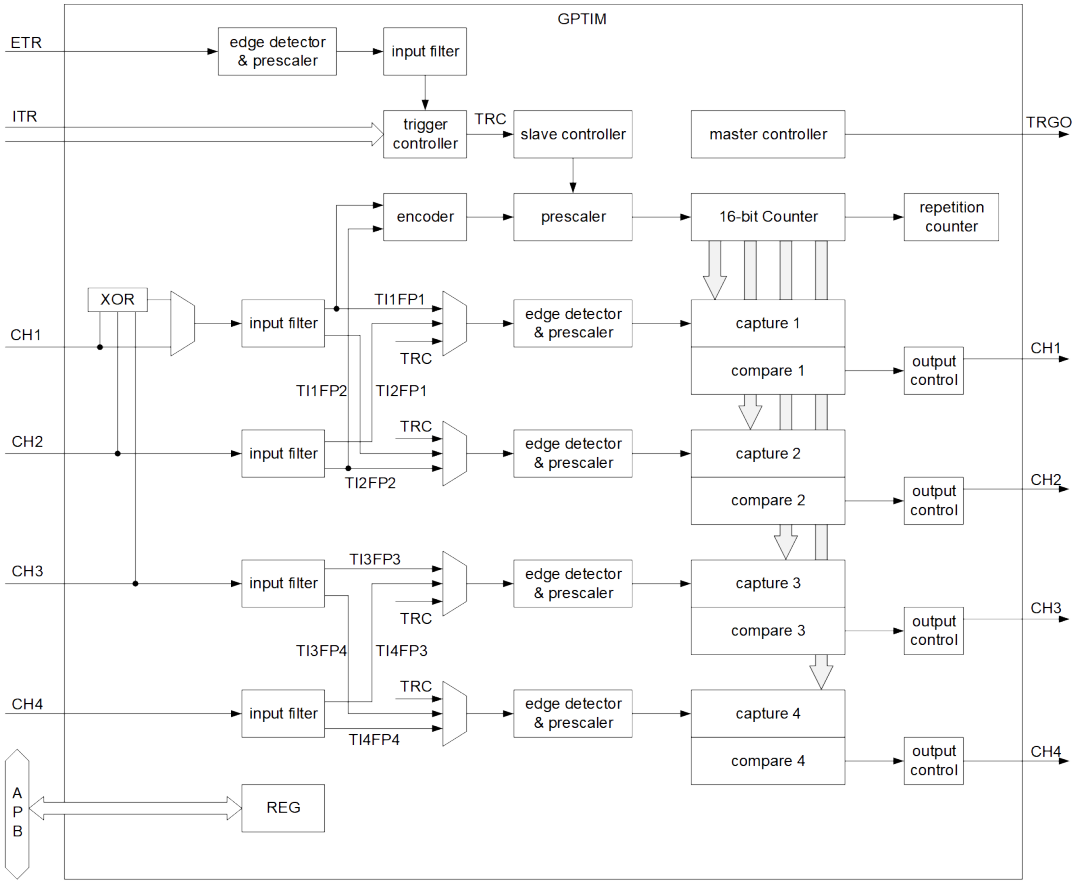


图 8-8: GPTIM 结构图

8.3.3 GPTIM 功能描述

8.3.3.1 计数器

GPTIM 的各项功能均基于一个 16 比特的计数器。计数器基于事件计数，最基本的事件是一个 PCLK 时钟的翻转。根据不同配置，其它计数事件包括外部输入的翻转、其它定时器的输出翻转、正交编码器接口解码输出等。

计数事件经过预分频处理才会真正进入计数器。预分频的次数介于 1 到 65536 之间 (PSC+1)，即仅当发生了 (PSC+1) 次计数事件，计数器的值才真正改变一次。

计数器共有三种计数模式：递增，递减以及中心对齐。在递增计数模式下 (CR1_CMS=0 且 CR1_DIR=0)，计数器从 0 计数到自动重载值 ARR，然后重新从 0 开始计数并产生计数器上溢事件。在递减计数模式下 (CR1_CMS=0 且 CR1_DIR=1)，计数器从 ARR 开始递减计数到 0，然后重新从 ARR 开始计数并产生计数器下溢事件。在中心对齐模式下 (CR1_CMS 不为 0)，计数器从 0 开始计数到 ARR-1，产生计数器上溢事件，然后从 ARR 开始向下计数到 1 并产生计数器下溢事件，之后从 0 开始重新计数。

计数值可以通过 CNT 读出。计数的方向可以从 CR1_DIR 读出。

8.3.3.2 更新事件 (UEV)

更新事件用于标志一个计数单元的结束。最基本的更新事件产生于每次计数器上溢或下溢时 (未开启重复计数时)。软件将 EGR_UG 置 1 时，也将产生更新事件。更新事件可以产生中断、DMA 请求以及 PTC 触发，是定时

器最基本的一项通知功能。

通过软件将 CR1_UDIS 置 1 可禁止产生更新事件。这可避免向预装载寄存器写入新值时更新影子寄存器。在 UDIS 位写入 0 之前不会产生任何更新事件。

如果 CR1_URS（更新请求选择）已置 1，则将 EGR_UG 置 1 会生成更新事件，但不会将 UIF 标志置 1（因此，不会发送任何中断或 DMA 请求）。这样一来，如果在发生捕获事件时将计数器清零，将不会同时产生更新中断和捕获中断。

发生更新事件时，将重新装载 RCR，ARR 以及 PSC 寄存器，且将更新标志 SR_UIF 置 1（CR1_URS=0 时）。该功能可以保证修改这些计数器的基本参数不影响当前计数单元，在下一个计数周期才生效。

8.3.3.3 重复计数

如果配置了重复计数器 (RCR>0)，每次计数器上溢或下溢时重复计数器会递减，并仅当重复计数器为 0 时才产生更新事件。更新事件发生时，重复计数器会重新装载 RCR 的值。

重复计数器的当前值不能读出。

8.3.3.4 影子寄存器

对 RCR，ARR 以及 PSC 寄存器的修改不会直接体现在当前计数单元中，而是等到更新事件发生时才真正更新进去。在更新事件发生前，计数器真正使用的是影子寄存器中的值。这样即使在计数中动态改变这些寄存器的值，也不会影响到当前计数单元的完整性，对于 PWM 输出等应用场景很有意义。

如果 CR1_APRE 为 0，ARR 寄存器将在配置后实时生效，不用等到更新事件发生。

输出比较寄存器 CCRx 也有影子寄存器。当 CCMRx_OCxPE 为 0 时，配置的 CCRx 会立即生效，否则要等到更新事件发生时才生效。

8.3.3.5 主从模式

定时器可同时处于主模式与从模式。主模式是指该定时器可以输出 TRGO 信号至芯片上其它定时器的 ITR 输入，用于控制其它定时器的计数行为。从模式是指该定时器的计数行为受外部输入 ETR，其它定时器输出至该定时器的 ITR 信号，或定时器的通道输入 CHx 的控制。

多个定时器可通过主从模式实现定时器同步，以实现多级分频、同时启动、门控计数等功能。

主模式可在不同事件发生时输出 TRGO 信号，如更新、使能、输入捕获、输出比较等，由 CR2_MMS 选择。

从模式可以选择计数器复位、触发启动、计数使能、计数事件等行为，由 SMCR_SMS 选择。从模式依赖的触发信号 TRGI 可灵活配置，可以在 ETR，ITR 以及通道输入中选择，并可选择信号极性，进行预分频、滤波等操作。

- 定时器处于复位从模式 (SMCR_SMS=0100) 时，当 TRGI 发生变化时，计数器及其预分频器重新初始化。如果 CR1_URS 为 0，则会生成更新事件 UEV，然后所有预装载寄存器 ARR 和 CCRx 都将更新。
- 定时器处于门控从模式 (SMCR_SMS=0101) 时，当 TRGI 满足高电平或低电平要求时才进行计数，否则计数器不变。
- 定时器处于触发从模式 (SMCR_SMS=0110) 时，软件不需配置 CR1_CEN 开启计数，而是当 TRGI 满足特定触发要求时自动启动计数器。

- 定时器处于外部时钟从模式 (SMCR_SMS=0111) 时，计数事件修改为 TRGI 的上升沿，仅当 TRGI 发生翻转时才进行计数。
- 定时器处于复位触发从模式 (SMCR_SMS=1000) 时，TRGI 满足特定触发要求时复位计数器并自动重新开启。

8.3.3.6 通道输入输出

定时器的部分通道可以独立配置为输入捕获模式 (CCMRx_CCxS!=0) 或输出模式 (CCMRx_CCxS=0)。

在输入捕获模式下，通道在对应的触发信号有效时，将计数器的值记录进 CCRx，并产生中断等通知信号。该触发信号可在 ETR，ITR 以及通道输入 CHx 中选择，并可选择信号极性，进行预分频、滤波等操作。通道产生的通知信号包括中断、DMA 请求、PTC 触发等。输入捕获模式可实现记录外部信号改变的时刻、测量 PWM 周期和占空比等功能。

在输出模式下，通道将比较计数器的值与 CCRx 的大小，在通道输出 CHx/CHxN 上产生固定电平，或产生基于本通道以及其它通道比较结果的 PWM 输出信号，并产生中断等通知信号。产生 PWM 信号的脉冲个数、频率、占空比、相位等参数均可调节。多个通道还可以联合产生特定关系的 PWM 组合。通道产生的通知信号包括中断、DMA 请求、PTC 触发等。

8.3.3.7 输入捕获模式

在输入捕获模式下，当通道相应的触发信号检测到跳变沿后，将使用 CCRx 来锁存计数器的值。发生捕获事件时，会将相应的 SR_CCxIF 标志置 1，并可发送中断、DMA 请求（如果已使能）或 PTC 触发信号。如果发生捕获事件时 SR_CCxIF 标志已处于高位，则会将重复捕获标志 SR_CCxOF 置 1。可通过软件将 SR_CCxIF 清零，方法是向 SR_CCxIF 写入 0，或读取存储在 CCRx 中的已捕获数据。向 SR_CCxOF 写入 0 后会将其清零。

以下示例说明了如何在 CH1 输入出现上升沿时将计数器的值捕获到 CCR1 中，具体操作步骤如下：

1. 选择有效输入：通道 1 要连接到 CH1 输入，因此向 CCMR1_CC1S 写入 01。
2. 根据连接到定时器的信号，对所需的输入滤波带宽进行配置。
   假设 CH1 信号边沿变化时，最多在 5 个 PCLK 周期内发生抖动，需将滤波带宽设置为大于 5 个 PCLK 周期。将 CCMR1_IC1F 设置为 0011(0x3)，则在检测到连续 8 个采样点（以 PCLK 频率采样）均为新电平后，可以确认 CH1 的跳变沿。
3. 将 CCER_CC1P 和 CCER_CC1NP 写 0，选择 CH1 上的有效转换边沿为上升沿。
4. 对输入预分频器进行编程。
   在本例中我们希望每次有效转换时都执行捕获操作，因此禁用预分频器（CCMR1_IC1PS 写 00）。
5. CCER_CC1E 置 1，使能通道 1，允许将计数器的值捕获到 CCR1 中。
6. 如果需要，可将 DIER_CC1IE 置 1 来使能相关中断请求，或将 DIER_CC1DE 置 1 来使能 DMA 请求。

配置完成后，通道将在 CH1 输入出现上升沿时执行下列操作：

1. CCR1 寄存器记录计数器的值。
2. SR_CCxIF 标志置 1（中断标志）。如果至少发生了两次连续捕获，但 SR_CCxIF 未被清零，这样 SR_CCxOF 捕获溢出标志会被置 1。
3. 根据 CCER_CC1IE 生成中断。
4. 根据 DIER_CC1DE 生成 DMA 请求。

要处理重复捕获，建议在读出 SR_CCxOF 之前读取数据。这样可避免丢失在读取 SR_CCxOF 之后与读取数据之前可能出现的重复捕获信息。

通过软件将 EGR_CCxG 置 1 可立即产生一次捕获，并生成通道捕获中断和 DMA 请求。

8.3.3.8 PWM 输入捕获

PWM 输入捕获是输入捕获的一种扩展应用，可用于测量 PWM 输入信号的周期和占空比。为实现该功能，需要将两个通道都配置为输入捕获模式，触发信号分别映射成输入 PWM 的正边沿和负边沿，并开启计数器复位的从模式。

以下示例说明了如何用通道 1 和通道 2 测量从 CH1 输入的 PWM 的周期和占空比，具体操作步骤如下：

1. 选择通道 1 的有效输入为 CH1 输入，因此向 CCMR1_CC1S 写入 01。
2. 选择通道 1 输入信号的有效极性（用于在 CCR1 中捕获和计数器清零），将 CCER_CC1P 和 CCER_CC1NP 写 0，选择 CH1 上的有效转换边沿为上升沿。
3. 选择通道 2 的有效输入也为 CH1 输入，向 CCMR1_CC2S 写入 10(0x2)。
4. 选择通道 2 输入信号的有效极性（用于 CCR2 捕获），将 CCER_CC2P 写 1，CCER_CC1NP 写 0，选择 CH1 上的有效转换边沿为下降沿。
5. 设置从模式控制信号为 CH1，向 SMCR_TS 写入 101(0x5)，选择 TI1FP1。
6. 将从模式控制器配置为复位模式，向 SMCR_SMS 写入 0100(0x4)。
7. 使能通道 1 和通道 2，将 CCER_CC1E 和 CCER_CC2E 置 1。

配置完成后，在每个 CH1 的上升沿，计数器的值被记录在 CCR1 中，同时计数器被复位并重新开始计数；在每个 CH1 的下降沿，计数器的值被记录在 CCR2 中。将 CCR1 的值乘以 PCLK 的周期，可以算出 PWM 的周期。将 CCR2 的值乘以 PCLK 的周期，可以算出 PWM 高电平持续的时间，从而得到 PWM 的占空比。

8.3.3.9 输出比较模式

在输出比较模式下，当计数值与 CCRx 满足一定关系时，可以在对应 CHx 及 CHxN 上产生特定输出，通常用于控制输出波形，或指示已经过某一时间段。

具体而言，通道将在 CCRx 与计数器之间相匹配时执行下列操作：

1. 将为相应的 CHx 和 CHxN 输出分配一个可编程值，该值由比较模式寄存器 CCMRx_OCxM 和输出极性寄存器 CCER_CCxP/CCxNP 定义。匹配时，输出引脚既可保持其电平（CCMRx_OCxM=0000），也可设置为有效电平 (CCMRx_OCxM=0001)、无效电平 (CCMRx_OCxM=0010) 或进行翻转 (CCMRx_OCxM=0011)。
2. 将中断状态寄存器标志 SR_CCxIF 置 1。
3. 根据 CCER_CC1IE 生成中断。
4. 根据 DIER_CC1DE 和 CR2_CCDS 生成 DMA 请求。

配置 CCMRx_OCxPE，可将 CCRx 寄存器配置为带或不带影子寄存器。当 CCMRx_OCxPE 为 0 时，软件修改 CCRx 实时生效，可通过在每次中断中修改下一次匹配的 CCRx 来实现自定义波形的输出。

8.3.3.10 基础 PWM 输出

利用输出比较模式，定时器可以产生周期、占空比、相位可控的多路 PWM 输出。PWM 输出的周期由 ARR 决定，占空比由 CCRx 决定。PWM 输出有多种模式，由每个通道的 CCMRx_OCxM 各自独立选择。最基本的单路

PWM 输出只需要占用一个通道，采用基础的 PWM 模式即可实现。复杂的 PWM 信号，或 PWM 组合则需要占用多个通道，并需仔细分配每个通道的 PWM 模式以及 CCRx。

在基础的 PWM 模式下，计数器值 CNT 与 CCRx 进行比较，并根据计数器的当前计数方向产生包含有效电平或无效电平的比较输出信号 OCxREF。有效电平的极性可通过 CCER_CCxP 配置，并根据 CCER_CCxE 和 BDTR_MOE 等寄存器使能 CHx 输出。

如在递增计数模式下，配置 CCMR1_OC1M 和 CCMR1_OC2M 为 0110(0x6)，则 PWM 输出如图8-9。其中计数值 CNT 小于 CCR1/2 时，输出高电平，否则输出低电平。

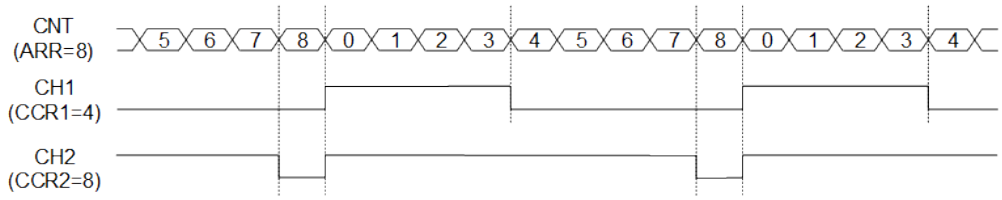


图 8-9: 递增计数模式下的 PWM 输出

如在中心对齐计数模式下，配置 CCMR1_OC1M 和 CCMR1_OC2M 为 0110(0x6)，则 PWM 输出如图8-10。其中递增阶段计数值 CNT 小于 CCR1/2 时，输出高电平，否则输出低电平；递减阶段计数值 CNT 大于 CCR1/2 时，输出低电平，否则输出高电平。

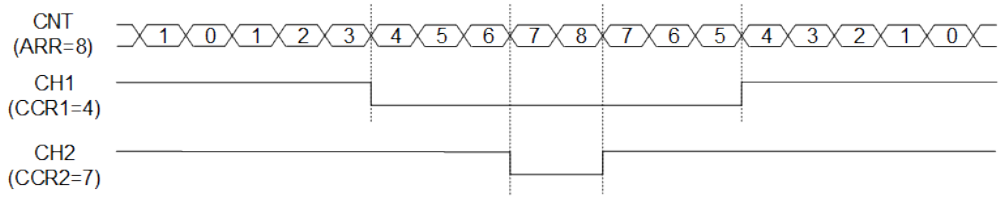


图 8-10: 中心对齐计数模式下的 PWM 输出

8.3.3.11 不对称 PWM 输出

在不对称 PWM 模式下，生成的两个 PWM 信号之间存在可编程相移。该模式仅限于计数器处于中心对齐模式时。生成的两个 PWM 信号频率相同，由 ARR 的值确定，而占空比和相移则各由一对 CCRx 寄存器确定。每一路输出 PWM 占用两个 CCRx 寄存器，分别控制递增计数和递减计数期间的行为，这样 PWM 的上升沿和下降沿时间点可以分别配置。CCR1 和 CCR2 共同控制 CH1/2 的输出，CCR3 和 CCR4 共同控制 CH3/4 的输出。

CH1/2 以及 CH3/4 可以独立选择不同的不对称 PWM 模式，配置 CCMRx_OCxM 为 1110(0xe) 或 1111(0xf)。

如配置 CCMR1_OC1M 和 CCMR2_OC3M 为 1110(0xe)，则 PWM 输出如图8-11。其中递增阶段 (0->ARR-1) 计数值 CNT 小于 CCR1/3 时，输出高电平，否则输出低电平；递减阶段 (ARR->1) 计数值 CNT 大于 CCR2/4 时，输出低电平，否则输出高电平。

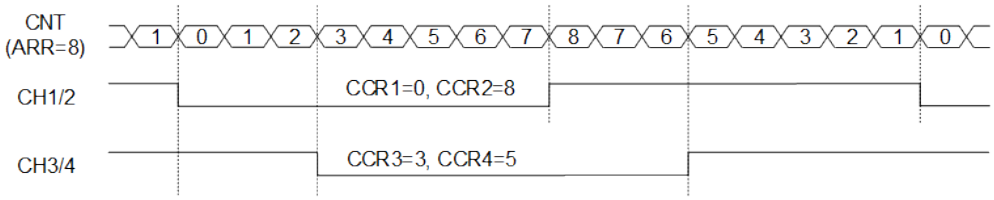


图 8-11: 不对称 PWM 输出

8.3.3.12 组合 PWM 输出

在组合 PWM 模式下，生成的两个 PWM 信号之间存在可编程延时和相移。计数器处于递增、递减或中心对齐模式均可，生成的两个 PWM 信号频率相同，由 ARR 的值确定，而占空比和相移则各由一对 CCRx 寄存器确定。每一路输出 PWM 占用两个 CCRx 寄存器，是由两路基础 PWM 输出波形的逻辑与运算或者逻辑或运算组合而成。CCR1 和 CCR2 共同控制 CH1/2 的输出，CCR3 和 CCR4 共同控制 CH3/4 的输出。

CH1/2 以及 CH3/4 可以独立选择不同的组合 PWM 模式，配置 CCMRx_OCxM 为 1100(0xc) 或 1101(0xd)。当 CH1 或 CH3 配置为组合 PWM 模式 1100(0xc) 时，CH2 或 CH4 必须配置为 0111(0x7) 或 1101(0xd) 或 1111(0xf)。当 CH1 或 CH3 配置为组合 PWM 模式 1101(0xd) 时，CH2 或 CH4 必须配置为 0110(0x6) 或 1100(0xc) 或 1110(0xe)。

如配置 CCMR1_OC1M 为 1101(0xd)，CCMR1_OC2M 为 0110(0x6)，CCMR2_OC3M 为 1100(0xc)，CCMR2_OC4M 为 0111(0x7)，则 PWM 输出如图8-12。其中计数值 CNT 小于 CCR1/4 时，OC1REF/OC4REF 为低电平，否则为高电平；计数值 CNT 小于 CCR2/3 时，OC2REF/OC3REF 为高电平，否则为低电平。CH1 输出是 OC1REF 和 OC2REF 的逻辑与运算。CH3 输出是 OC3REF 和 OC4REF 的逻辑或运算。

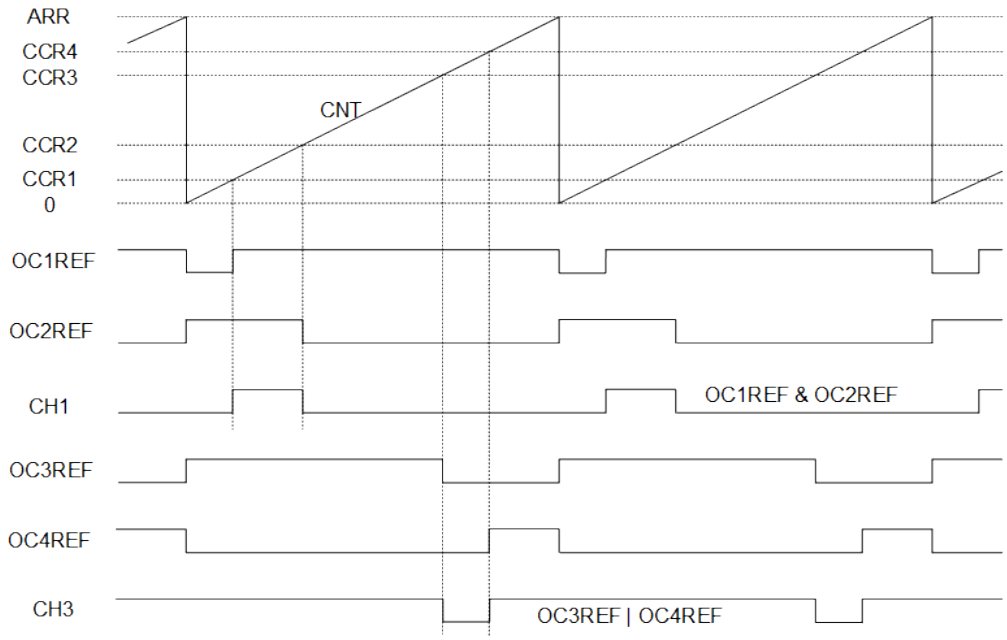


图 8-12: 组合 PWM 输出

8.3.3.13 单脉冲模式

将 CR1_OPM 写 1 可以使能单脉冲模式。该模式下计数器启动以后一旦发生更新事件，就会自动停止计数。该模式可以用于单次计数，或在一个激励信号的触发下启动，并在一段可编程的延时后产生一个脉宽可编程的脉冲。

例如，希望实现这样的功能，在 CH2 输入引脚检测到上升沿时，经过一定时间延迟，在 CH1 上产生单个一定宽度的正脉冲。配置方法如下：

1. CCMR1_CC2S=01，以将 TI2FP2 映射到通道 2。
2. CCER_CCxP 和 CCER_CCxNP 写 0，TI2FP2 反应 CH2 上升沿的变化。
3. SMCR_TS=110(0x6)，将 TI2FP2 配置为从模式控制器的触发 TRGI。
4. SMCR_SMS=110(0x6)，将从模式控制器配置为触发模式，触发后开启计数。
5. 根据需要的时间延迟与脉冲宽度配置 ARR 与 CCR1，定义时间延迟与脉冲宽度。
6. CCMR1_OC1M=0111(0x7)，配置为正脉冲 PWM。
7. CR1_OPM=1，一次触发只产生一个脉冲。
8. EGR_UG=1，手动刷新 ARR 与 CCR1 寄存器。

从模式为触发模式时不需要手动使能 CR1_CEN，一旦检测到触发信号生效，计数器就会自动使能。

8.3.3.14 编码器接口模式

编码器接口模式下，通道 1 和通道 2 可以用于连接外部正交编码器，将外部编码器的信号转化为定时器的计数值变化，从而获知外部编码器的工作状态。

如果计数器仅在 CH1 边沿处计数，SMCR_SMS 配置为 0001；如果计数器仅在 CH2 边沿处计数，SMCR_SMS 配置为 0010(0x2)；如果计数器在 CH1 和 CH2 边沿处均计数，SMCR_SMS 配置为 0011(0x3)。CCER_CC1P/CC2P 用于选择 CH1 和 CH2 极性。如果需要，还可对输入滤波器进行编程。两个输入的信号转换序列会产生计数脉冲和方向信号，根据该信号转换序列，计数器相应递增或递减计数，同时硬件对 CR1_DIR 进行相应修改。

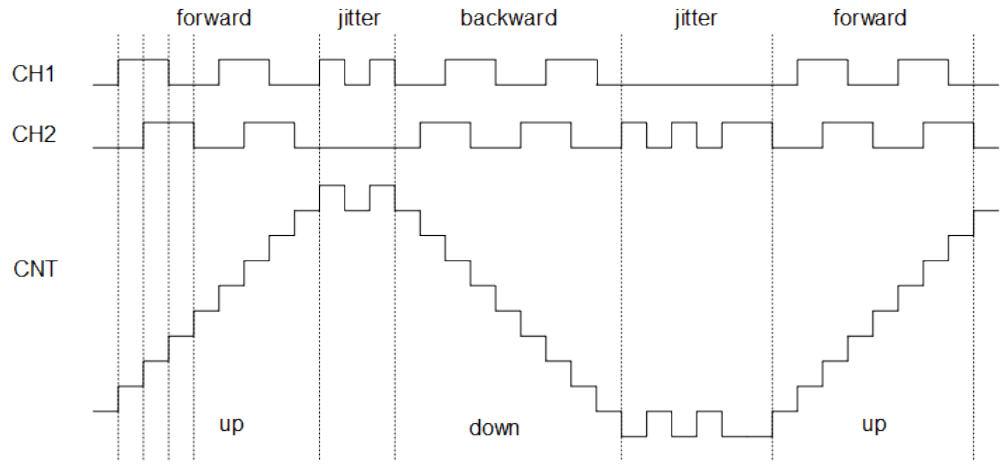
编码器接口模式下，计数器的计数事件是正交编码器接口的解码输出。计数器仅在 0 到 ARR 之间进行连续计数（根据计数的具体方向，从 0 递增计数到 ARR，或从 ARR 递减计数到 0）。因此，在启动前必须先配置 ARR。同样，捕获、比较、重复计数器和触发输出功能继续正常工作。在此模式下，计数器会根据正交编码器的速度和方向自动进行修改，因此，其内容始终表示编码器的位置。计数方向对应于所连传感器的旋转方向。下表汇总了可能的组合（假设 CH1 和 CH2 不同时切换）。

SMCR_SMS	条件	CH1 上升沿	CH1 上升沿	CH2 上升沿	CH2 上升沿
0001 或 0011	CH2=0	递增	递减	/	/
	CH2=1	递减	递增	/	/
0010 或 0011	CH1=0	/	/	递减	递增
	CH1=1	/	/	递增	递减

下图示意了计数器如何根据正交编码器的信号变化进行计数的，配置如下：

CCMR1_CC1S=01（CH1 映射到通道 1 上），CCMR2_CC2S=01（CH2 映射到通道 2 上），

CCER_CC1P/CC1NP/CC2P/CC2NP=0，SMCR_SMS=0011(0x3)，CR1_CEN=1。



8.3.3.15 定时器同步

多个定时器可通过主从模式连接在一起，实现定时器同步，以完成多级分频、同时启动、门控计数等功能。

将主模式定时器的 TRGO 设置为更新事件 (CR2_MMS=010)，连接至另一个设置为外部时钟从模式 (SMCR_SMS = 0111) 的定时器，可以实现定时器级联计数。此时主模式定时器相当于从模式定时器的预分频，计数总位宽等于两个定时器各自的位宽相加。

将主模式定时器的 TRGO 设置为计数使能 (CR2_MMS=001)，并设置从模式为触发从模式 (SMCR_SMS=0110)，同时连接至另一个设置为触发从模式 (SMCR_SMS=0110) 的定时器，可以实现多个定时器同步触发启动，从而对齐多个定时器的开启时机。该场景下主模式定时器还需将 SMCR_MSM 设为 1。

将主模式定时器的 TRGO 设置为比较输出 (CR2_MMS=100)，连接至另一个设置为门控从模式 (SMCR_SMS=0101) 的定时器，可以实现门控 PWM 输出。主模式定时器可以对从模式定时器输出的 PWM 载波进行调制输出。

8.3.3.16 通知机制

ATIM 能够产生中断、DMA 请求、PTC 触发等多种通知机制。能够触发通知的事件主要包括更新事件、触发事件、比较器匹配、输入捕获等。DIER 寄存器可以控制各种事件是否产生中断和 DMA 请求。各事件状态可在 SR 寄存器中查询。

8.3.4 GPTIM 寄存器

表 8-3: GPTIM 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00		**0x00000000**	**CR1**	**TIM control register 1**
[31:12]		20'h0	RSVD	
[11]	rw	1'h0	UIFREMAP	UIF status bit remapping 0: No remapping. UIF status bit is not copied to CNT register bit 31 1: Remapping enabled. UIF status bit is copied to CNT register bit 31
[10:8]		3'h0	RSVD	
[7]	rw	1'h0	ARPE	Auto-reload preload enable 0: ARR register is not buffered 1: ARR register is buffered

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表 8-3: GPTIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[6:5]	rw	2'h0	CMS	Center-aligned mode selection 00: Edge-aligned mode. The counter counts up or down depending on the direction bit (DIR). 01: Center-aligned mode 1. The counter counts up and down alternatively. Output compare interrupt flags of channels configured in output (CCxS=00 in CCMRx register) are set only when the counter is counting down. 10: Center-aligned mode 2. The counter counts up and down alternatively. Output compare interrupt flags of channels configured in output (CCxS=00 in CCMRx register) are set only when the counter is counting up. 11: Center-aligned mode 3. The counter counts up and down alternatively. Output compare interrupt flags of channels configured in output (CCxS=00 in CCMRx register) are set both when the counter is counting up or down.
[4]	rw	1'h0	DIR	Direction 0: Counter used as upcounter 1: Counter used as downcounter
[3]	rw	1'h0	OPM	One-pulse mode 0: Counter is not stopped at update event 1: Counter stops counting at the next update event (clearing the bit CEN)
[2]	rw	1'h0	URS	Update request source This bit is set and cleared by software to select the UEV event sources. 0: Any of the following events generate an update interrupt or DMA request if enabled. These events can be: –Counter overflow/underflow –Setting the UG bit –Update generation through the slave mode controller 1: Only counter overflow/underflow generates an update interrupt or DMA request if enabled.
[1]	rw	1'h0	UDIS	Update disable This bit is set and cleared by software to enable/disable UEV event generation. 0: UEV enabled. The Update (UEV) event is generated by one of the following events: –Counter overflow/underflow –Setting the UG bit –Update generation through the slave mode controller Buffered registers are then loaded with their preload values. 1: UEV disabled. The Update event is not generated, shadow registers keep their value (ARR, PSC, CCRx). However the counter and the prescaler are reinitialized if the UG bit is set or if a hardware reset is received from the slave mode controller.
[0]	rw	1'h0	CEN	Counter enable 0: Counter disabled 1: Counter enabled Note: External clock, gated mode and encoder mode can work only if the CEN bit has been previously set by software. However trigger mode can set the CEN bit automatically by hardware. CEN is cleared automatically in one-pulse mode, when an update event occurs.
0x04		**0x00000000**	**CR2**	**TIM control register 2**
[31:8]		24'h0	RSVD	

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表 8-3: GPTIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[7]	rw	1'h0	TI1S	TI1 selection 0: The CH1 pin is connected to TI1 input 1: The CH1, CH2 and CH3 pins are connected to the TI1 input (XOR combination)
[6:4]	rw	3'h0	MMS	Master mode selection These bits allow to select the information to be sent in master mode to slave timers for synchronization (TRGO). The combination is as follows: 000: Reset - the UG bit from the EGR register is used as trigger output (TRGO). If the reset is generated by the trigger input (slave mode controller configured in reset mode) then the signal on TRGO is delayed compared to the actual reset. 001: Enable - the Counter enable signal is used as trigger output (TRGO). It is useful to start several timers at the same time or to control a window in which a slave timer is enabled. The Counter Enable signal is generated by a logic OR between CEN control bit and the trigger input when configured in gated mode. When the Counter Enable signal is controlled by the trigger input, there is a delay on TRGO, except if the master/slave mode is selected. 010: Update - The update event is selected as trigger output (TRGO). For instance a master timer can then be used as a prescaler for a slave timer. 011: Compare Pulse - The trigger output send a positive pulse when the CC1IF flag is to be set (even if it was already high), as soon as a capture or a compare match occurred. (TRGO) 100: Compare - OC1REF signal is used as trigger output (TRGO) 101: Compare - OC2REF signal is used as trigger output (TRGO) 110: Compare - OC3REF signal is used as trigger output (TRGO) 111: Compare - OC4REF signal is used as trigger output (TRGO)
[3]	rw	1'h0	CCDS	Capture/compare DMA selection 0: CCx DMA request sent when CCx event occurs 1: CCx DMA requests sent when update event occurs
[2:0]		3'h0	RSVD	
0x08		**0x00000000**	**SMCR**	**TIM slave mode control register**
[31:20]		12'h0	RSVD	

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表 8-3: GPTIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[19:16]	rw	4'h0	SMS	Slave mode selection When external signals are selected the active edge of the trigger signal (TRGI) is linked to the polarity selected on the external input. 0000: Slave mode disabled. 0001: Encoder mode 1 - Counter counts up/down on TI1FP1 edge depending on TI2FP2 level. 0010: Encoder mode 2 - Counter counts up/down on TI2FP2 edge depending on TI1FP1 level. 0011: Encoder mode 3 - Counter counts up/down on both TI1FP1 and TI2FP2 edges depending on the level of the other input. 0100: Reset Mode - Rising edge of the selected trigger input (TRGI) reinitializes the counter and generates an update of the registers. 0101: Gated Mode - The counter clock is enabled when the trigger input (TRGI) is high. The counter stops (but is not reset) as soon as the trigger becomes low. Both start and stop of the counter are controlled. 0110: Trigger Mode - The counter starts at a rising edge of the trigger TRGI (but it is not reset). Only the start of the counter is controlled. 0111: External Clock Mode 1 - Rising edges of the selected trigger (TRGI) clock the counter. 1000: Combined reset + trigger mode - Rising edge of the selected trigger input (TRGI) reinitializes the counter, generates an update of the registers and starts the counter.
[15]	rw	1'h0	ETP	External trigger polarity 0: ETR is non-inverted, active at high level or rising edge 1: ETR is inverted, active at low level or falling edge
[14]	rw	1'h0	ECE	External clock enable This bit enables External clock mode 2. 0: External clock mode 2 disabled 1: External clock mode 2 enabled. The counter is clocked by any active edge on the ETRF signal.
[13:12]	rw	2'h0	ETPS	External trigger prescaler External trigger signal ETRP frequency must be at most 1/4 of CK_INT frequency. A prescaler can be enabled to reduce ETRP frequency. It is useful when inputting fast external clocks. 00: Prescaler OFF 01: ETRP frequency divided by 2 10: ETRP frequency divided by 4 11: ETRP frequency divided by 8

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表 8-3: GPTIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[11:8]	rw	4'h0	ETF	External trigger filter This bit-field then defines the frequency used to sample ETRP signal and the length of the digital filter applied to ETRP. The digital filter is made of an event counter in which N consecutive events are needed to validate a transition on the output: 0000: No filter 0001: fSAMPLING=fCLK, N=2 0010: fSAMPLING=fCLK, N=4 0011: fSAMPLING=fCLK, N=8 0100: fSAMPLING=fCLK/2, N=6 0101: fSAMPLING=fCLK/2, N=8 0110: fSAMPLING=fCLK/4, N=6 0111: fSAMPLING=fCLK/4, N=8 1000: fSAMPLING=fCLK/8, N=6 1001: fSAMPLING=fCLK/8, N=8 1010: fSAMPLING=fCLK/16, N=5 1011: fSAMPLING=fCLK/16, N=6 1100: fSAMPLING=fCLK/16, N=8 1101: fSAMPLING=fCLK/32, N=5 1110: fSAMPLING=fCLK/32, N=6 1111: fSAMPLING=fCLK/32, N=8
[7]	rw	1'h0	MSM	Master/Slave mode 0: No action 1: The effect of an event on the trigger input (TRGI) is delayed to allow a perfect synchronization between the current timer and its slaves (through TRGO). It is useful if we want to synchronize several timers on a single external event.
[6:4]	rw	3'h0	TS	Trigger selection This bit-field selects the trigger input to be used to synchronize the counter. 000: Internal Trigger 0 (ITR0) 001: Internal Trigger 1 (ITR1) 010: Internal Trigger 2 (ITR2) 011: Internal Trigger 3 (ITR3) 100: TI1 Edge Detector (TI1F_ED) 101: Filtered Timer Input 1 (TI1FP1) 110: Filtered Timer Input 2 (TI2FP2) 111: External Trigger input (ETRF)
[3:0]		4'h0	RSVD	
0x0C		**0x00000000**	**DIER**	**TIM DMA/Interrupt enable register**
[31:15]		17'h0	RSVD	
[14]	rw	1'h0	TDE	Trigger DMA request enable 0: Trigger DMA request disabled. 1: Trigger DMA request enabled.
[13]		1'h0	RSVD	
[12]	rw	1'h0	CC4DE	Capture/Compare 4 DMA request enable 0: CC4 DMA request disabled. 1: CC4 DMA request enabled
[11]	rw	1'h0	CC3DE	Capture/Compare 3 DMA request enable 0: CC3 DMA request disabled. 1: CC3 DMA request enabled.

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表 8-3: GPTIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[10]	rw	1'h0	CC2DE	Capture/Compare 2 DMA request enable 0: CC2 DMA request disabled. 1: CC2 DMA request enabled.
[9]	rw	1'h0	CC1DE	Capture/Compare 1 DMA request enable 0: CC1 DMA request disabled. 1: CC1 DMA request enabled.
[8]	rw	1'h0	UDE	Update DMA request enable 0: Update DMA request disabled. 1: Update DMA request enabled
[7]		1'h0	RSVD	
[6]	rw	1'h0	TIE	Trigger interrupt enable 0: Trigger interrupt disabled. 1: Trigger interrupt enabled
[5]		1'h0	RSVD	
[4]	rw	1'h0	CC4IE	Capture/Compare 4 interrupt enable 0: CC4 interrupt disabled. 1: CC4 interrupt enabled
[3]	rw	1'h0	CC3IE	Capture/Compare 3 interrupt enable 0: CC3 interrupt disabled. 1: CC3 interrupt enabled
[2]	rw	1'h0	CC2IE	Capture/Compare 2 interrupt enable 0: CC2 interrupt disabled. 1: CC2 interrupt enabled.
[1]	rw	1'h0	CC1IE	Capture/Compare 1 interrupt enable 0: CC1 interrupt disabled. 1: CC1 interrupt enabled
[0]	rw	1'h0	UIE	Update interrupt enable 0: Update interrupt disabled. 1: Update interrupt enabled
0x10		**0x00000000**	**SR**	**TIM status register**
[31:13]		19'h0	RSVD	
[12]	rw0c	1'h0	CC4OF	Capture/Compare 4 overcapture flag
[11]	rw0c	1'h0	CC3OF	Capture/Compare 3 overcapture flag
[10]	rw0c	1'h0	CC2OF	Capture/Compare 2 overcapture flag
[9]	rw0c	1'h0	CC1OF	Capture/Compare 1 overcapture flag This flag is set by hardware only when the corresponding channel is configured in input capture mode. It is cleared by software by writing it to '0'. 0: No overcapture has been detected. 1: The counter value has been captured in CCR1 register while CC1IF flag was already set
[8:7]		2'h0	RSVD	
[6]	rw0c	1'h0	TIF	Trigger interrupt flag This flag is set by hardware on trigger event (active edge detected on TRGI input when the slave mode controller is enabled in all modes but gated mode). It is set when the counter starts or stops when gated mode is selected. It is cleared by software. 0: No trigger event occurred. 1: Trigger interrupt pending.
[5]		1'h0	RSVD	

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表 8-3: GPTIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[4]	rw0c	1'h0	CC4IF	Capture/Compare 4 interrupt flag
[3]	rw0c	1'h0	CC3IF	Capture/Compare 3 interrupt flag
[2]	rw0c	1'h0	CC2IF	Capture/Compare 2 interrupt flag
[1]	rw0c	1'h0	CC1IF	Capture/Compare 1 interrupt flag If channel CC1 is configured as output: This flag is set by hardware when the counter matches the compare value. It is cleared by software. 0: No match. 1: The content of the counter CNT has matched the content of the CCR1 register. If channel CC1 is configured as input: This bit is set by hardware on a capture. It is cleared by software or by reading the CCR1 register. 0: No input capture occurred. 1: The counter value has been captured in CCR1 register (An edge has been detected on IC1 which matches the selected polarity).
[0]	rw0c	1'h0	UIF	Update interrupt flag This bit is set by hardware on an update event. It is cleared by software. 0: No update occurred 1: Update interrupt pending. This bit is set by hardware when the registers are updated: At overflow or underflow and if UDIS=0 in the CR1 register. When CNT is reinitialized by software using the UG bit in EGR register, if URS=0 and UDIS=0 in the CR1 register. When CNT is reinitialized by a trigger event, if URS=0 and UDIS=0 in the CR1 register.
0x14		**0x00000000**	**EGR**	**Event generation register**
[31:7]		25'h0	RSVD	
[6]	w	1'h0	TG	Trigger generation This bit is set by software in order to generate an event, it is automatically cleared by hardware. 0: No action 1: The TIF flag is set in SR register. Related interrupt or DMA transfer can occur if enabled.
[5]		1'h0	RSVD	
[4]	w	1'h0	CC4G	Capture/compare 4 generation
[3]	w	1'h0	CC3G	Capture/compare 3 generation
[2]	w	1'h0	CC2G	Capture/compare 2 generation
[1]	w	1'h0	CC1G	Capture/compare 1 generation This bit is set by software in order to generate an event, it is automatically cleared by hardware. 0: No action 1: A capture/compare event is generated on channel 1: If channel CC1 is configured as output: CC1IF flag is set, Corresponding interrupt or DMA request is sent if enabled. If channel CC1 is configured as input: The current value of the counter is captured in CCR1 register. The CC1IF flag is set, the corresponding interrupt or DMA request is sent if enabled. The CC1OF flag is set if the CC1IF flag was already high.

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表 8-3: GPTIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[0]	w	1'h0	UG	Update generation This bit can be set by software, it is automatically cleared by hardware. 0: No action 1: Re-initialize the counter and generates an update of the registers. Note that the prescaler counter is cleared too (anyway the prescaler ratio is not affected). The counter is cleared if the center-aligned mode is selected or if DIR=0 (upcounting), else it takes the auto-reload value (ARR) if DIR=1 (downcounting).
0x18		**0x00000000**	**CCMR1**	**TIM capture/compare mode register 1**
[31:28]	rw	4'h0	OC2M	Output compare 2 mode
[27]	rw	1'h0	OC2PE	Output compare 2 preload enable
[26:25]		2'h0	RSVD	
[24]	rw	1'h0	OC2CE	Output compare 2 clear enable

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表 8-3: GPTIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[23:20]	rw	4'h0	OC1M	Output compare 1 mode These bits define the behavior of the output reference signal OC1REF from which OC1 and OC1N are derived. OC1REF is active high whereas OC1 and OC1N active level depends on CC1P and CC1NP bits. 0000: Frozen - The comparison between the output compare register CCR1 and the counter CNT has no effect on the outputs.(this mode is used to generate a timing base). 0001: Set channel 1 to active level on match. OC1REF signal is forced high when the counter CNT matches the capture/compare register 1 (CCR1). 0010: Set channel 1 to inactive level on match. OC1REF signal is forced low when the counter CNT matches the capture/compare register 1 (CCR1). 0011: Toggle - OC1REF toggles when CNT=CCR1. 0100: Force inactive level - OC1REF is forced low. 0101: Force active level - OC1REF is forced high. 0110: PWM mode 1 - In upcounting, channel 1 is active as long as CNT<CCR1 else inactive. In downcounting, channel 1 is inactive (OC1REF= '0) as long as CNT>CCR1 else active (OC1REF=1). 0111: PWM mode 2 - In upcounting, channel 1 is inactive as long as CNT<CCR1 else active. In downcounting, channel 1 is active as long as CNT>CCR1 else inactive. 1000: Retriggerable OPM mode 1 - In up-counting mode, the channel is active until a trigger event is detected (on TRGI signal). Then, a comparison is performed as in PWM mode 1 and the channels becomes inactive again at the next update. In down-counting mode, the channel is inactive until a trigger event is detected (on TRGI signal). Then, a comparison is performed as in PWM mode 1 and the channels becomes inactive again at the next update. 1001: Retriggerable OPM mode 2 - In up-counting mode, the channel is inactive until a trigger event is detected (on TRGI signal). Then, a comparison is performed as in PWM mode 2 and the channels becomes inactive again at the next update. In down-counting mode, the channel is active until a trigger event is detected (on TRGI signal). Then, a comparison is performed as in PWM mode 1 and the channels becomes active again at the next update. 1010: Reserved, 1011: Reserved, 1100: Combined PWM mode 1 - OC1REF has the same behavior as in PWM mode 1. OC1REFC is the logical OR between OC1REF and OC2REF. 1101: Combined PWM mode 2 - OC1REF has the same behavior as in PWM mode 2. OC1REFC is the logical AND between OC1REF and OC2REF. 1110: Asymmetric PWM mode 1 - OC1REF has the same behavior as in PWM mode 1. OC1REFC outputs OC1REF when the counter is counting up, OC2REF when it is counting down. 1111: Asymmetric PWM mode 2 - OC1REF has the same behavior as in PWM mode 2. OC1REFC outputs OC1REF when the counter is counting up, OC2REF when it is counting down.
[19]	rw	1'h0	OC1PE	Output compare 1 preload enable 0: Preload register on CCR1 disabled. CCR1 can be written at anytime, the new value is taken in account immediately. 1: Preload register on CCR1 enabled. Read/Write operations access the preload register. CCR1 preload value is loaded in the active register at each update event.

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表 8-3: GPTIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[18:17]		2'h0	RSVD	
[16]	rw	1'h0	OC1CE	Output compare 1 clear enable 0: OC1Ref is not affected by the ETRF input 1: OC1Ref is cleared as soon as a High level is detected on ETRF input
[15:12]	rw	4'h0	IC2F	Input capture 2 filter
[11:10]	rw	2'h0	IC2PSC	Input capture 2 prescaler
[9:8]	rw	2'h0	CC2S	Capture/Compare 2 selection This bit-field defines the direction of the channel (input/output) as well as the used input. 00: CC2 channel is configured as output 01: CC2 channel is configured as input, IC2 is mapped on TI2 10: CC2 channel is configured as input, IC2 is mapped on TI1 11: CC2 channel is configured as input, IC2 is mapped on TRC. This mode is working only if an internal trigger input is selected through the TS bit (SMCR register)
[7:4]	rw	4'h0	IC1F	Input capture 1 filter This bit-field defines the frequency used to sample TI1 input and the length of the digital filter applied to TI1. The digital filter is made of an event counter in which N consecutive events are needed to validate a transition on the output: 0000: No filter, sampling is done at fCLK 0001: fSAMPLING=fCLK, N=2 0010: fSAMPLING=fCLK, N=4 0011: fSAMPLING=fCLK, N=8 0100: fSAMPLING=fCLK/2, N=6 0101: fSAMPLING=fCLK/2, N=8 0110: fSAMPLING=fCLK/4, N=6 0111: fSAMPLING=fCLK/4, N=8 1000: fSAMPLING=fCLK/8, N=6 1001: fSAMPLING=fCLK/8, N=8 1010: fSAMPLING=fCLK/16, N=5 1011: fSAMPLING=fCLK/16, N=6 1100: fSAMPLING=fCLK/16, N=8 1101: fSAMPLING=fCLK/32, N=5 1110: fSAMPLING=fCLK/32, N=6 1111: fSAMPLING=fCLK/32, N=8
[3:2]	rw	2'h0	IC1PSC	Input capture 1 prescaler This bit-field defines the ratio of the prescaler acting on CC1 input (IC1). The prescaler is reset as soon as CC1E=0. 00: no prescaler, capture is done each time an edge is detected on the capture input 01: capture is done once every 2 events 10: capture is done once every 4 events 11: capture is done once every 8 events

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表 8-3: GPTIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[1:0]	rw	2'h0	CC1S	Capture/Compare 1 selection This bit-field defines the direction of the channel (input/output) as well as the used input. 00: CC1 channel is configured as output 01: CC1 channel is configured as input, IC1 is mapped on TI1 10: CC1 channel is configured as input, IC1 is mapped on TI2 11: CC1 channel is configured as input, IC1 is mapped on TRC. This mode is working only if an internal trigger input is selected through TS bit (SMCR register)
0x1C		**0x00000000**	**CCMR2**	**TIM capture/compare mode register 2**
[31:28]	rw	4'h0	OC4M	Output compare 4 mode
[27]	rw	1'h0	OC4PE	Output compare 4 preload enable
[26:25]		2'h0	RSVD	
[24]	rw	1'h0	OC4CE	Output compare 4 clear enable
[23:20]	rw	4'h0	OC3M	Output compare 3 mode
[19]	rw	1'h0	OC3PE	Output compare 3 preload enable
[18:17]		2'h0	RSVD	
[16]	rw	1'h0	OC3CE	Output compare 3 clear enable
[15:12]	rw	4'h0	IC4F	Input capture 4 filter
[11:10]	rw	2'h0	IC4PSC	Input capture 4 prescaler
[9:8]	rw	2'h0	CC4S	Capture/Compare 4 selection This bit-field defines the direction of the channel (input/output) as well as the used input. 00: CC4 channel is configured as output 01: CC4 channel is configured as input, IC4 is mapped on TI4 10: CC4 channel is configured as input, IC4 is mapped on TI3 11: CC4 channel is configured as input, IC4 is mapped on TRC. This mode is working only if an internal trigger input is selected through TS bit (SMCR register)
[7:4]	rw	4'h0	IC3F	Input capture 3 filter
[3:2]	rw	2'h0	IC3PSC	Input capture 3 prescaler
[1:0]	rw	2'h0	CC3S	Capture/Compare 3 selection This bit-field defines the direction of the channel (input/output) as well as the used input. 00: CC3 channel is configured as output 01: CC3 channel is configured as input, IC3 is mapped on TI3 10: CC3 channel is configured as input, IC3 is mapped on TI4 11: CC3 channel is configured as input, IC3 is mapped on TRC. This mode is working only if an internal trigger input is selected through TS bit (SMCR register)
0x20		**0x00000000**	**CCER**	**Capture/Compare enable register**
[31:16]		16'h0	RSVD	
[15]	rw	1'h0	CC4NP	Capture/Compare 4 output Polarity.
[14]		1'h0	RSVD	
[13]	rw	1'h0	CC4P	Capture/Compare 4 output Polarity.
[12]	rw	1'h0	CC4E	Capture/Compare 4 output enable.
[11]	rw	1'h0	CC3NP	Capture/Compare 3 output Polarity.
[10]		1'h0	RSVD	
[9]	rw	1'h0	CC3P	Capture/Compare 3 output Polarity.

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表 8-3: GPTIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[8]	rw	1'h0	CC3E	Capture/Compare 3 output enable.
[7]	rw	1'h0	CC2NP	Capture/Compare 2 output Polarity.
[6]		1'h0	RSVD	
[5]	rw	1'h0	CC2P	Capture/Compare 2 output Polarity.
[4]	rw	1'h0	CC2E	Capture/Compare 2 output enable.
[3]	rw	1'h0	CC1NP	Capture/Compare 1 output Polarity. CC1 channel configured as output: CC1NP must be kept cleared in this case. CC1 channel configured as input: This bit is used in conjunction with CC1P to define TI1FP1/TI2FP1 polarity. refer to CC1P description.
[2]		1'h0	RSVD	
[1]	rw	1'h0	CC1P	Capture/Compare 1 output Polarity. CC1 channel configured as output: 0: OC1 active high 1: OC1 active low CC1 channel configured as input: CC1NP/CC1P bits select TI1FP1 and TI2FP1 polarity for trigger or capture operations. 00: noninverted/rising edge Circuit is sensitive to TIxFP1 rising edge (capture, trigger in reset, external clock or trigger mode), TIxFP1 is not inverted (trigger in gated mode, encoder mode). 01: inverted/falling edge Circuit is sensitive to TIxFP1 falling edge (capture, trigger in reset, external clock or trigger mode), TIxFP1 is inverted (trigger in gated mode, encoder mode). 10: reserved, do not use this configuration. 11: noninverted/both edges Circuit is sensitive to both TIxFP1 rising and falling edges (capture, trigger in reset, external clock or trigger mode), TIxFP1 is not inverted (trigger in gated mode). This configuration must not be used for encoder mode.
[0]	rw	1'h0	CC1E	Capture/Compare 1 output enable. CC1 channel configured as output: 0: Off - OC1 is not active 1: On - OC1 signal is output on the corresponding output pin CC1 channel configured as input: This bit determines if a capture of the counter value can actually be done into the input capture/compare register 1 (CCR1) or not. 0: Capture disabled 1: Capture enabled
0x24		**0x00000000**	**CNT**	**Counter**
[31]	r	1'h0	UIFCPY	Value depends on IUFREMAP in CR1. If UIFREMAP = 1 UIFCPY: UIF Copy This bit is a read-only copy of the UIF bit of the ISR register
[30:16]		15'h0	RSVD	
[15:0]	rw	16'h0	CNT	counter value
0x28		**0x00000000**	**PSC**	**Prescaler**
[31:16]		16'h0	RSVD	

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表 8-3: GPTIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[15:0]	rw	16'h0	PSC	Prescaler value The counter clock frequency is equal to fCLK / (PSC[15:0] + 1). PSC contains the value to be loaded in the active prescaler register at each update event (including when the counter is cleared through UG bit of EGR register or through trigger controller when configured in "reset mode").
0x2C		**0x00000000**	**ARR**	**Auto-reload register**
[31:16]		16'h0	RSVD	
[15:0]	rw	16'h0	ARR	Auto-reload value ARR is the value to be loaded in the actual auto-reload register.
0x30		**0x00000000**	**RCR**	**Repetition counter register**
[31:8]		24'h0	RSVD	
[7:0]	rw	8'h0	REP	Repetition counter value These bits allow the user to set-up the update rate of the compare registers (i.e. periodic transfers from preload to active registers) when preload registers are enable, as well as the update interrupt generation rate, if this interrupt is enable. Each time the REP_CNT related downcounter reaches zero, an update event is generated and it restarts counting from REP value. As REP_CNT is reloaded with REP value only at the repetition update event, any write to the RCR register is not taken in account until the next repetition update event. It means in PWM mode (REP+1) corresponds to the number of PWM periods in edge-aligned mode.
0x34		**0x00000000**	**CCR1**	**Capture/Compare register 1**
[31:16]		16'h0	RSVD	
[15:0]	rw	16'h0	CCR1	Capture/Compare 1 value If channel CC1 is configured as output: CCR1 is the value to be loaded in the actual capture/compare 1 register (preload value).It is loaded permanently if the preload feature is not selected in the CCMR1 register (bit OC1PE). Else the preload value is copied in the active capture/compare 1 register when an update event occurs. The active capture/compare register contains the value to be compared to the counter CNT and signaled on OC1 output. If channel CC1is configured as input: CCR1 is the counter value transferred by the last input capture 1 event (IC1). The CCR1 register is read-only and cannot be programmed.
0x38		**0x00000000**	**CCR2**	**Capture/Compare register 2**
[31:16]		16'h0	RSVD	
[15:0]	rw	16'h0	CCR2	Capture/Compare 2 value If channel CC2 is configured as output: CCR2 is the value to be loaded in the actual capture/compare 2 register (preload value).It is loaded permanently if the preload feature is not selected in the CCMR1 register (bit OC2PE). Else the preload value is copied in the active capture/compare 2 register when an update event occurs. The active capture/compare register contains the value to be compared to the counter CNT and signalled on OC2 output. If channel CC2 is configured as input: CCR2 is the counter value transferred by the last input capture 2 event (IC2). The CCR2 register is read-only and cannot be programmed.
0x3C		**0x00000000**	**CCR3**	**Capture/Compare register 3**
[31:16]		16'h0	RSVD	

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表 8-3: GPTIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[15:0]	rw	16'h0	CCR3	Capture/Compare value If channel CC3 is configured as output: CCR3 is the value to be loaded in the actual capture/compare 3 register (preload value).It is loaded permanently if the preload feature is not selected in the CCMR2 register (bit OC3PE). Else the preload value is copied in the active capture/compare 3 register when an update event occurs. The active capture/compare register contains the value to be compared to the counter CNT and signalled on OC3 output. If channel CC3is configured as input: CCR3 is the counter value transferred by the last input capture 3 event (IC3). The CCR3 register is read-only and cannot be programmed.
0x40		**0x00000000**	**CCR4**	**Capture/Compare register 4**
[31:16]		16'h0	RSVD	
[15:0]	rw	16'h0	CCR4	Capture/Compare value 1. if CC4 channel is configured as output: CCR4 is the value to be loaded in the actual capture/compare 4 register (preload value).It is loaded permanently if the preload feature is not selected in the CCMR2 register (bit OC4PE). Else the preload value is copied in the active capture/compare 4 register when an update event occurs. The active capture/compare register contains the value to be compared to the counter CNT and signalled on OC4 output. 2. if CC4 channel is configured as input: CCR4 is the counter value transferred by the last input capture 4 event (IC4). The CCR4 register is read-only and cannot be programmed.

8.3.5 定时器级联

表 8-4: 定时器级联

下级定时器	级联端口	上级定时器
ATIM1	ITR0	BTIM2
	ITR1	GPTIM2
	ITR2	GPTIM1
	ITR3	BTIM1
GPTIM1	ITR0	GPTIM2
	ITR1	BTIM2
	ITR2	ATIM1
	ITR3	BTIM1
GPTIM2	ITR0	GPTIM1
	ITR1	ATIM1
	ITR2	BTIM1
	ITR3	BTIM2
BTIM1	ITR0	BTIM2
	ITR1	GPTIM1
	ITR2	ATIM1
	ITR3	GPTIM2
BTIM2	ITR0	GPTIM1
	ITR1	BTIM1
	ITR2	GPTIM2
	ITR3	ATIM1

8.4 LPTIM

8.4.1 简介

LPTIM (Low Power Timer) 基于一个 24 比特递增计数器，可实现计时、产生输出波形 (输出比较和 PWM) 和唤醒系统等功能。计数时钟可以为系统时钟，低功耗时钟，IO 输入信号或比较器输出，并可进行最多 128 倍的预分频以及最多 256 次的循环计数。根据计数结果可以产生 PWM 输出，并可产生中断，或产生唤醒信号将系统从低功耗模式唤醒。当用 IO 输入信号作为计数时钟时，支持不依赖于内部时钟进行计数并产生唤醒信号。

8.4.2 主要特性

- 24 位向上自动重装载计数器，最大计数 16777215(2^24-1)
- 计数时钟选择
  - 内部时钟，PCLK2 或低功耗时钟
  - 可选边沿的 IO 输入信号或比较器输出，可利用内部时钟进行防抖动，也可不依赖内部时钟独立计数
- 8 档预分频，计数时钟分频系数为 2 的 0~7 次方
- 1~256 循环次数
- 计数模式
  - 连续计数模式

  - 单笔计数模式，循环次数完成后计数结束
- 可配极性的输出模式
  - PWM 输出，可配脉宽，周期
  - 单次翻转输出
  - 单脉冲或指定个数脉冲输出
- 触发模式
  - 软件触发
  - IO 输入信号边沿触发，支持防抖动滤波
- 超时检测，每次外部触发时计数器复位
- 如下事件发生时产生中断或唤醒信号：
  - 更新
  - 计数器溢出
  - 输出比较
  - 外部触发

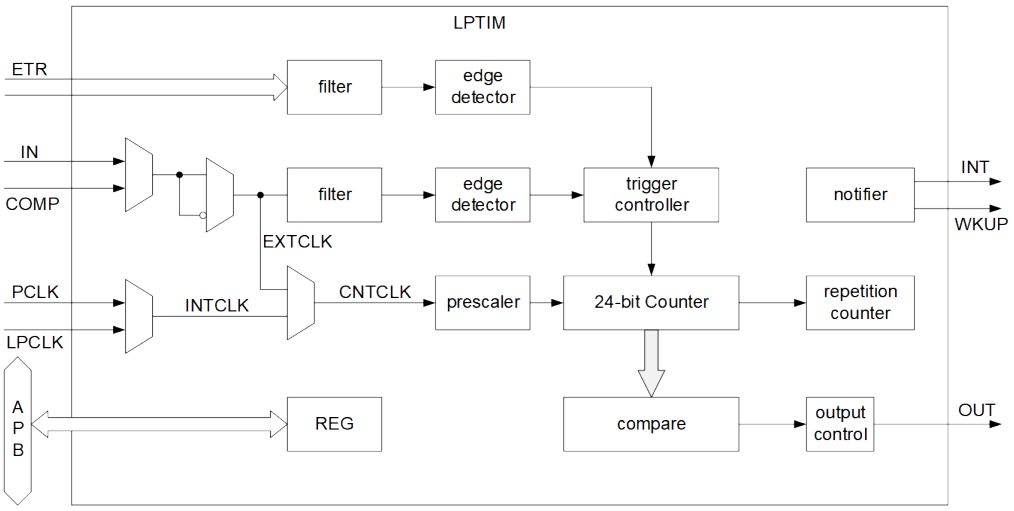

图 8-13: LPTIM 结构图

8.4.3 LPTIM 功能描述

8.4.3.1 计数器

LPTIM 的各项功能均基于一个 24 比特的计数器。计数器基于事件计数，包括时钟翻转、外部输入翻转、比较器结果翻转等。

计数事件经过预分频处理才会真正进入计数器。预分频的次数介于 1 到 128 之间 (2^CFGR_PRESCPSC)，即仅当发生了 (2^CFGR_PRESCPSC) 次计数事件，计数器的值才真正改变一次。

计数器固定为递增计数模式，计数器从 0 计数到自动重载值 ARR，然后重新从 0 开始计数并产生计数器上溢事件。

计数值可以通过 CNT 读出。由于计数时钟与 APB 时钟异步，需要连续两次读取的数值相同才能认为是一次有效数据读取。

8.4.3.2 计数时钟

LPTIM 计数器的计数时钟 CNTCLK 可以在多个来源中选择。最常用的默认模式是选择内部低功耗时钟 LPCLK，此时 LPTIM 可以在芯片进入低功耗睡眠模式以后继续保持工作。当不处于低功耗睡眠模式时，LPTIM 也可以选择内部 PCLK 做时钟。LPTIM 还能够不依赖于内部时钟，直接用外部信号 IN 或者比较器输出信号 COMP 做时钟进行计数。时钟选择相关的寄存器包括 CFGR_EXTCKSEL/INTCKSEL/CKSEL。外部时钟的极性可以用 CFGR_CKPOL 选择。

当选择内部时钟时，还可以对外部信号 IN 或者比较器输出信号 COMP 翻转的事件进行计数，并能够进行预滤波和边沿选择处理。这种模式下应保证内部时钟的翻转频率至少为外部信号 IN 或者比较器输出信号 COMP 翻转频率的五倍。

8.4.3.3 更新事件 (UEV)

更新事件用于标志一个计数单元的结束。最基本的更新事件产生于每次计数器上溢时 (未开启重复计数时)。更新事件可以产生中断和唤醒信号，是定时器最基本的一项通知功能。

8.4.3.4 重复计数

如果配置了重复计数器 (RCR>0)，每次计数器上溢时重复计数器会递减，并仅当重复计数器为 0 时才产生更新事件。

重复计数器的当前值可以通过 RCR 读出。由于计数时钟与 APB 时钟异步，需要连续两次读取的数值相同才能认为是一次有效数据读取。

8.4.3.5 计数器触发

计数器可配置为一级触发模式 (CFGR_TRIGEN=00) 或两级触发模式 (CFGR_TRIGEN!=00)。

一级触发模式为软件触发，包括单次触发和连续触发两种。触发前，需先将 CR_ENABLE 置 1 使能计数器。随后将 CR_SNGSTRT 置 1 启动单次触发，计数器即刻启动，并在更新事件后停止；或将 CR_CNTSTRT 置 1 启动连续触发，计数器即刻启动持续计数直到计数器关闭使能或复位。

两级触发模式在软件触发基础上增加硬件触发机制，仅当经过滤波的 ETR 可选边沿到来时才真正启动计数器。

8.4.3.6 超时监测

在两级触发模式下，如果将 CFGR_TIMOUT 置 1，则每次硬件触发时均会复位计数器并重新启动计数。该功能可用于监测两个连续触发信号之间的间隔，当间隔超出预期时产生比较或更新事件。

8.4.3.7 PWM 输出

LPTIM 可以产生周期、占空比可控的单路 PWM 输出至 OUT 端口。PWM 输出的周期由 ARR 决定，占空比由 CMP 决定。计数器值 CNT 与 CMP 进行比较，生成 PWM，极性通过 CFGR_WAVEPOL 配置。单次触发模式下，根据 RCR 的值可生成单个或多个脉冲。连续触发模式下可生成持续的 PWM。如果 CFGR_WAVE 为 1，可以生成单次置 1 波形。

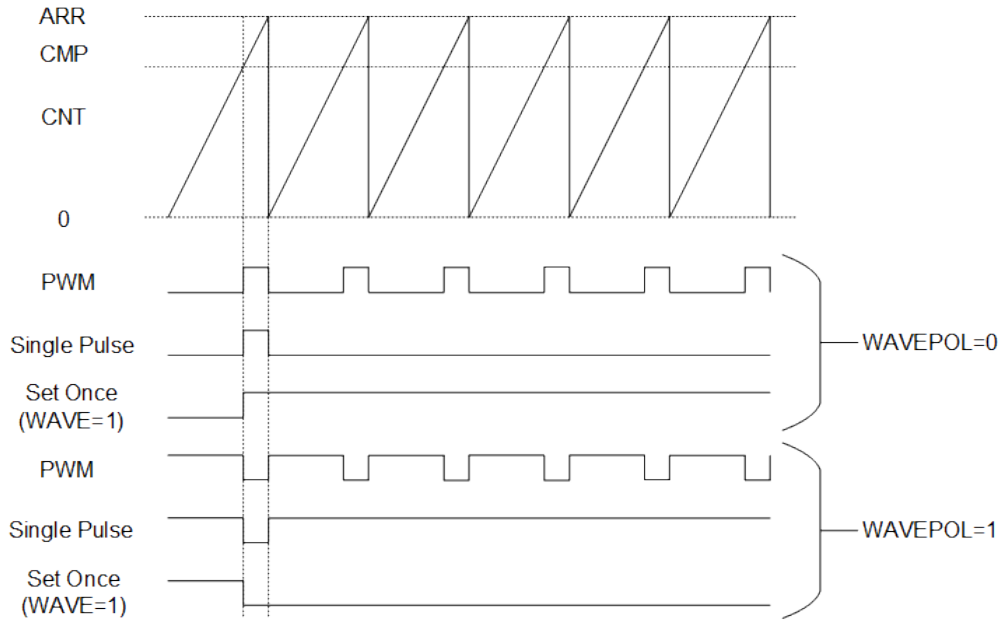

图 8-14: PWM 输出

8.4.3.8 通知机制

LPTIM 能够产生中断和唤醒等通知。中断仅在系统处于非低功耗睡眠状态时产生。唤醒信号无论系统是否处于低功耗睡眠状态均可产生，并能够将系统唤醒。能够触发通知的事件主要包括上溢事件、更新事件、触发事件、比较器匹配等。IER 寄存器可以控制各种事件是否产生中断和唤醒。各事件状态可在 ISR 寄存器中查询。

8.4.4 LPTIM 寄存器

表 8-5: LPTIM 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00		**0x00000000**	**ISR**	**LPTIM interrupt and status register**
[31:11]		21'h0	RSVD	
[10]	r	1'h0	OCWKUP	Indicates output compare wakeup occurred The OCWKUP bit is set by hardware when LPTIM_CNT register value reached the LPTIM_CMP register's value. To clear OCWKUP, first write 0 to the OCWE bit in the LPTIM_IER register to disable, then write 1 to the WKUPCLR bit in the LPTIM_ICR register.
[9]	r	1'h0	OFWKUP	Indicates overflow wakeup occurred OFWKUP is set by hardware when LPTIM_CNT register's value reached the LPTIM_ARR register's value and count from zero again. To clear OFWKUP, first write 0 to the OFWE bit in the LPTIM_IER register to disable, then write 1 to the WKUPCLR bit in the LPTIM_ICR register.
[8]	r	1'h0	UEWKUP	Indicates update event wakeup occurred UEWKUP is set by hardware when an update event was generated (overflow occurred while repetition counter reached zero). To clear UEWKUP, first write 0 to the UEWE bit in the LPTIM_IER register to disable, then write 1 to the WKUPCLR bit in the LPTIM_ICR register.
[7:4]		4'h0	RSVD	

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表 8-5: LPTIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[3]	r	1'h0	ET	External trigger edge event ET is set by hardware to inform application that a valid edge on the selected external trigger input has occurred. If the trigger is ignored because the timer has already started, then this flag is not set. ET flag can be cleared by writing 1 to the ETCLR bit in the LPTIM_ICR register.
[2]	r	1'h0	OC	Output compare match The OC bit is set by hardware to inform application that LPTIM_CNT register value reached the LPTIM_CMP register's value. OC flag can be cleared by writing 1 to the OCCLR bit in the LPTIM_ICR register.
[1]	r	1'h0	OF	Overflow occurred OF is set by hardware to inform application that LPTIM_CNT register's value reached the LPTIM_ARR register's value and count from zero again. OF flag can be cleared by writing 1 to the OFCLR bit in the LPTIM_ICR register.
[0]	r	1'h0	UE	LPTIM update event occurred UE is set by hardware to inform application that an update event was generated when overflow occurred while repetition counter reached zero. UE flag can be cleared by writing 1 to the UECLR bit in the LPTIM_ICR register.
0x04		**0x00000000**	**ICR**	**LPTIM interrupt and status clear register**
[31:9]		23'h0	RSVD	
[8]	w	1'h0	WKUPCLR	wakeup status clear flag Writing 1 to this bit clears all wakeup status flags in the LPTIM_ISR register.
[7:4]		4'h0	RSVD	
[3]	w	1'h0	ETCLR	External trigger valid edge clear flag Writing 1 to this bit clears the ET flag in the LPTIM_ISR register
[2]	w	1'h0	OCCLR	Output compare clear flag Writing 1 to this bit clears the OC flag in the LPTIM_ISR register
[1]	w	1'h0	OFCLR	Overflow clear flag Writing 1 to this bit clears the OF flag in the LPTIM_ISR register
[0]	w	1'h0	UECLR	Update event clear flag Writing 1 to this bit clear the UE flag in the LPTIM_ISR register.
0x08		**0x00000000**	**IER**	**LPTIM interrupt and wakeup enable register**
[31:11]		21'h0	RSVD	
[10]	rw	1'h0	OCWE	Output compare Wakeup Enable 0: Output compare wakeup disabled 1: Output compare wakeup enabled
[9]	rw	1'h0	OFWE	Overflow Wakeup Enable 0: Overflow Wakeup disabled 1: Overflow Wakeup enabled
[8]	rw	1'h0	UEWE	Update event Wakeup enable 0: Update event Wakeup disabled 1: Update event Wakeup enabled
[7:4]		4'h0	RSVD	
[3]	rw	1'h0	ETIE	External trigger valid edge Interrupt Enable 0: External trigger interrupt disabled 1: External trigger interrupt enabled
[2]	rw	1'h0	OCIE	Output compare Interrupt Enable 0: Output compare interrupt disabled 1: Output compare interrupt enabled

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表 8-5: LPTIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[1]	rw	1'h0	OFIE	Overflow Interrupt Enable 0: Overflow interrupt disabled 1: Overflow interrupt enabled
[0]	rw	1'h0	UEIE	Update event interrupt enable 0: Update event interrupt disabled 1: Update event interrupt enabled
0x0C		**0x00000000**	**CFGR**	**LPTIM configuration register**
[31:24]		8'h0	RSVD	
[23]	rw	1'h0	COUNTMODE	counter mode in internal clock source mode (CKSEL=0). If CKSEL=1, this bit has no effect. 0: the counter is incremented following each internal clock pulse 1: the counter is incremented following each valid pulse on the external clock
[22]		1'h0	RSVD	
[21]	rw	1'h0	WAVPOL	Waveform shape polarity The WAVEPOL bit controls the output polarity 0: The LPTIM output reflects the compare results between LPTIM_ARR and LPTIM_CMP registers 1: The LPTIM output reflects the inverse of the compare results between LPTIM_ARR and LPTIM_CMP registers
[20]	rw	1'h0	WAVE	Waveform shape The WAVE bit controls the output shape 0: Deactivate Set-once mode 1: Activate the Set-once mode
[19]	rw	1'h0	TIMOUT	Timeout enable The TIMOUT bit controls the Timeout feature 0: A trigger event arriving when the timer is already started will be ignored 1: A trigger event arriving when the timer is already started will reset and restart the LPTIM counter and the repetition counter
[18:17]	rw	2'h0	TRIGEN	Trigger enable and polarity The TRIGEN bits controls whether the LPTIM counter is started by an external trigger or not. If the external trigger option is selected, three configurations are possible for the trigger active edge: 00: software trigger (counting start is initiated by software) 01: rising edge is the active edge 10: falling edge is the active edge 11: both edges are active edges
[16]		1'h0	RSVD	
[15:13]	rw	3'h0	TRIGSEL	Trigger selector The TRIGSEL bits select the trigger source that will serve as a trigger event for the LPTIM among the below 8 available sources: 000: lptim_ext0 001: lptim_ext1 010: lptim_ext2 011: lptim_ext3 100: lptim_ext4 101: lptim_ext5 110: lptim_ext6 111: lptim_ext7
[12]		1'h0	RSVD	

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表 8-5: LPTIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[11:9]	rw	3'h0	PRESC	Clock prescaler The PRESC bits configure the prescaler division factor. It can be one among the following division factors: 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128
[8]	rw	1'h0	EXTCKSEL	External clock source selector 0: external clock source is from lptim_in 1: external clock source is from LPCOMP (if LPCOMP integrated)
[7:6]	rw	2'h0	TRGFLT	Configurable digital filter for trigger The TRGFLT value sets the number of consecutive equal samples that should be detected when a level change occurs on an internal trigger before it is considered as a valid level transition. An internal clock source must be present to use this feature 00: any trigger active level change is considered as a valid trigger 01: trigger active level change must be stable for at least 2 clock periods before it is considered as valid trigger. 10: trigger active level change must be stable for at least 4 clock periods before it is considered as valid trigger. 11: trigger active level change must be stable for at least 8 clock periods before it is considered as valid trigger.
[5]	rw	1'h0	INTCKSEL	Internal clock source selector 0: internal clock source is clk_lp 1: internal clock source is pclk2
[4:3]	rw	2'h0	CKFLT	Configurable digital filter for external clock The CKFLT value sets the number of consecutive equal samples that should be detected when a level change occurs on an external clock signal before it is considered as a valid level transition. An internal clock source must be present to use this feature 00: any external clock signal level change is considered as a valid transition 01: external clock signal level change must be stable for at least 2 clock periods before it is considered as valid transition. 10: external clock signal level change must be stable for at least 4 clock periods before it is considered as valid transition. 11: external clock signal level change must be stable for at least 8 clock periods before it is considered as valid transition.

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表 8-5: LPTIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[2:1]	rw	2'h0	CKPOL	Clock Polarity If LPTIM is clocked by an external clock source, CKPOL bits is used to configure the active edge or edges used by the counter: 00: the rising edge is the active edge used for counting 01: the falling edge is the active edge used for counting 10: both edges are active edges. When both external clock signal edges are considered active ones, the LPTIM must also be clocked by an internal clock source with a frequency equal to at least four time the external clock frequency. 11: not allowed
[0]	rw	1'h0	CKSEL	Clock selector The CKSEL bit selects which clock source the LPTIM will use: 0: LPTIM is clocked by internal clock source, according to INTCKSEL 1: LPTIM is clocked by external clock source, according to EXTCKSEL
0x10		**0x00000000**	**CR**	**LPTIM control register**
[31:4]		28'h0	RSVD	
[3]	rw	1'h0	COUNTRST	Counter reset This bit is set by software and cleared by hardware. When set to 1 this bit will trigger a synchronous reset of the CNT register. Due to the synchronous nature of this reset, it only takes place after a synchronization delay. COUNTRST must never be set to 1 by software before it is already cleared to 0 by hardware. Software should consequently check that COUNTRST bit is already cleared to 0 before attempting to set it to 1.
[2]	w	1'h0	CNTSTRT	Timer start in Continuous mode This bit is set by software and cleared by hardware. In case of software start (TRIGEN[1:0] = 00), setting this bit starts the LPTIM in Continuous mode. If the software start is disabled (TRIGEN[1:0] different than 00), setting this bit starts the timer in Continuous mode as soon as an external trigger is detected. If this bit is set when a single pulse mode counting is ongoing, then the timer will not stop at the next match between ARR and CNT registers and the LPTIM counter keeps counting in Continuous mode.
[1]	w	1'h0	SNGSTRT	LPTIM start in Single mode This bit is set by software and cleared by hardware. In case of software start (TRIGEN[1:0] = 00), setting this bit starts the LPTIM in single pulse mode. If the software start is disabled (TRIGEN[1:0] different than 00), setting this bit starts the LPTIM in single pulse mode as soon as an external trigger is detected. If this bit is set when the LPTIM is in continuous counting mode, then the LPTIM will stop at the following match between ARR and CNT registers. If this bit is set simultaneously with CNTSTRT, then LPTIM will be in continuous counting mode.
[0]	rw	1'h0	ENABLE	LPTIM enable The ENABLE bit is set and cleared by software. 0:LPTIM is disabled 1:LPTIM is enabled
0x14		**0x00000000**	**CMP**	**LPTIM compare register**
[31:24]		8'h0	RSVD	
[23:0]	rw	24'h0	CMP	Compare value CMP is the compare value used by the LPTIM.

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表 8-5: LPTIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
0x18		**0x00000000**	**ARR**	**LPTIM autoreload register**
[31:24]		8'h0	RSVD	
[23:0]	rw	24'h0	ARR	Auto reload value ARR is the autoreload value for the LPTIM. This value must be strictly greater than the CMP[15:0] value.
0x1C		**0x00000000**	**CNT**	**LPTIM counter register**
[31:24]		8'h0	RSVD	
[23:0]	r	24'h0	CNT	Counter value When the LPTIM is running with an asynchronous clock, reading the CNT register may return unreliable values. So in this case it is necessary to perform two consecutive read accesses and verify that the two returned values are identical.
0x20		**0x00000000**	**RCR**	**LPTIM repetition register**
[31:8]		24'h0	RSVD	
[7:0]	rw	8'h0	REP	Repetition register value REP is the repetition value for the LPTIM. Read REP will return left repetition times. It should be noted that for a reliable REP register read access, two consecutive read accesses must be performed and compared. A read access can be considered reliable when the values of the two consecutive read accesses are equal.

8.5 WDT

8.5.1 简介

看门狗计时器作为一种计数器主要是用于在到达设定好的时间之后重置系统，以防止软件挂死。

看门狗计时器基本功能：

- 支持两种工作模式：
  - mode0
    - wdt 不会产生中断，在到达设定的时间之后会直接重置系统。
    - 最高支持 24bit 的计数器
  - mode1
    - 分为两段计数，在到达第一段设定的时间之后，会产生中断，在到达第二段设定的时间之后，再重置系统。
    - 每个时间段最高支持 24bit 的计数器
- 支持写保护，以防止软件对 wdt 进行误操作

8.5.2 WDT 的工作方式

wdt 根据需求有两种 reset 产生模式：

模式 1：只计数一轮，计数结束直接产生 reset 的信号。

模式 2：计数两轮，第一轮计数结束产生中断，第二轮计数结束产生 reset 信号。

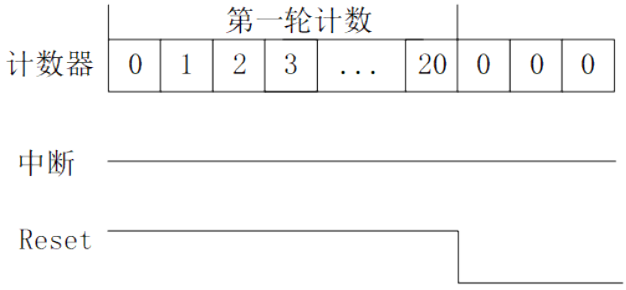

图 8-15: 模式 1 的中断以及 reset 信号产生与计数器的关系（假定超时值为 20，reset 低有效）

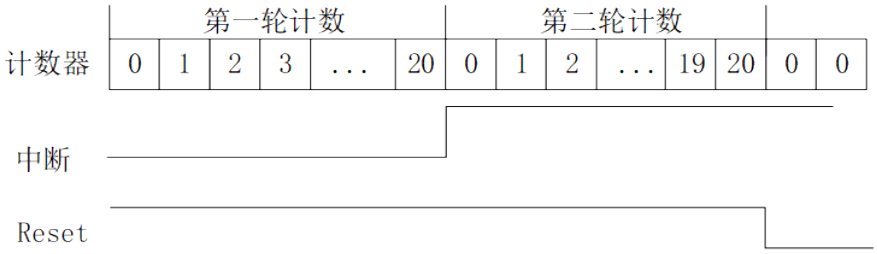

图 8-16: 模式 2 的中断以及 reset 信号产生与计数器的关系（假定超时值为 20，reset 低有效）

两种模式下的“喂狗”行为：

在模式 1 下，第一轮计数结束之前“喂狗”，则计数器从零开始重新计数；

在模式 2 下，第一轮计数结束之前“喂狗”，则计数器从零开始重新计数；如果第一轮计数器结束之前没有“喂狗”行为，则 wdt 进入第二轮计数，此时通过清除中断，或者“喂狗”的行为都可以让 wdt 重新进入第一轮开始计数。

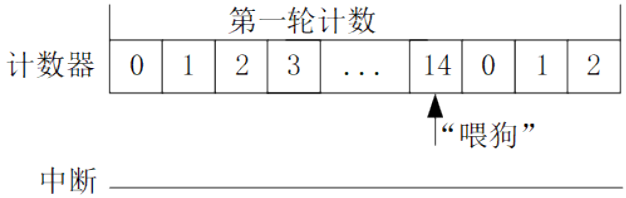

图 8-17: 模式 1“喂狗”行为对计数器的影响（假定超时值为 20）

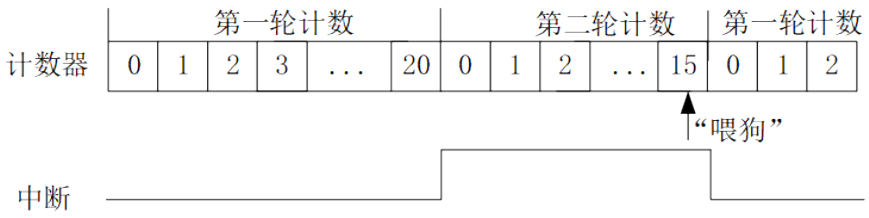

图 8-18: 模式 2 在第二轮计数时“喂狗“操作对计数器的影响，第一轮计数时的影响和模式 1 相同（假定超时值为 20）

两种模式下停止 wdt 的方式：

在模式 1 下，在计数结束之前配置寄存器 0x0C(counter_control)=0x34，wdt 则会停止；

在模式 2 下,在第一轮计数结束之前配置寄存器 0x0C(counter_control)=0x34,wdt 则会停止;如果在第二轮计数阶段则需要清除中断或者进行“喂狗”的操作让 wdt 回到第一轮计数才能进行配置寄存器 0x0C(counter_control)=0x34，让 wdt 停止。

清除中断的方法：

在模式 2 下，wdt 在第一轮计数完成之后会产生中断 0x14 WDT_SR 中 int_assert 为 1，此时可以通过配置 0x10 的 WDT_IDR 的 int_clr 来清除或者通过配置 0xc WDT_CCR 中 counter_control 为 0x76 即喂狗来清除。

8.5.2.1 WDT 寄存器配置流程

1. 根据需要选择 wdt 的工作模式。配置 0x08 中 response_mode 寄存器，配置 0x0 选择模式 1，配置 0x1 选择模式 2
2. 根据 wdt 触发 reset 时间配置 0x00 中 count_value_0 寄存器（两种模式下第一轮计数的超时值）以及 0x04 中的 count_value_1（模式 2 下第二轮计数器的超时值）
3. 根据需求配置 0x08 中 reset length 的长度
4. 配置 0x0c 中 counter_control 寄存器（=0x76）触发 wdt 开始工作
   1~3 的顺序没有要求，只要在 4 之前完成即可。

8.5.2.2 注意事项

1. wdt 提供了 write protect 写保护功能以防止 wdt 中的配置被意外改写，使用方法如下：
   配置 0x18 中 wrpt 寄存器为 0x58ab99fc，当 0x18 寄存器中 wrpt_st 为 1 说明写保护使能，此状态下 wdt 中的所有寄存器无法被改写但不影响读操作，如要取消写保护则配置 0x18 中 wrpt 寄存器为 0x51ff8621。
2. wdt 中 0x1c 的 sync_fg 寄存器为 1 表示 start，stop，irq clear，reset flag clear 的操作已经从 pclk 同步到 wdt clk 中即已经生效。
3. rst_fg 为 1 表示此 wdt 发生了 reset，此寄存器只有 iwdt 才有效。
4. 如果 0xc 中的 counter_control 写不进去，先 check 对应 sys rcc 里面的 wdt 时钟 enable 寄存器有没有配置为 1。

8.5.3 WDT 寄存器

表 8-6: WDT 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00			**WDT_CVR0**	**WatchDog Counter Value 0**
[31:24]		8'h0	RSVD	
[23:0]	rw	24'hffffff	count_value_0	Count Value for 1st TimeOut
0x04			**WDT_CVR1**	**WatchDog Counter Value 1**
[31:24]		8'h0	RSVD	
[23:0]	rw	24'hffffff	count_value_1	Count Value for 2nd TimeOut
0x08			**WDT_CR**	**WatchDog Control Register**
[31:5]		27'h0	RSVD	
[4]	rw	1'b1	response_mode	0:reset only, 1:interrupt and reset
[3]		1'b0	RSVD	

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表 8-6: WDT 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[2:0]	rw	3'b000	reset_length	reset pulse length in number of wdt clock cycles
0x0C			**WDT_CCR**	**WatchDog Counter Control Register**
[31:8]		24'h0	RSVD	
[7:0]	rw	8'h0	counter_control	SinglePulse /Write 8'h76 to restart, write8'h34 to stop, else do nothing
0x10			**WDT_ICR**	**WatchDog Interrupt Clear Register**
[31:1]		31'h0	RSVD	
[0]	w1c	1'b0	int_clr	SinglePulse /A pulse to clear interrupt
0x14			**WDT_SR**	**WatchDog Status Register**
[31:2]		30'h0	RSVD	
[1]	r	1'b0	wdt_active	Watchdog runs when 1, else 0
[0]	r	1'b0	int_assert	Interrupt assert when 1
0x18			**WDT_WP**	**WatchDog Write Protect Register**
[31]	r	1'b0	wrpt_st	1 indicates write protect is active
[30:0]	w	31'h0	wrpt	write 0x58ab99fc generate write_protect, write 0x51ff8621 to release
0x1C			**WDT_FG**	**WatchDog Flag Register**
[31:4]		28'h0	RSVD	
[3]	r	1'b0	sync_fg	1 indicates one transition from system clk to wdt clk has complicated
[2]	w1c	1'b0	sync_fg_clr	SinglePulse/A pulse to clear sync flag
[1]	r	1'b0	rst_fg	1 indicates wdt has already reset system
[0]	w1c	1'b0	rst_fg_clr	SinglePulse/A pulse to clear reset flag

9 图形

9.1 ePicasso™ 高性能 2.5D 图形引擎

在 2.5D 图像处理中，有许多常见的图像运算会耗费大量的 CPU 计算资源。ePicasso™ 则是专为 2.5D 图像运算设计的加速引擎，能够对 2.5D 图像运算中常见图层叠加、缩放、旋转等功能提供指数级的速度提升。除此以外，ePicasso™ 能够兼容各种常见的 RGB 图像格式，简化了系统中不同格式的图像格式转换。

9.1.1 图层叠加

ePicasso™ 最多支持两个前景图层，一个专用的掩膜图层，和一个单色背景图层叠加，输入和输出格式包括常用 RGB565、RGB888、ARGB8565、ARGB8888、L8、A8、A4、A2、YUV。每个前景图层有独立的叠加模式和叠加区域，掩膜图层主要是提取图像中特定的形状。除此以外，每个图层还提供了单独的 filter 配置选项，可以使图层滤除某一特定的颜色，该功能可用于简单的图像捕获。

9.1.2 图形缩放

ePicasso™ 有一个图层称为功能图层，除了支持叠加的功能外，这个功能图层还能够实现图形的缩放。缩放最大比例可以到达 1024 倍，精度则可以达到 1/65536。在 X 和 Y 方向上，缩放的比例可以分别配置，以此适应各种不同的需求。

9.1.3 图形旋转

ePicasso™ 的功能图层除了可以支持缩放的功能以外，还能够支持图像的高精度旋转。用户可以自定义旋转角的 sin/cos 值，来满足任意角度的旋转需求。旋转和缩放的功能可以同时启用，一次性完成图像的两种操作，提高了图像处理的性能。

9.2 LCD 控制器

LCD 控制器主要用于将 Framebuffer 内数据输出至外部显示，现有的 LCD 控制器可以支持常用的屏幕接口包括 DBI、DPI。此外，LCD 控制器还支持压缩格式的图像，使用压缩格式的图像可以显著降低 memory 的使用带宽，提升系统的性能。

9.2.1 TurboPixel™ 帧缓存压缩

为了提高图像的帧率和显示的平滑度，多个（两个或三个）帧缓存（Frame Buffer）是经常被使用的架构。通常来说为了将图像输出和图像处理并行化，需要专用的帧缓存用于向屏幕输出图像数据。为了能够减小这些帧缓存的存储空间和读取时候的带宽，MCU 系统中提供了基于自主算法的 TurboPixel™ 图像帧压缩模块。而在读取图像数据时，LCD 控制器中的解压缩模块可以直接读取压缩数据，并将解压缩后的数据输出到屏幕。这样就可以节省下帧缓存的存储空间和读取消耗的带宽资源。

9.2.2 显示接口

LCD 控制器主要完成显示用数据到主流显示接口之间的适配，本芯片支持的显示接口有：

9.2.2.1 MIPI-DBI

LCD 控制器可以支持 DBI 接口中的串行 SPI 模式和并行的 8080 模式。对于 SPI 模式，LCD 控制器可以支持 3 线和 4 线两种模式，同时也支持 dual/quad data line 两种工作方式。色彩格式上支持 8-bit RGB332、16-bit RGB565 和 24-bit RGB888。对于 8080 模式，LCD 控制器可以支持 8-bit、16-bit 和 24-bit 的总线位宽，同时支持 RGB332、RGB444、RGB565、RGB666、RGB888 等色彩格式。

9.2.2.2 JDI 反射屏

为了适应可穿戴产品的低功耗需求，JDI 研发超低功耗的反射屏。该屏幕利用太阳光线呈现图像，相较传统 LCD 屏幕耗电可以降低 95% 以上，配备在可穿戴产品上可以实现超长续航。LCD 控制器内也加入了 JDI 反射屏幕接口支持，包括串行接口和并行接口。两种接口最高可以支持到 64 色显示，支持局部刷新和整屏刷新，从而进一步降低屏幕刷新功耗，满足超长续航的需求。

9.3 eZip™ 无损压缩解码器

eZip™ 解码器是基于自有算法的实时无损解压缩模块，压缩率与 Zip 格式相当。它可以用于将通用数据解码后保存，以此加快数据的实时加载能力。如果数据是从芯片外部传输，压缩后的传输有助于缩短传输时间，减少传输功耗。

此外，eZip™ 还支持专有格式的图片压缩，压缩率与 PNG 格式相当，并支持独立 DMA 操作或与 ePicasso™ 联动读取。当独立操作时，eZip™ 可通过 DMA 机制，可以灵活地将存储在 Flash 或 RAM 的压缩图片解压缩并搬运至目标缓存中。在联动模式下，ePicasso™ 通过 eZip™ 模块，实时从存储中读取图片并实时解压缩，然后按照一般的图形流程进行所需要的 2.5D 计算，从而省去了暂存解压缩图片的缓存。

通过以上机制，eZip™ 可以有效地降低图像素材对存储容量的需求，在有限的存储中最大化素材的丰富度，减小对片外存储的带宽要求，从而提高大大系统的整体运行效率。

eZip™ 模块是将 eZip™ 压缩图片进行解码输出的模块。该模块通过 AHB 总线读入压缩数据，解码后的图像数据可配置通过 AHB 总线输出或直接送给 epic 模块进行后续处理。

该模块具有以下特点：

- 通过 AHB 总线输入\输出的数据地址可配
- 输出图片数据可直接送给 epic 模块
- 可输出一个指定区域的图片数据
- 支持解码参数 cache 功能，cache 命中的情况下可缩短解码时间

10 音频

10.1 PDM

10.1.1 简介

PDM (Pulse Density Modulation) 脉冲密度调制接口主要是用于将 PDM 麦克风采集到的 PDM 音频信号转化为 PCM（Pulse Code Modulation）脉冲编码调制信号以供后续的音频处理。

主要功能：

- 同时支持左右两路立体声信号，也可以单独采集单声道信号
- 可提供的 PDM 麦克风时钟速率：3.072MHz、1.536MHz、0.768MHz、1.024MHz、2.4MHz、1.6MHz、0.8MHz 等
- 支持 PCM 数据的速率：48kHz、32kHz、24kHz、16kHz、12kHz、8kHz 等
- 支持 32bit、24bit、16bit、8bit 的 PCM 信号
- 支持分辨率为 0.5dB 并且从-15dB 到 45dB 增益可调

10.1.2 使用说明

PDM(脉冲密度调制) 模块旨在支持数字麦克风。

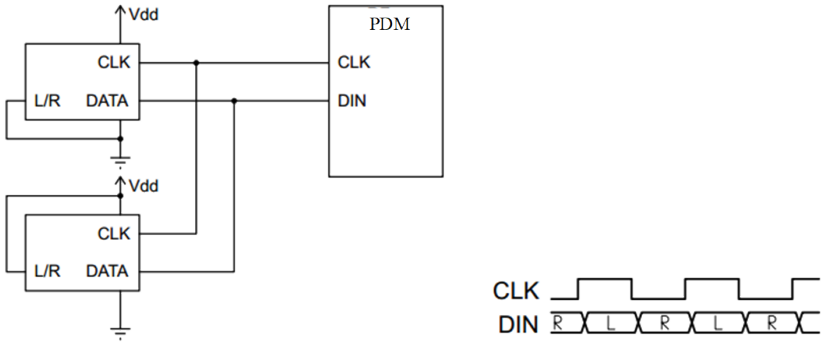


图 10-1: 数字麦克风通过 PDM 模块的典型连接

上图所示为一对数字麦克风通过 PDM 模块的典型连接，两个麦克风共用同一比特流时钟和数据线。借助麦克风的配置引脚 (L/R)，其中一个麦克风可在 CLK 上升沿提供有效数据，而另一个麦克风则在 CLK 下降沿提供有效数据。

10.1.2.1 PDM 模块的整体结构

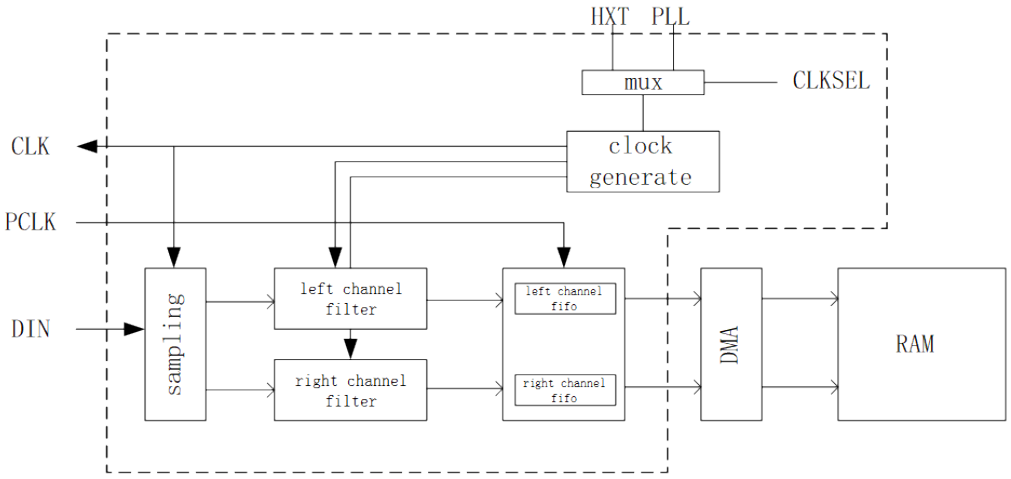


图 10-2: PDM 模块的整体结构

10.1.2.2 PDM 模块的时钟结构

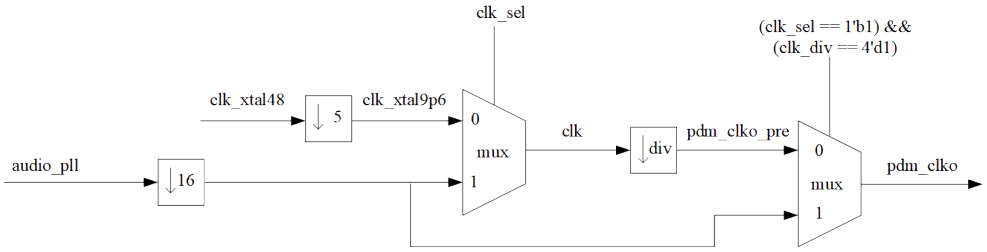


图 10-3: PDM 模块的时钟结构

PDM 模块的时钟源有两个，一个是系统的 48mHz 晶振，一个是系统的音频 PLL 经过 16 倍分频的时钟。而 48mHz 晶振在 PDM 模块内部先经过一个 5 倍的分频器得到一个 9.6mHz 的时钟，此时钟和音频 PLL 的时钟进行二选一，在经过可以配置的分频器得到最终送给数字麦克风的时钟 pdm_clko。pdm 模块最终的输出数据速率为 pdm_clko/(sinc_rate×lpf_downsample)。其中 sinc_rate 和 lpf_downsample 根据如下表格对寄存器 sinc_rate 以及 lpf_ds 进行配置得到最终的数据。

表 10-1: PDM 麦克风时钟源以及对应输出数据速率的配置关系表

PDM_CLK(MHz)	Fs (PCM 输出 Rate, KHz)	OSR（过采样率）	SINC RATE(CIC 下采样率)	LPF 后下采样率	SINC ORDER
3.072	48	64	32	2	3
3.072	32	96	48	2	3
3.072	24	128	64	2	3
3.072	16	192	96	2	3
3.072	12	256	64	4	3
3.072	8	384	96	4	3
1.536	48	32	16	2	4
1.536	32	48	24	2	4
1.536	24	64	32	2	3

续表下页...

表 10-1: PDM 麦克风时钟源以及对应输出数据速率的配置关系表（续）

PDM_CLK(MHz)	Fs (PCM 输出 Rate, KHz)	OSR（过采样率）	SINC RATE(CIC 下采样率)	LPF 后下采样率	SINC ORDER
1.536	16	96	48	2	3
1.536	12	128	64	2	3
1.536	8	192	96	2	3
0.768	24	32	16	2	4
0.768	16	48	24	2	4
0.768	12	64	32	2	3
0.768	8	96	24	4	4
1.024	32	32	16	2	4
1.024	16	64	32	2	3
1.024	8	128	64	2	3
2.4	48	50	25	2	4
2.4	24	100	50	2	3
2.4	16	150	75	2	3
2.4	12	200	100	2	3
2.4	8	300	75	4	3
1.6	32	50	25	2	4
1.6	16	100	50	2	3
1.6	8	200	100	2	3
0.8	16	50	25	2	4
0.8	8	100	50	2	3
2.4	32	75	75	LPF bypass	3
1.2	48	25	25	LPF bypass	4
1.2	24	50	25	2	4
1.2	16	75	75	LPF bypass	3
1.2	12	100	50	2	3
1.2	8	150	75	2	
2.8224	44.1	64	32	2	3
2.8224	22.05	128	64	2	3
2.8224	11.025	256	64	4	3
1.4112	44.14	32	16	2	4
1.4112	22.05	64	32	2	3
1.4112	11.025	128	64	2	3
0.7056	22.05	32	16	2	4
0.7056	11.025	64	32	2	3

以表中第一行的配置为例对 PDM 模块的寄存器配置进行说明。输出时钟 3.072mHz，输出数据速率 48kHz。输出数据位宽 16 比特，双声道打开。

PDM 寄存器的配置流程：

1. 根据表格选择输出的速率。根据表中的 PDM_CLK 选择时钟源，配置 0x00 中 clk_sel 寄存器，0x0 表示 pdm 模块的输入时钟为 9.6mHz，0x1 表示 pdm 模块的输入时钟为音频 PLL 的十六分频时钟。此例 clk_sel 的配置为 1。（音频时钟的配置不在此处讨论）
2. 根据表格中 SINC RATE 以及 SINC ORDER 配置 0x08 中 sinc_rate 以及 sinc_order_sel 寄存器，其中 sinc_order_sel 为 1 对应表格中 SINC ORDER 为 4，0 对应 3。根据 LPF 后下采样率配置 0x34 中 lpf_ds 寄存器以及 lpf_bypass 寄存器，配置 lpf_ds 寄存器 1 表示对应 excel 中 lpf 下采样 4，配置 lpf_ds 寄存器 0 表示对应 excel 中 lpf 下采样 2，配置 lpf_bypass 为 1 对应表格中的 LPF BYPASS。此例 0x08 sinc_rate=64，sinc_order_sel=0，0x34

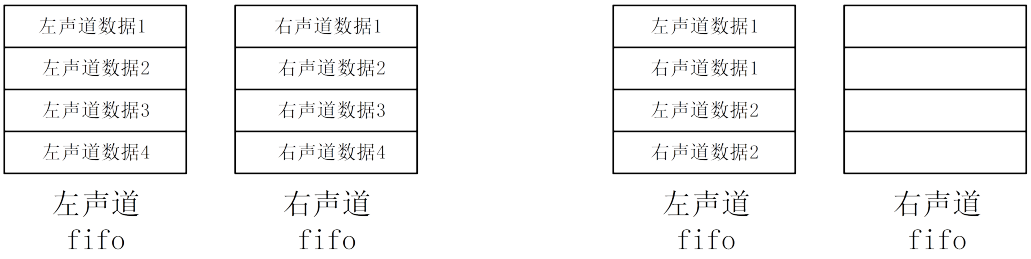
lpf_ds=0。

3. 根据声道配置打开对应的使能信号：

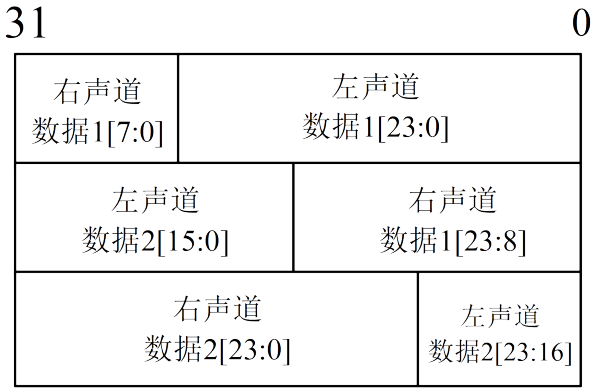
		双声道		左声道	右声道
寄存器 0x0 CFG0	left_en	1	0	1	0
	right_en	1	0	0	1
	stereo_en	0	1	0	0

在 0x0 的 swap_en 寄存器为 0 时，pdm 模块认为的右声道采集的是 pdm mic 上升沿输出的数据，左声道采集的是 pdm mic 下降沿输出的数据；在 0x0 的 swap_en 寄存器为 1 时则正好相反，pdm 模块认为的右声道采集的时 pdm mic 下降沿输出的数据，左声道采集的时 pdm mic 上升沿输出的数据。根据需求进行配置。此例 0x0 stereo_en=1 left_en=0 rignt_en=0 或者 stereo_en=0 left_en=1 rignt_en=1。

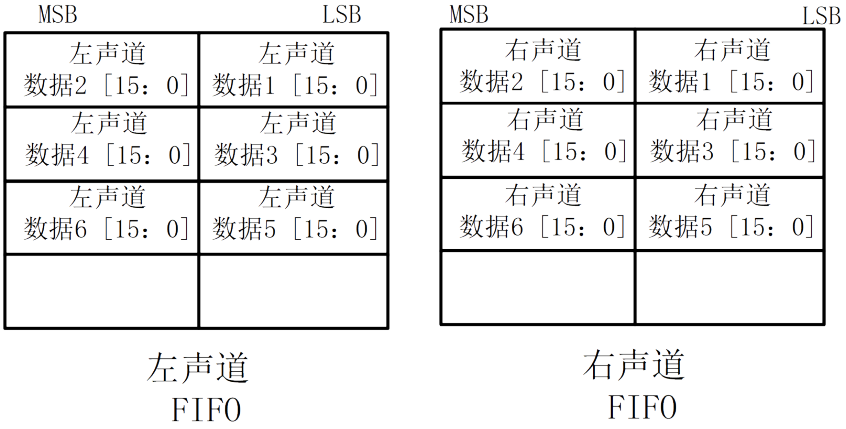
4. 根据 pdm 模块的输出数据格式进行配置，输出数据的位宽不同对 0x38 的 byte_trunc 寄存器进行配置，配置 0 对应 24bits 输出，配置 1 对应 16bits 输出，配置 2 对应 8bits 输出，配置 3 对应 32bits 输出。此例 0x38 byte_trunc 为 1。
5. 根据左右声道数据是否需要混合到一起配置 0x38 的 byte_con 寄存器，配置 0 左右两个声道的数据各自存到各自的 fifo 中，配置 1 则左右两个声道的数据都存在左声道的 fifo 中。不同 byte_con 寄存器配置对应的输出数据的存储区别示意图。



不满 32 比特的数据会自动将下一个数据的低位补到上一个数据的高位凑成 32 比特数据，以 24 比特双声道数据，byte_con 为 1 为例如下图所示。



以 16 比特双声道数据，byte_con 为 0 为例如下图所示。



此例中对数据存储格式没有要求，请使用者根据需求自行选择配置。

6. 根据 dma 的使用说明配置 dma 的寄存器用去将 pdm fifo 中的数据一次一个 32 比特数据通过 dma 搬到指定的 ram 地址中。
7. 配置 0x0 中 pdmcoreen 寄存器使能 pdm 模块。

1~6 的顺序不固定，只要在 7 之前完成即可。

10.1.2.3 注意事项

PDM 模块产生的中断都是 fifo 出现溢出产生错误发出的中断。

10.1.3 PDM 寄存器

表 10-2: PDM 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00			**CFG0**	
[31:10]		22'h0	RSVD	
[9]	rw	1'b0	swap_en	1: Swap right channel and left channel pdm data; 0: Not swap right channel and left channel pdm data
[8]	rw	1'b0	stereo_en	1:Enable double channels pdm data sampling; 0: Disable double channels pdm data sampling
[7]	rw	1'b0	right_en	1: Enable right channel pdm data sampling; 0: Disable right channel pdm data sampling
[6]	rw	1'b0	left_en	1: Enable left channel pdm data sampling; 0: Disable left channel pdm data sampling
[5:2]	rw	4'h4	clk_div	Clock frequency division ratio of 3.072MHz or 9.6MHz according to register clk_sel
[1]	rw	1'b0	clk_sel	1:Clk select dll 3.072MHz; 0: Clk selct xtal 9.6MHz
[0]	rw	1'b0	pdmcoreen	1:Enable pdm module; 0: Disable pdm module
0x04			**CFG1**	
[31:11]		21'h0	RSVD	
[10:8]	rw	3'h0	sample_dly_r	The number of delay dff before the right data stream in processing
[7:5]	rw	3'h0	sample_dly_l	The number of delay dff before the left data stream in processing
[4:0]		5 'b0	RSVD	
0x08			**SINC_CFG**	

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表 10-2: PDM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:9]		23'h0	RSVD	
[8]	rw	1'b1	sinc_order_sel	1:select four differentiators in sinc filter; 0:select three differentiators in sinc filter
[7:0]	rw	8'd32	sinc_rate	dowmsampling rate of sinc filter
0x14			**HPF_CFG**	
[31:6]		26'h0	RSVD	
[5]	rw	1'b1	hpf_rst	1:high-pass filter normal operation ; 0:reset high-pass filter
[4]	rw	1'b0	hpf_bypass	1:bypass-high pass filter ; 0: enable high-pass filter
[3:0]	rw	4'hd	hpf_coeff	coefficient of high-pass filter
0x18			**PGA_CFG**	
[31:14]		18'h0	RSVD	
[13:7]	rw	7'd0	pga_gain_r	right channel gain control , the range is -15dB 45dB. Resolution is 0.5dB/LSB
[6:0]	rw	7'd0	pga_gain_l	left channel gain control , the range is -15dB 45dB. Resolution is 0.5dB/LSB
0x34			**LPF_CFG6**	
[31:14]		18'h0	RSVD	
[13]	rw	1'b0	lpf_bypass	1:bypass low-pass filter ; 0: enable low-pass filter
[12]	rw	1'b0	lpf_ds	1:downsampling rate of low pass filter is two;0:No downsampling of low pass filter
[11:0]		12'h0	RSVD	
0x38			**FIFO_CFG**	
[31:9]		23'h0	RSVD	
[8]	rw	1'b0	lr_chg	1:exchange storage location of left and right channel; 0: don't exchange storage location of left and right channel
[7]	rw	1'b0	rx_dma_msk_l	1:disable left channel dma request; 0: enable left channel dma request
[6]	rw	1'b0	rx_dma_msk_r	1:disable right channel dma request; 0: enable right channel dma request
[5:3]	rw	3'h0	pdm_shift	the number of data left shift for higher data accuracy
[2:1]	rw	2'b0	byte_trunc	1: 16bits output ; 0: 24bits output ;2: 8bits output ; 3: 32bits output
[0]	rw	1'b0	byte_con	1: combine left channel and right channel; 0: not combine left channel and right channel
0x44			**FIFO_ST**	
[31:8]		24'h0	RSVD	
[7]	r	1'h0	full_l	1 indicates left channel fifo is full
[6]	r	1'b0	empty_l	1 indicates left channel fifo is empty
[5]	r	1'b0	almost_full_l	1 indicates left channel fifo is less than two full
[4]	r	1'b0	almost_empty_l	1 indicates left channel fifo is less than two datas left
[3]	r	1'h0	full_r	1 indicates right channel fifo is full
[2]	r	1'b0	empty_r	1 indicates right channel fifo is empty
[1]	r	1'b0	almost_full_r	1 indicates right channel fifo is less than two full
[0]	r	1'b0	almost_empty_r	1 indicates right channel fifo is less than two datas left
0x48			**INT_ST**	
[31:2]		30'h0	RSVD	
[1]	r	1'b0	overflow_l	1 indicates left channel fifo has already overflowed and as irq at same time
[0]	r	1'b0	overflow_r	1 indicates right channel fifo has already overflowed and as irq at same time
0x4c			**INT_MSK**	
[31:2]		30'h0	RSVD	
[1]	rw	1'b0	int_mask_l	1:disable left channel irq to system; 0: enable left channel irq to system
[0]	rw	1'b0	int_mask_r	1:disable right channel irq to system; 0: enable right channel irq to system
0x50			**INT_CLR**	
[31:2]		30'h0	RSVD	

续表下页...

表 10-2: PDM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[1]	w1c	1'b0	int_clr_l	clear left channel irq
[0]	w1c	1'b0	int_clr_r	clear right channel irq

10.2 I2S

10.2.1 简介

I2S(也叫 IIS，即：Inter IC Sound) 总线, 又称集成电路内置音频总线，是飞利浦公司为数字音频设备之间的音频数据传输而制定的一种总线标准，该总线采用主/从模式，专责于音频设备之间的数据传输，广泛应用于各种多媒体系统。

目前 I2S 有 MSB 对齐（左对齐），LSB 对齐（右对齐）和 I2S 标准模式。

I2S 标准模式如下图所示：

数据在跟随 LRCLK 传输的 BCLK 的第二个上升沿时传输 MSB，其他位一直到 LSB 按顺序传。传输依赖于字长、BCLK 频率和采样率 (BCLK=Fs x 声道数 x 采样位数)，在每个采样的 LSB 和下一个采样的 MSB 之间都应该有未用的 BCLK 周期，LRCLK 为 0 传输左声道数据，LRCLK 为 1 传输右声道数据。

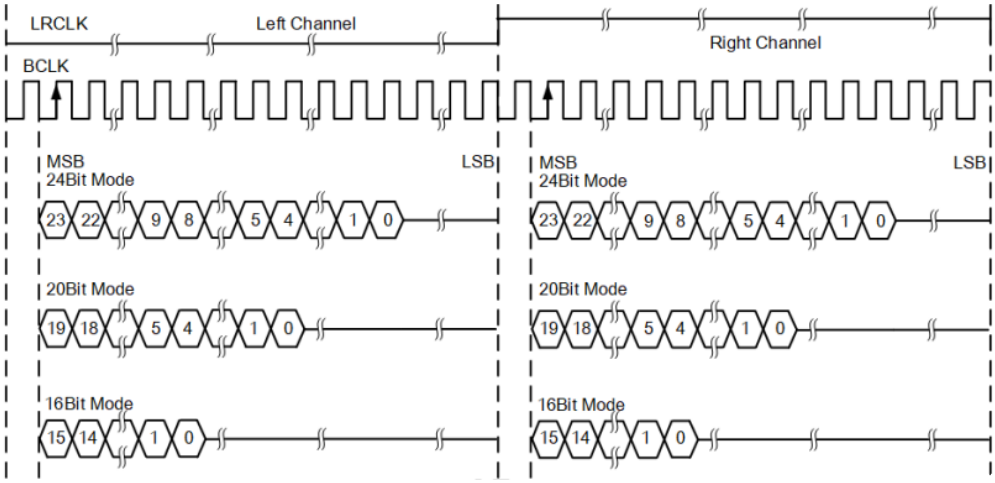

图 10-4: I2S 标准模式

I2S 左对齐如下图所示：

标准左对齐格式的数据的 MSB 没有相对于 BCLK 延迟一个时钟。左对齐格式的左右声道数据的 MSB 在 LRCLK 边沿变化后 BCLK 的第一个上升沿有效。LRCLK 为 1 传输左声道数据，LRCLK 为 0 传输右声道数据。

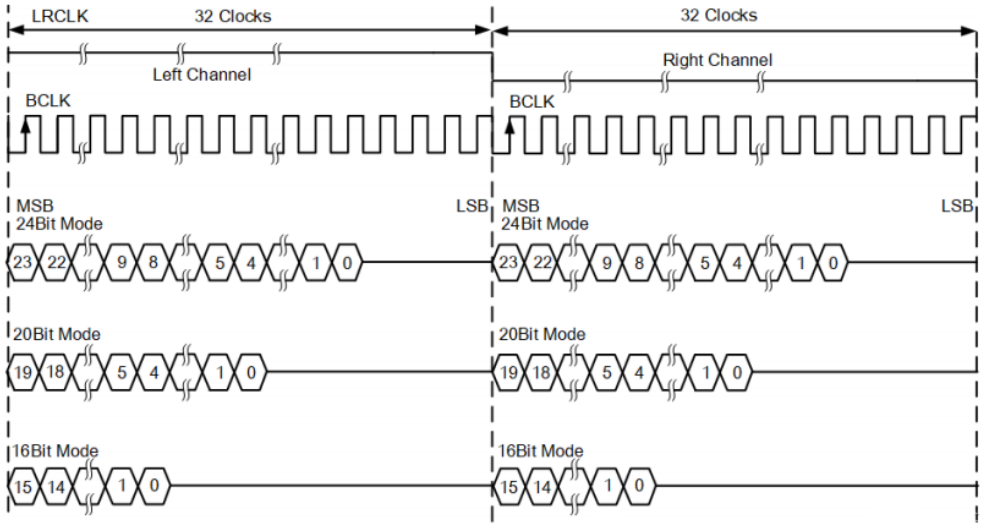

图 10-5: I2S 左对齐

I2S 右对齐如下图所示：

声音数据 LSB 传输完成的同时，LRCLK 完成第二次翻转，LRCLK 为 1 传输左声道数据，LRCLK 为 0 传输右声道数据。

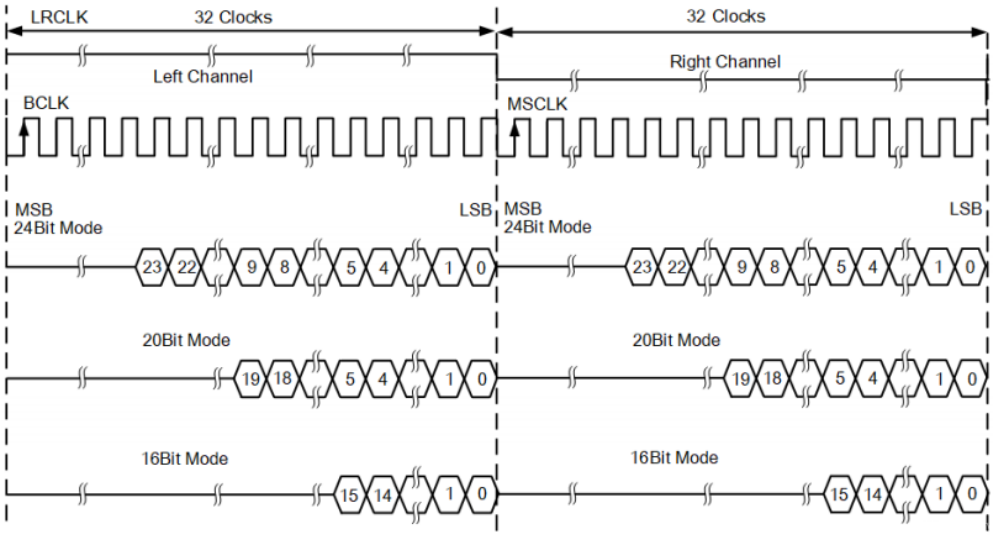

图 10-6: I2S 右对齐

10.2.2 I2S 功能描述

SF32LB52x 的 I2S 模块可以支持主从两种模式。主模式时，MCU 可以提供采样时钟 LRCK，bit 始终 BCLK 以及更高频率的同步工作时钟 MCLK。从模式时，BCLK 和 LRCK 由外部提供，MCU 负责 I2S 的数据收发。

SF32LB52x 可以支持 I2S，左对齐和右对齐三种数据格式。在主模式下，用户可以根据需求定义 MCLK，BCLK 和 LRCK 的比例关系。

10.2.3 I2S 寄存器

表 10-3: I2S 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x10		**0x00000010**	**TX_PCM_FORMAT**	
[31:6]		26'h0	RSVD	
[5]	rw	1'h0	track_flag	0: stereo 1: mono
[4:0]	rw	5'h10	dw	tx source pcm data width N(N>=8) common value is 8,13,14,16,18,20,22,24 This data width indicate the tx fifo output data width. When writing to tx fifo, please refer to following format: Mono 8 bit: fifo_data[31:0] = L3,L2,L1,L0, each word contains 4 samples, so four samples need read one word Stereo 8 bit: fifo_data[31:0] = R1,L1,R0,L0 , each word contains 2 samples, so two samples need read one word Mono 13/14/16 bit: fifo_data[31:0] = L1,L0, each word contains 2 samples, so two samples need read one word Stereo 13/14/16 bit: fifo_data[31:0] = R0,L0, each word contains 1 samples, so each sample need read one word Mono 18/20/22/24 bit: fifo_data[31:0] = L0, each word contains 1 samples, so each sample need read one word Stereo 18/20/22/24 bit: fifo_data[31:0][0] = L0, fifo_data[31:0][1]=R0, each 2 words contain 1 samples, so each sample need read two word
0x20		**0x000000FA**	**TX_PCM_SAMPLE_CLK**	
[31:13]		19'h0	RSVD	
[12:0]	rw	13'd250	fs_duty	source PCM sample clock duty cycle(with GCLK=12MHz): 250 for 48K FS 272 for 44.1K FS 375 for 32K FS 500 for 24K FS 544 for 22.05K FS 750 for 16K FS 1000 for 12K FS 1088 for 11.025K FS 1500 for 8K FS
0x30		**0x00000000**	**TX_RS_SMOOTH**	
[31:1]		31'h0	RSVD	
[0]	rw	1'h0	en	0: Disable TX re-sample smooth filter 1: Enable TX re-sample smooth filter This function is not implemented.
0x40		**0x00000000**	**TX_PCM_CH_SEL**	
[31:4]		28'h0	RSVD	
[3:2]	rw	2'h0	left_channel_sel	TX re-sampling module setting: 00: TX left = source left 01: TX left = source right 10,11: TX left = (source left + source right)/2

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表 10-3: I2S 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[1:0]	rw	2'h0	right_channel_sel	TX re-sampling module setting: 00: TX right = source right 01: TX right = source left 10,11: TX right = (source left + source right)/2
0x50		**0x0000000F**	**TX_VOL_CTRL**	
[31:4]		28'h0	RSVD	
[3:0]	rw	4'hf	vol	volume control: 0000: +6dB, 0001: +4.5dB, 0010: +3dB, 0011: +1.5dB, 0100: 0dB, 0101: -1.5dB, 0110: -3.0dB, 0111: -4.5dB, 1000: -6.0dB, 1001: -7.5dB, 1010: -9dB, 1011: -10.5dB, 1100: -12dB, 1101: -13.5dB, 1110: -15dB, 1111: mute Note: 1) +1.5db = 20log(1+1/4-1/16+1/1024) 2) -1.5dB = 20log(1-1/8-1/32-1/512-1/2048)
0x60		**0x00000000**	**TX_LR_BAL_CTRL**	
[31:6]		26'h0	RSVD	
[5:4]	rw	2'h0	en	LR balance enable: 00: both left and right in full volume 10: left channel balance volume adjustment enable 01: right channel balance volume adjustment enable 11: reserved, still kepp left and right in full volume
[3:0]	rw	4'h0	bal_vol	Balance volume control: 0000: Reserved, 0001: -1.5dB, 0010: -3.0dB, 0011: -4.5dB, 0100: -6.0dB, 0101: -7.5dB, 0110: -9.0dB, 0111: -10.5dB, 1000: -12dB, 1001: -13.5dB, 1010: -15dB, 1011: -16.5dB, 1100: -18dB, 1101: -19.5dB, 1110: -21dB, 1111: mute Note: 1) bit[5:0] = 101111 for left mute 2) bit[5:0] = 011111 for right mute 3) bit[5:4] = 00 or 11, bit[3:0] is don't care 4) +1.5db = 20log(1+1/4-1/16+1/1024) 5) -1.5dB = 20log(1-1/8-1/32-1/512-1/2048)
0x70		**0x007D007D**	**AUDIO_TX_LRCK_DIV**	
[31:28]		4'h0	RSVD	

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表 10-3: I2S 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[27:16]	rw	12'd125	duty_high	TX LRCK duty cycle high: 125 for 48K FS 136 for 44.1K FS 185 for 32K FS 250 for 24K FS 272 for 22.05K FS 375 for 16K FS 500 for 12K FS 544 for 11.025K FS 750 for 8K FS
[15:12]		4'h0	RSVD	
[11:0]	rw	12'd125	duty_low	TX LRCK duty cycle low: 125 for 48K FS 136 for 44.1K FS 190 for 32K FS 250 for 24K FS 272 for 22.05K FS 375 for 16K FS 500 for 12K FS 544 for 11.025K FS 750 for 8K FS Note: 1)duty_cycle = 12M/FS
0x80		**0x00000000**	**AUDIO_TX_BCLK_DIV**	
[31:6]		26'h0	RSVD	
[5:0]	rw	6'h5	duty	TX serial bit clock duty cycle 5 for 48K FS 4 for 44.1K FS 5 for 32KFS 10 for 24K FS 8 for 22.05K FS 15 for 16K FS 20 for 12K FS 16 for 11.025K FS 30 for 8KFs
0x90		**0x00000000**	**AUDIO_TX_FORMAT**	
[31:5]		27'h0	RSVD	
[4:0]	rw	5'h10	pcm_data_width	I2S out pcm data width M >= 16, common value: 16, 18, 20, 22, 24
0xa0		**0x00000000**	**AUDIO_SERIAL_TIMING**	
[31:4]		28'h0	RSVD	
[3]	rw	1'h0	lrck_pol	TX LRCK polarity control. 0: disable TX_LRCK inventor 1: enable TX_LRCK inventor for standard I2S, set tx_lrck_pol to low for Left/Right Justified, set tx_lrck_pol to hgih
[2]	rw	1'h0	slave_en	audio code transmit mode select. 0: master mode, 1: slave mode

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表 10-3: I2S 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[1:0]	rw	2'h0	timing	00: I2S mode 01: Left justified 10: right justified 11: reserved
0xb0		**0x00000000**	**AUDIO_TX_FUNC_EN**	
[31:2]		30'h0	RSVD	
[1]	rw	1'h0	tx_intf_sel	1: select external tx interface 0: select internal apb tx interface
[0]	rw	1'h0	tx_en	1: enable 0:disable
0xc0		**0x00000000**	**AUDIO_TX_PAUSE**	
[31:1]		31'h0	RSVD	
[0]	rw	1'h0	tx_pause	TX pause control when tx_enable = 1. 1: pause 0: TX work
0xc8		**0x00000000**	**AUDIO_I2S_SL_MERGE**	
[31:1]		31'h0	RSVD	
[0]	rw	1'h0	slave_timing_merge	when work as an I2S slave, and external I2S master TX/RX share an only BCLK/LRCK, we need set this bit high. 0: I2S slave use separated timing control port. TX_BCLK_IN/TX_LRCK_IN and RX_BCLK/RX_LRCK_IN are separated. 1: I2S slave use the same BCLK/LRCK, the TX_BCLK_IN/TX_LRCK also is used for RX controller.
0x100		**0x00000000**	**AUDIO_RX_FUNC_EN**	
[31:2]		30'h0	RSVD	
[1]	rw	1'h0	rx_intf_sel	1: select external rx interface 0: select internal apb rx interface
[0]	rw	1'h0	rx_en	1: enable 0: disable
0x110		**0x00000000**	**AUDIO_RX_PAUSE**	
[31:1]		31'h0	RSVD	
[0]	rw	1'h0	rx_pause	RX pause control when rx_enable = 1. 1: pause 0: RX work
0x120		**0x00040000**	**AUDIO_RX_SERIAL_TIMING**	
[31:4]		28'h0	RSVD	
[3]	rw	1'h0	lrck_pol	RX LRCK polarity control. 0: disable RX_LRCK inventor 1: enable RX_LRCK inventor for standard I2S, set tx_lrck_pol to low for Left/Right Justified, set tx_lrck_pol to hgih
[2]	rw	1'h0	slave_en	audio code receiver mode select. 0: master mode, 1: slave mode
[1:0]	rw	2'h0	timing	00: I2S 01: Left justified 10: right justified 11: reserved
0x130		**0x00000010**	**AUDIO_RX_PCM_DW**	
[31:5]		27'h0	RSVD	
[4:0]	rw	5'h10	pcm_data_width	For I2S and left justified mode, M can be 8,13,14,16 For right justified mode, M can be 8, 13, 14, 16, 18, 20, 22, 24
0x140		**0x007D007D**	**AUDIO_RX_LRCK_DIV**	

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表 10-3: I2S 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:28]		4'h0	RSVD	
[27:16]	rw	12'd125	duty_high	RX LRCK duty cycle high: 125 for 48K FS 136 for 44.1K FS 185 for 32K FS 250 for 24K FS 272 for 22.05K FS 375 for 16K FS 500 for 12K FS 544 for 11.025K FS 750 for 8K FS
[15:12]		4'h0	RSVD	
[11:0]	rw	12'd125	duty_low	RX LRCK duty cycle low: 125 for 48K FS 136 for 44.1K FS 190 for 32K FS 250 for 24K FS 272 for 22.05K FS 375 for 16K FS 500 for 12K FS 544 for 11.025K FS 750 for 8K FS Note: 1)duty_cycle = 12M/FS
0x150		**0x00000005**	**AUDIO_RX_BCLK_DIV**	
[31:10]		22'h0	RSVD	
[9:0]	rw	10'h5	duty	RX serial bit clock duty cycle 5 for 48K FS 4 for 44.1K FS 5 for 32KFS 10 for 24K FS 8 for 22.05K FS 15 for 16K FS 20 for 12K FS 16 for 11.025K FS 30 for 8KFs
0x160		**0x00000000**	**RECORD_DATA_SEL**	
[31:1]		31'h0	RSVD	
[0]	rw	1'h0	rs_data_sel	0: I2S audio recording 1: BT recording
0x170		**0x0000007D**	**RX_RE_SAMPLE_CLK_DIV**	
[31:13]		19'h0	RSVD	

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表 10-3: I2S 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[12:0]	rw	13'd250	rs_duty	source PCM sample clock duty cycle: 250 for 48K FS 272 for 44.1K FS 375 for 32K FS 500 for 24K FS 544 for 22.05K FS 750 for 16K FS 1000 for 12K FS 1088 for 11.025K FS 1500 for 8K FS Note: 1)duty_cycle = 12M/FS
0x180		**0x00000000**	**RX_RE_SAMPLE**	
[31:1]		31'h0	RSVD	
[0]	rw	1'h0	smooth_en	0: Disable RX re-sample smooth filter 1: Enable RX re-sample smooth filter
0x190		**0x00000000**	**RECORD_FORMAT**	
[31:2]		30'h0	RSVD	
[1]	rw	1'h0	track	1: mono recording, 0: stereo recording
[0]	rw	1'h0	dw	0: 8bit 1: 16bit RX fifo data format: Mono 8 bit (unsigned): RX FIFO_DIN[31:0] = L3,L2,L1,L0, each four samples need one FIFO write operation Stereo 8 bit (unsigned): RX_FIFO_DIN[31:0] = R1,L1,R0,L0, each tow samples need one FIFO write operation Mono 16 bit (Signed 2's complement): RX_FIFO_DIN[31:0] = L1,L0, each two samples need one FIFO write operation Stereo 16 bit (Signed 2's complement): RX_FIFO_DIN[31:0] = R0,L0, each sample need one FIFO write operation
0x1a0		**0x00000000**	**RX_CH_SEL**	
[31:4]		28'h0	RSVD	
[3:2]	rw	2'h0	left_channel_sel	RX re-sampling module setting: 00: RD left = RX left 01: RD left = RX right 10,11: RD left = (RX left + RX right)/2
[1:0]	rw	2'h0	right_channel_sel	RX re-sampling module setting: 00: RD right = RX right 01: RD right = RX left 10,11: RD right = (RX left + RX right)/2
0x200		**0x00000000**	**BT_PHONE_CTRL**	
[31:6]		26'h0	RSVD	
[5]	rw	1'h0	bb_i2s_bps_to_cdc	bypass baseband I2S interface to audio codec i2s interface 0: no bypass, 1: bypass
[4]	rw	1'h0	bt_pcm_if_bps	bypass baseband PCM signals to BT VCI master: 0: no bypass, 1: bypass
[3]	rw	1'h0	bt_path_sel	BT path select 0: digital path, 1: analog path
[2]	rw	1'h0	bt_mix_smooth_filter_en	0: disable the smooth filter for background mixer 1: enable the smooth filer for background mixer

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表 10-3: I2S 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[1]	rw	1'h0	bt_back_mix_en	background mixer enable 0: disable, 1: enable
[0]	rw	1'h0	bt_ph_en	BT phone enable 0: disable, 1: enable
0x210		**0x00000000**	**BB_PCM_FORMAT**	
[31:11]		21'h0	RSVD	
[10]	rw	1'h0	pcm_clk_pol	input BB pcm clock polarity: 0: rising edge for data transmitting, falling edge for data receiving 1: rising edge for data receiving, falling edge for data transmitting
[9]	rw	1'h0	i2s_lrck_pol	0: no bb_i2s_lrck input inventor 1: enable bb_i2s_lrck input inventor for standard I2S, set tx_lrck_pol to low for Left/Right Justified, set tx_lrck_pol to high
[8]	rw	1'h0	pcm_lsb_flag	Serial PCM data bit sequence. 0: MSB first, 1: LSB first
[7]	rw	1'h0	pcm_sync_flag	0: short sync, 1: long sync
[6:5]	rw	2'h0	pcm_tim_sel	00: I2S timing, 01: Left Justified 10: Right Justified, 11: PCM timing
[4:0]	rw	5'h8	pcm_dw	Baseband Master PCM data width (>=8) Common value: 8, 13,14, 16, 18, 20, 22, 24. for I2S/Left Justified/Right Kistified timing, bb_pcm_dw >=16 For PCM timing, only 8, 13, 14, 16 configure value is available.
0x220		**0x00000010**	**BT_PCM_DW**	
[31:5]		27'h0	RSVD	
[4:0]	rw	5'h10	dw	BT PCM master data width (>= 8), common value: 8, 13,14, 16
0x230		**0x00000000**	**BT_PCM_TIMING**	
[31:3]		29'h0	RSVD	
[2]	rw	1'h0	clk_pol	BT PCM master output pcm clock polarity: 0: rising edge for data transmitting, falling edge for data receiving 1: rising edge for data receiving, falling edge for data transmitting
[1]	rw	1'h0	sync_flag	0: short sync, 1: long sync
[0]	rw	1'h0	lsb_flag	Serial PCM data bit sequence. 0: MSB first, 1: LSB first
0x240		**0x00000000**	**BT_PCM_CLK_DUTY**	
[31:10]		22'h0	RSVD	
[9:0]	rw	10'h0	clk_duty	BT_PCM_CLK duty cycle <= (GCLK/(bt_pcm_sync*bt_pcm_dw))
0x250		**0x00000000**	**BT_PCM_SYNC_DUTY**	
[31:6]		26'h0	RSVD	
[5:0]	rw	6'h0	sync_duty	PCM_SYNC duty cycle (bt_pcm_sync frequency = bt_pclk_clk/bt_pcm_sync_duty)
0x260		**0x00000000**	**BT_VOL_CTRL**	
[31:4]		28'h0	RSVD	
[3]	rw	1'h0	vol_adj_en	BT volume adjust enable
[2:0]	rw	3'h0	vol	BT master volume
0x300		**0x00000003**	**INT_MASK**	
[31:2]		30'h0	RSVD	

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表 10-3: I2S 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[1]	rw	1'h1	tx_fifo_int_mask	Interrupt mask for TX FIFO pop underflow, high active
[0]	rw	1'h1	rx_fifo_int_mask	Interrupt mask for RX FIFO push overflow, high active
0x310		**0x00000000**	**INT_STATUS**	
[31:2]		30'h0	RSVD	
[1]	rw	1'h0	tx_fifo_underflow	TX FIFO pop underflow
[0]	rw	1'h0	rx_fifo_overflow	RX FIFO push overflow
0x400		**0x00000000**	**TX_DMA_ENTRY**	
[31:0]	w	32'h0	tx_dma_entry	TX DMA entry
0x440		**0x00000000**	**RX_DMA_ENTRY**	
[31:0]	r	32'h0	rx_dma_entry	RX DMA entry
0x480		**0x00000003**	**DMA_MASK**	
[31:2]		30'h0	RSVD	
[1]	rw	1'h1	tx_dma_mask	TX DMA mask enable:1: mask0: do not mask
[0]	rw	1'h1	rx_dma_mask	RX DMA mask enable:1: mask0: do not mask
0x500		**0x00000000**	**DEBUG_LOOP**	
[31:24]		8'h0	RSVD	
[23:16]	rw	8'h2	sp_clk_div	sp clock divider value
[15:9]		7'h0	RSVD	
[8]	w1c	1'h0	sp_clk_div_update	update sp clock divider
[7:3]		5'h0	RSVD	
[2]	rw	1'h0	sp_clk_sel	clock select 0: xtal clock 1: pll clock
[1]	rw	1'h0	ad2da_loop_back	RX–>TX Loop debug control: 0: disable 1: enable, internally connect RX Resampled PCM to TX Resample PCM input
[0]	rw	1'h0	da2ad_loop_back	TX–>RX Loop debug control: 0: disable 1: enable, internally connect TX SDTO to RX SDTI
0x600		**0x00000000**	**FIFO_STATUS**	
[31:8]		24'h0	RSVD	
[7:0]	rw	8'h0	fifo_status_out	FIFO Status output: Bit [7:0] = tx_full,tx_empty, tx_almost_full, tx_almost_empty, rx_full, rx_empty, rx_almost_full, rx_almost_empty
0x700		**0x00000000**	**TX_EQUALIZER_EN**	
[31:1]		31'h0	RSVD	
[0]	rw	1'h0	tx_equalizer_en	0: Disable TX equalizer 1: Enable TX equalizer equalizer is not implemented
0x710		**0x00000000**	**TX_EQUALIZER_GAIN1**	
[31:30]		2'h0	RSVD	
[29:25]	rw	5'h0	band6_gain	
[24:20]	rw	5'h0	band5_gain	
[19:15]	rw	5'h0	band4_gain	
[14:10]	rw	5'h0	band3_gain	
[9:5]	rw	5'h0	band2_gain	
[4:0]	rw	5'h0	band1_gain	

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表 10-3: I2S 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
0x720		**0x00000000**	**TX_EQUALIZER_GAIN2**	
[31:20]		12'h0	RSVD	
[19:15]	rw	5'h0	band10_gain	
[14:10]	rw	5'h0	band9_gain	
[9:5]	rw	5'h0	band8_gain	
[4:0]	rw	5'h0	band7_gain	

11 加速器

11.1 数字信号处理加速器

11.1.1 Cordic 协处理器

Cordic 协处理器用于计算三角函数和双曲函数及其推演出的一些算术运算。在 HPSYS/LPSYS 中各集成了一个 Cordic 协处理器。

Cordic 协处理器特性如下：

- 支持 ARM coprocessor 协处理器指令
- 支持 ARM Custom Datapath Extention 指令（只有 HPSYS）
- 支持三角函数类运算：cos、sin、ang、mod、atan、rot
- 支持双曲函数类运算 cosh、sinh、atanh、angh、modh、mul、div、ln、exp、sqrt
- 支持 32 位定点输入输出

11.2 CRC

11.2.1 简介

CRC(Cyclic Redundancy Check) 可进行特定位宽，任意生成多项式，任意初始值的 CRC 计算。数据可以通过 CPU 或 DMA 输入，最小输入单元为单字节，没有最长字节数限制。单 HCLK 周期即能够完成单字节输入的计算。数据输入全部完成后即时得到校验结果。支持输入数据高低位倒转和输出数据高低位倒转。支持不同有效位宽的输入数据。

11.2.2 主要特性

- 7/8/16/32 比特 CRC 计算
- 任意自定义多项式
- 任意初始值
- 输入数据支持单字节/双字节/三字节/四字节有效位宽
- 输入数据支持字节/双字节/四字节高低位比特倒转
- 输出数据支持高低位比特倒转
- 计算速度为每 HCLK 周期 1 字节

11.2.3 CRC 配置方法

启动 CRC 计算前，需要预先配置相应寄存器，包括多项式宽度，有效数据位宽，输入输出倒转模式，多项式和初始值等。主流的 CRC 格式配置方法见下表。

表 11-1: CRC 配置方法

CRC 算法	多项式公式	POLYSIZE	POL	INIT	REV_IN	REV_OUT	结果异或值
CRC-7/MMC	x^7+x^3+1	3	0x09	0x00	0	0	0x00
CRC-8	x^8+x^2+x+1	2	0x07	0x00	0	0	0x00
CRC-8/ITU	x^8+x^2+x+1	2	0x07	0x00	0	0	0x55
CRC-8/ROHC	x^8+x^2+x+1	2	0x07	0xFF	1	1	0x00
CRC-8/MAXIM	$x^8+x^5+x^4+1$	2	0x31	0x00	1	1	0x00
CRC-16/IBM	$x^{16}+x^5+x^2+1$	1	0x8005	0x0000	1	1	0x0000
CRC-16/MAXIM	$x^{16}+x^5+x^2+1$	1	0x8005	0x0000	1	1	0xFFFF
CRC-16/USB	$x^{16}+x^5+x^2+1$	1	0x8005	0xFFFF	1	1	0xFFFF
CRC-16/ MODBUS	$x^{16}+x^5+x^2+1$	1	0x8005	0xFFFF	1	1	0x0000
CRC-16/CCITT	$x^{16}+x^{12}+x^5+1$	1	0x1021	0x0000	1	1	0x0000
CRC-16/ CCITT-FALSE	$x^{16}+x^{12}+x^5+1$	1	0x1021	0xFFFF	0	0	0x0000
CRC-16/x5	$x^{16}+x^{12}+x^5+1$	1	0x1021	0xFFFF	1	1	0xFFFF
CRC-16/ XMODEM	$x^{16}+x^{12}+x^5+1$	1	0x1021	0x0000	0	0	0x0000
CRC-16/DNP	$x^{16}+x^{13}+x^{12}+x^{11}+$ $x^{10}+x^8+x^6+x^5+x^2+1$	1	0x3D65	0x0000	1	1	0xFFFF
CRC-32	$x^{32}+x^{26}+x^{23}+x^{22}+x^{16}+$ $x^{12}+x^{11}+x^{10}+x^8+x^7+$ $x^5+x^4+x^2+x+1$	0	0x04C11DB7	0xFFFFFFFF	1	1	0xFFFFFFFF
CRC-32/ MPEG-2	$x^{32}+x^{26}+x^{23}+x^{22}+x^{16}+$ $x^{12}+x^{11}+x^{10}+x^8+x^7+$ $x^5+x^4+x^2+x+1$	0	0x04C11DB7	0xFFFFFFFF	0	0	0x00000000

CRC 模块不进行结果异或运算，需要由软件读出结果后进行后处理。

11.2.4 数据格式

CRC 计算的基本数据单元为字节。向 DR 寄存器写入的数据固定为 4 字节，该数据中哪些字节参与运算由 CR_DATASIZE 指定。下表中灰色格子参与运算。

表 11-2: 参与运算的数据

CR_DATASIZE	DR			
0	BYTE3	BYTE2	BYTE1	BYTE0
1	BYTE3	BYTE2	BYTE1	BYTE0
2	BYTE3	BYTE2	BYTE1	BYTE0
3	BYTE3	BYTE2	BYTE1	BYTE0

可以单独指定每一笔数据参与运算的字节，但应注意改变 CR_DATASIZE 必须在 SR_DONE 为 1 时，否则可能影响当前数据的计算结果。

运算顺序由 BYTE0,BYTE1,BYTE2,BYTE3 依次进行。计算每个字节时，默认按照从最高比特到最低比特的次序进行。如果配置了输入倒转模式，则按照倒转后从最高比特到最低比特的次序进行。下表为配置的示例，可根据内存中的数据格式灵活调整输入格式。

表 11-3: 运算顺序

DATASIZE	REV_IN	DR	倒转后输入	第一拍计算字节	第二拍计算字节	第三拍计算字节	第四拍计算字节
0	0	0x12345678	/	0x78	/	/	/
1	0	0x12345678	/	0x78	0x56	/	/
2	0	0x12345678	/	0x78	0x56	0x34	/
3	0	0x12345678	/	0x78	0x56	0x34	0x12
3	1	0x12345678	0x482C6A1E	0x1E	0x6A	0x2C	0x48
3	2	0x12345678	0x2C481E6A	0x6A	0x1E	0x48	0x2C
3	3	0x12345678	0x1E6A2C48	0x48	0x2C	0x6A	0x1E

11.2.5 计算速率

CRC 每个 HCLK 周期完成一个字节的计算。数据连续输入时，计算花费的时间约为字节数 ×HCLK 周期。

11.2.6 CRC 配置流程

1. 配置 CRC 格式，依需求设置 POL，INIT，CR_POLYSIZE，CR_REV_IN，CR_REV_OUT，CR_DATASIZE。
2. CR_RESET 置 1 初始化 CRC。
3. 由 CPU 或 DMA 向 DR 寄存器连续搬运所需数据。
4. 如果还剩余的数据字节数与 CR_DATASIZE 不匹配，则需首先查询 SR_DONE，为 1 时改变 CR_DATASIZE，并将剩余数据写入 DR 寄存器。
5. 读 DR 寄存器获取计算结果，并根据需求进行软件异或运算，得到最终 CRC 值。

11.2.7 CRC 寄存器

表 11-4: CRC 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00			**DR**	**Data register**
[31:0]	rw	32'hffffffff	DR	Data register bits. This register is used to write new data to the CRC calculator. It holds the previous CRC calculation result when it is read. If the data size is less than 32 bits, the least significant bits are used to write/read the correct value.
0x04			**SR**	**Status register**
[31:2]		30'h0	RSVD	
[1]	r	1'h0	overflow	Overflow when new data arrive while last calculation not done yet
[0]	r	1'h0	done	Done flag. When DR written, done flag will be cleared automatically. The flag will assert after CRC operation of current DR finished.
0x08			**CR**	**Control register**
[31:8]		24'h0	RSVD	
[7]	rw	1'h0	REV_OUT	Reverse output data This bit controls the reversal of the bit order of the output data. 0: Bit order not affected 1: Bit-reversed output format

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表 11-4: CRC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[6:5]	rw	2'h0	REV_IN	Reverse input data These bits control the reversal of the bit order of the input data 00: Bit order not affected 01: Bit reversal done by byte 10: Bit reversal done by half-word 11: Bit reversal done by word
[4:3]	rw	2'h0	POLYSIZE	Polynomial size These bits control the size of the polynomial. 00: 32 bit polynomial 01: 16 bit polynomial 10: 8 bit polynomial 11: 7 bit polynomial
[2:1]	rw	2'h3	DATASIZE	Valid input data size These bits control the valid size of the input data. 00: lower 8-bit 01: lower 16-bit 10: lower 24-bit 11: all 32-bit
[0]	w	1'h0	RESET	This bit is set by software to reset the CRC calculation unit and set the data register to the value stored in the CRC_INIT register. This bit can only be set, it is automatically cleared by hardware
0x10			**INIT**	**Initial CRC value**
[31:0]	rw	32'hffffffff	INIT	Programmable initial CRC value
0x14			**POL**	**CRC polynomial**
[31:0]	rw	32'h04c11db7	POL	Programmable polynomial This register is used to write the coefficients of the polynomial to be used for CRC calculation. If the polynomial size is less than 32 bits, the least significant bits have to be used to program the correct value.

11.3 AES

11.3.1 简介

SF32LB52x 的 AES_ACC 模块主要针对安全领域的专用算法进行加解密的运算加速。对称加密算法包括 AES128、AES192、AES256 和 SM4。模式包括 ECB、CTR 和 CBC。散列算法包括 SHA1、SHA224、SHA256 和 SM3。启动后，AES_ACC 模块调用内部的 DMA 读入原始数据，根据算法将相应的结果通过内部 DMA 写入目标地址，或者存储在模块内部寄存器中。

11.3.2 AES 功能描述

11.3.2.1 对称加密算法

对称加密算法主要包括 AES 和 SM4，其中 AES 根据 Key 的长度不同又分为 AES128、AES192 和 AES256，SM4 则是国密的对称加密算法。强度上密码长度越长则强度越高，同时加解密花费的时间也会更长，SM4 算法花费的时间则是最长。

11.3.2.2 对称加密模式

对称加密模式主要包括 ECB、CTR 和 CBC。

ECB 模式：ECB 模式通过 KEY 直接对明文数据进行加解密，数据按 16byte 为一组，每次加解密都是对整个 16byte 进行操作。优点是每组数据之间相互独立，可以并行计算，支持数据按组的随机读写。缺点是不同组数据若明文相同，则密文也相同，容易被破解。

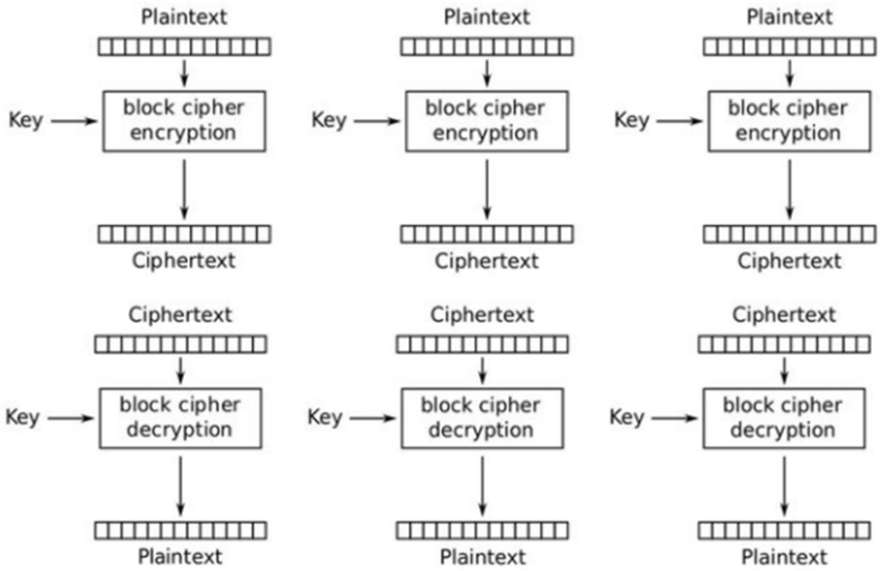

图 11-1: ECB 模式解密

CTR 模式：CTR 模式通过 KEY 对一个由 NONCE 和 COUNTER 组成的向量进行加密，然后用加密后的结果与明文数据进行异或，得到数据密文，实现加密操作。解密时用相同的向量加密后的结果与密文数据进行异或，得到明文数据，实现解密操作。实际使用中，NONCE 通常用常数表示，COUNTER 则会使用数据的地址，这样保证每组数据的向量不同，从而使加解密过程中使用的异或数据也不相同。在了解 CTR 使用的向量组成方式的情

况下，该模式每组数据加解密互相独立，可以并行计算，这一点与 ECB 模式相同。同时该模式只有加密和异或运算，结构也相对简单。加解密时对向量的运算与数据无关，所以该模式常用于外部存储的数据进行加解密。

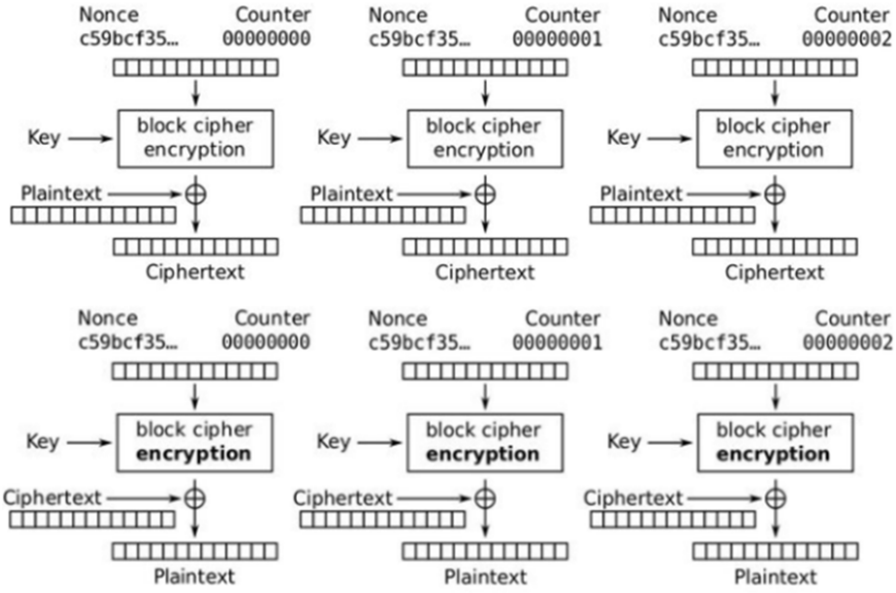

图 11-2: CTR 模式解密

CBC 模式：CBC 模式是将上一组数据的密文，作为初始化向量与当前组异或之后，用 KEY 进行加密生成密文。解密时用 KEY 将密文解密后与上一组的密文进行异或，生成明文。该模式既可以对数据进行加解密也可以将最后一组密文数据作为数据的 MAC 值进行完整性校验，因为该模式加解密过程中，每组数据之间都相互关联，所以安全度更高，但无法做到并行计算，也无法对单独某组数据进行随机读写。

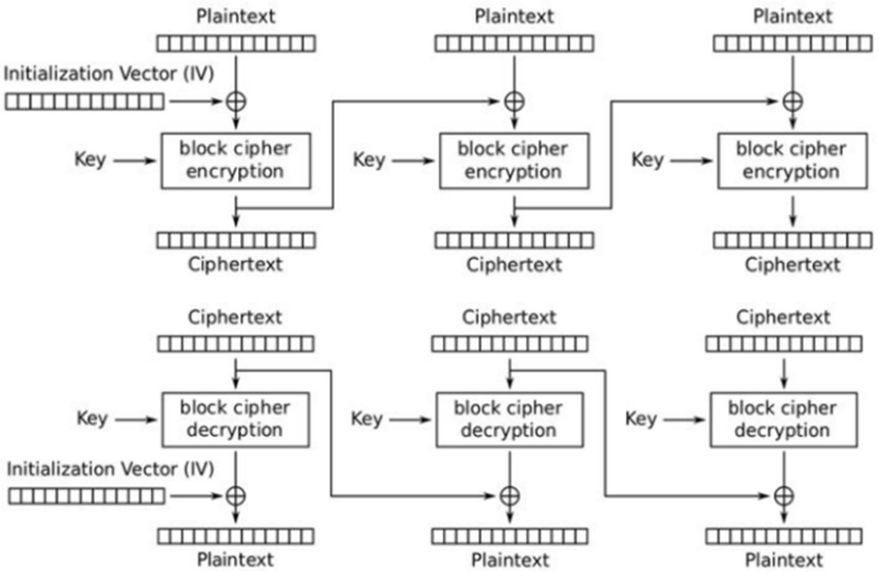

图 11-3: CBC 模式解密

11.3.2.3 对称加解密的多次调用

有时候需要对大量数据进行加解密的操作，但受限制与存储空间或者传输速率的影响，数据会被分为多批次进行处理，当需要多次调用对称加解密模块对一大段数据进行连续处理时就需要考虑到调用之间数据上下文的保存和维护。

ECB 模式：

ECB 模式对于每一组 16byte 数据进行单独的加解密操作的，对于单次加解密的数据，需要保证数据量为 16byte 的整数倍，多余的数据可以等到下一批数据准备好以后合并进行处理。

CTR 模式：

CTR 模式对于每一组 16byte 的数据均有对应的 NONCE 和 COUNTER 值，通常情况下，NONCE 为常数，COUNTER 为当前数据组的编号，数据组编号按每次加 1 递增。对于单次加解密的数据，上层软件调用时需要保证数据量为 16byte 的整数倍，同时根据数据量记录下 COUNTER 值，在下一次调用将累计的 COUNTER 值作为初始向量输入到对应的 IV 寄存器。多余的数据可以等到下一批数据准备好后合并进行处理。

CBC 模式：

CBC 模式的每组数据使用的初始向量均来自上一组数据的密文，对于单次加解密数据，上层软件调用时需要保证数据量为 16byte 的整数倍，同时需要记录下当前加解密操作最后一组数据的密文，在下一次操作时作为初始向量输入到对应的 IV 寄存器中。多余的数据则等到下一批数据准备好之后合并进行处理。

11.3.2.4 散列算法

散列算法包括 SHA1，SHA224，SHA256 和 SM3，不同算法的摘要长度不同。SHA1 摘要为 160bit，SHA224 为 224bit，SHA256 和 SM3 均为 256bit，碰撞性角度来说，摘要越长碰撞概率则会越低。

11.3.2.5 散列值计算的多次调用

有时候需要对大量数据进行散列值计算，但受限于存储空间或者传输速率的影响，数据会被分为多批次进行处理。当需要多次调用散列值计算模块对一大段数据进行处理时，需要注意以下几点。

第一，除最后一次以外，每一次处理的数据量必须为 4byte 的整数倍，单次处理多余的数据需保存，与下一批次的数据进行合并处理。

第二，对于所有散列算法，每一次计算前需要将上一次散列计算的中间结果 H0~H7 写入对应的寄存器，然后设置散列值计算模块使用外部 H0~H7 的初始值并且装载入模块。

第三，每次调用 HASH 时需要将上一次结束时的 HASH LEN RESULT 更新到当前 HASH LEN 寄存器，并且装载入模块。

第四，除最后一次调用以外，需要设置散列值计算模块不使用 padding。

11.3.3 AES 寄存器

表 11-5: AES 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00		**0x0000_0000**	**COMMAND**	
[31:5]		27'h0	RSVD	
[4]	rw	1'h0	AUTO_GATE	auto clock gating
[3]	rw	1'h0	HASH_RESET	HASH_ACC soft reset, 1'h1: reset the HASH_ACC block
[2]	w1t	1'h0	HASH_START	write 1 to trigger the HASH_ACC block
[1]	rw	1'h0	AES_ACC_RESET	AES_ACC soft reset, 1'h1: reset the AES_ACC block
[0]	w1t	1'h0	START	write 1 to trigger the AES_ACC block
0x04		**0x0000_0000**	**STATUS**	
[31:3]		29'h0	RSVD	
[2]	r	1'h0	HASH_BUSY	HASH_ACC block is busy
[1]	r	1'h0	FLASH_KEY_VALID	flash key valid indicator
[0]	r	1'h0	BUSY	AES_ACC block is busy
0x08		**0x0000_0000**	**IRQ**	
[31:22]		10'h0	RSVD	
[21]	rw1c	1'h0	HASH_PAD_ERR_RAW_STAT	HASH_ACC padding error raw status
[20]	rw1c	1'h0	HASH_BUS_ERR_RAW_STAT	HASH_ACC bus error raw status
[19]	rw1c	1'h0	HASH_DONE_RAW_STAT	HASH_ACC done raw status
[18]	rw1c	1'h0	SETUP_ERR_RAW_STAT	AES_ACC setup error raw status
[17]	rw1c	1'h0	BUS_ERR_RAW_STAT	AES_ACC bus error raw status
[16]	rw1c	1'h0	DONE_RAW_STAT	AES_ACC done raw status
[15:6]		10'h0	RSVD	
[5]	rw1c	1'h0	HASH_PAD_ERR_STAT	HASH_ACC padding error status
[4]	rw1c	1'h0	HASH_BUS_ERR_STAT	HASH_ACC bus error status
[3]	rw1c	1'h0	HASH_DONE_STAT	HASH_ACC done status
[2]	rw1c	1'h0	SETUP_ERR_STAT	AES_ACC setup error status
[1]	rw1c	1'h0	BUS_ERR_STAT	AES_ACC bus error status
[0]	rw1c	1'h0	DONE_STAT	AES_ACC done status
0x0C		**0x0000_0000**	**SETTING**	
[31:6]		26'h0	RSVD	
[5]	rw	1'h0	HASH_PAD_ERR_MASK	HASH_ACC padding error interrupt mask, 0: mask the interrupt
[4]	rw	1'h0	HASH_BUS_ERR_MASK	HASH_ACC bus error interrpt mask, 0: mask the interrupt
[3]	rw	1'h0	HASH_DONE_MASK	HASH_ACC done interrupt mask, 0: mask the interrupt
[2]	rw	1'h0	SETUP_ERR_IRQ_MASK	AES_ACC setup error interrupt mask, 0: mask the interrupt
[1]	rw	1'h0	BUS_ERR_IRQ_MASK	AES_ACC bus error interrupt mask, 0: mask the interrupt
[0]	rw	1'h0	DONE_IRQ_MASK	AES_ACC done interrupt mask, 0: mask the interrupt
0x10		**0x0000_0000**	**AES_SETTING**	
[31:9]		23'h0	RSVD	
[8]	rw	1'h0	AES_BYPASS	1'h0: normal operation 1'h1: bypass
[7]	rw	1'h0	AES_OP_MODE	1'h0: decryption 1'h1: encryption
[6]	rw	1'h0	ALGO_STANDARD	1'h0: AES 1'h1: SM4
[5]	rw	1'h0	KEY_SEL	1'h0: select key from AES_ACC key registers 1'h1: use internal root key

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表 11-5: AES 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[4:3]	rw	2'h0	AES_LENGTH	AES Length: 2'h0: 128-bit 2'h1: 192-bit 2'h2: 256-bit 2'h3: Reserved
[2:0]	rw	3'h0	AES_MODE	AES Mode: 3'h0: ECB 3'h1: CTR 3'h2: CBC Others: Reserved
0x14		**0x0000_0000**	**DMA_IN**	
[31:0]	rw	32'h0	ADDR	AES_ACC input data address
0x18		**0x0000_0000**	**DMA_OUT**	
[31:0]	rw	32'h0	ADDR	AES_ACC output data address
0x1C		**0x0000_0000**	**DMA_DATA**	
[31:28]		4'h0	RSVD	
[27:0]	rw	28'h0	SIZE	AES_ACC data block size, AES_ACC only support block aligned transaction. Each block contains 16 bytes.
0x20		**0x0000_0000**	**IV_W0**	
[31:0]	rw	32'h0	DATA	Initial Vector Word0
0x24		**0x0000_0000**	**IV_W1**	
[31:0]	rw	32'h0	DATA	Initial Vector Word1
0x28		**0x0000_0000**	**IV_W2**	
[31:0]	rw	32'h0	DATA	Initial Vector Word2
0x2C		**0x0000_0000**	**IV_W3**	
[31:0]	rw	32'h0	DATA	Initial Vector Word3
0x30		**0x0000_0000**	**EXT_KEY_W0**	
[31:0]	rw	32'h0	DATA	External Key Word0
0x34		**0x0000_0000**	**EXT_KEY_W1**	
[31:0]	rw	32'h0	DATA	External Key Word1
0x38		**0x0000_0000**	**EXT_KEY_W2**	
[31:0]	rw	32'h0	DATA	External Key Word2
0x3c		**0x0000_0000**	**EXT_KEY_W3**	
[31:0]	rw	32'h0	DATA	External Key Word3
0x40		**0x0000_0000**	**EXT_KEY_W4**	
[31:0]	rw	32'h0	DATA	External Key Word4
0x44		**0x0000_0000**	**EXT_KEY_W5**	
[31:0]	rw	32'h0	DATA	External Key Word5
0x48		**0x0000_0000**	**EXT_KEY_W6**	
[31:0]	rw	32'h0	DATA	External Key Word6
0x4C		**0x0000_0000**	**EXT_KEY_W7**	
[31:0]	rw	32'h0	DATA	External Key Word7
0x50		**0x0000_0000**	**HASH_SETTING**	
[31:9]		23'h0	RSVD	
[8]	w1t	1'h0	HASH_LEN_LOAD	write 1 to load hash length
[7]	w1t	1'h0	HASH_IV_LOAD	write 1 to load hash iv

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表 11-5: AES 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[6]	rw	1'h0	RESULT_ENDIAN	hash result endian setting: 1'h0: little endian 1'h1: big endian
[5]	rw	1'h0	DFT_IV_SEL	HASH default iv select. 1'h0: default iv according to hash mode 1'h1: default iv from HASH_IV_H* registers
[4]	rw	1'h0	BYTE_SWAP	HASH byte swap option. Set 1 to swap byte order when read data from memory.
[3]	rw	1'h0	DO_PADDING	HASH padding enable. Set 1 to do padding after data transfer.
[2:0]	rw	3'h0	HASH_MODE	HASH Mode: 3'h0: SHA-1 3'h1: SHA-224 3'h2: SHA-256 3'h3: SM3 Others: Reserved
0x54		**0x0000_0000**	**HASH_DMA_IN**	
[31:0]	rw	32'h0	ADDR	input data address
0x58		**0x0000_0000**	**HASH_DMA_DATA**	
[31:0]	rw	32'h0	SIZE	HASH input data byte size.
0x5C		**0x0000_0000**	**HASH_IV_H0**	
[31:0]	rw	32'h0	DATA	HASH IV H0
0x60		**0x0000_0000**	**HASH_IV_H1**	
[31:0]	rw	32'h0	DATA	HASH IV H1
0x64		**0x0000_0000**	**HASH_IV_H2**	
[31:0]	rw	32'h0	DATA	HASH IV H2
0x68		**0x0000_0000**	**HASH_IV_H3**	
[31:0]	rw	32'h0	DATA	HASH IV H3
0x6C		**0x0000_0000**	**HASH_IV_H4**	
[31:0]	rw	32'h0	DATA	HASH IV H4
0x70		**0x0000_0000**	**HASH_IV_H5**	
[31:0]	rw	32'h0	DATA	HASH IV H5
0x74		**0x0000_0000**	**HASH_IV_H6**	
[31:0]	rw	32'h0	DATA	HASH IV H6
0x78		**0x0000_0000**	**HASH_IV_H7**	
[31:0]	rw	32'h0	DATA	HASH IV H7
0x7C		**0x0000_0000**	**HASH_RESULT_H0**	
[31:0]	r	32'h0	DATA	HASH result H0
0x80		**0x0000_0000**	**HASH_RESULT_H1**	
[31:0]	r	32'h0	DATA	HASH result H1
0x84		**0x0000_0000**	**HASH_RESULT_H2**	
[31:0]	r	32'h0	DATA	HASH result H2
0x88		**0x0000_0000**	**HASH_RESULT_H3**	
[31:0]	r	32'h0	DATA	HASH result H3
0x8C		**0x0000_0000**	**HASH_RESULT_H4**	
[31:0]	r	32'h0	DATA	HASH result H4
0x90		**0x0000_0000**	**HASH_RESULT_H5**	
[31:0]	r	32'h0	DATA	HASH result H5

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表 11-5: AES 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
0x94		**0x0000_0000**	**HASH_RESULT_H6**	
[31:0]	r	32'h0	DATA	HASH result H6
0x98		**0x0000_0000**	**HASH_RESULT_H7**	
[31:0]	r	32'h0	DATA	HASH result H7
0x9C		**0x0000_0000**	**HASH_LEN_L**	
[31:0]	rw	32'h0	DATA	HASH load length l
0xA0		**0x0000_0000**	**HASH_LEN_H**	
[31:29]		3'h0	RSVD	
[28:0]	rw	29'h0	DATA	HASH load length h
0xA4		**0x0000_0000**	**HASH_RESULT_LEN_L**	
[31:0]	r	32'h0	DATA	HASH result length l
0xA8		**0x0000_0000**	**HASH_RESULT_LEN_H**	
[31:29]		3'h0	RSVD	
[28:0]	r	29'h0	DATA	HASH result length h

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