SF32LB56x

用户手册

V0.9（非正式发布）

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更新历史

文档状态说明

文档状态	版本范围	说明
草稿	0.0.0 ~0.9.9	初稿，非正式发布，信息为初步数据，反映量产前产品的规格与性能，不能保证准确性，随时可能更改，思澈科技将不会主动通知
发布版	1.0.0 ~1.9.9	正式发布，信息有可能还会小范围修正，以便更准确地反映量产产品的规格与性能；如有更改，思澈科技将不会主动通知

本文档更新历史

日期	版本	发布说明
2025-01-10	0.9	增加了合封 IO 的描述以及各个 IP 的概述
2024-12-20	0.8	更新 LCDC，EFUSE 等模块
2024-12-06	0.7	更新时钟与复位，低功耗等章节
2023-06-15	0.6	新增定时器级联
2023-06-14	0.5	新增 SPI 章节
2023-02-23	0.4	更新 IO 章节，新增 AON 章节
2023-02-21	0.3	新增 GPADC、AES 章节
2023-02-03	0.2	新增 RCC、IO、I2S、CRC 等章节
2023-01-31	0.1	初稿

产品概述

SF32LB56x 是一系列用于超低功耗人工智能物联网（AIoT）场景下的高集成度、高性能 MCU 芯片。芯片采用了基于 Arm Cortex-M33 STAR-MC1 处理器的大小核架构，集成高性能 2D/2.5D 图形引擎，人工智能神经网络加速器，双模蓝牙 5.3，以及音频 CODEC，可广泛用于腕带类可穿戴电子设备、智能移动终端、智能家居等各种应用场景。

芯片中大核性能处理器最高工作频率达 240MHz，单核性能达 984 CoreMark，用于提供丰富应用和流畅人机交互所需的高性能算力。小核低功耗处理器最高工作频率 96MHz，性能达 394 CoreMark，功耗效率 3.8uA/CoreMark，在作为 Sensor Hub 控制多种传感器的同时兼顾运行蓝牙协议栈，从而很好地兼顾流畅人机交互所需的高计算性能与长待机时间所需的超低功耗运行之间的平衡关系。

芯片内集成 2D/2.5D GPU，主频最高达到 240MHz，支持四图层叠加，alpha 混叠，硬件加速的实时旋转和缩放，以及各种常用图形格式转换。支持硬件加速无损压缩图形解压缩，支持原生动画，可以大幅提高带宽利用率，降低存储成本。芯片内置 LCD 控制器，支持 8080/QSPI/JDI 等多种接口，可不依赖于 CPU 自主实现最高 60fps 的全屏刷新帧率，并支持低功耗息屏常显。

集成世界水平的双模蓝牙 5.3 收发机，经典蓝牙 EDR2 模式最高发射功率 13dBm，接收峰值功耗低至 2.2mA@3.3V，低功耗蓝牙接收灵敏度达到-100dBm（1Mbps），经典蓝牙 EDR2 模式灵敏度-95.5dBm。集成高保真音频 ADC 和 DAC，支持蓝牙通话和连接耳机 MP3 播放。

功能框图

图 0-1: 功能框图

产品特性

CPU 与内存

- 性能处理器/大核（HCPU）
  - 处理器：Arm Cortex-M33 STAR-MC1
  - 主频：最高 240MHz，可调节
  - 最高 370DMIPS，984EEMBC CoreMark
  - I/D-Cache：32KB(2-way)+16KB(4-way)
  - SRAM：800KB （其中 128KB 为 Retention SRAM）
  - CoreMark 功耗效率：<34uA/MHz @3.3V
  - 单精度浮点运算单元（FPU）
  - 内存保护单元（MPU）
- 超低功耗处理器/小核（LCPU）
  - 处理器：Arm Cortex-M33 STAR-MC1
  - 主频：最高 96MHz，可调节
  - 最高 148DMIPS，394 EEMBC CoreMark
  - I/D-Cache：16KB(2-way)+8KB(4-way)
  - SRAM：160KB（全部为 Retention SRAM）
  - CoreMark 功耗效率：<15.5uA/MHz @3.3V
  - 单精度浮点运算单元（FPU）
  - 内存保护单元（MPU）

无线连接

- 双模蓝牙 5.3，支持 BLE Audio
- 灵敏度：-100dBm（BLE/1Mbps），-96.2dBm（BR），-95.5dBm（EDR2），-88.7dBm（EDR3）
- 最大发射功率：13dBm (EDR2/3)，17dBm (BR/BLE)
- 接收机峰值功耗（BR）：2.2mA@3.3V

图形显示

- 2D/2.5D 图形引擎—ePicasso™2.0
  - 支持四图层 alpha 混叠，外加纯色背景图层
  - 支持硬件加速的旋转、缩放和镜像
  - 最大解析度 512×512
  - 支持 aRGB8565，aRGB8888，L8，A8/4，支持 alpha 混叠
- 无损解压缩加速器—eZip™2.0
  - 硬件无损图形解压缩，支持无损动画 eZip-A
  - 支持 aRGB8565，aRGB8888，L8，A8/4 格式
  - 支持与 ePicasso™2.0 联动，无须中间缓存
- LCD 控制器
  - 支持 8080，SPI，Dual-SPI，Quad-SPI，JDI 接口
  - 支持两图层 alpha 混叠，外加纯色背景图层
  - TurboPixel™ 帧缓存压缩与解压缩

音频

- 1× 高保真 24-bit 音频 DAC，108dB SNR
- 1× 高保真 24-bit 音频 ADC，99dB SNR
- 2×PDM 数字麦克风输入
- 1×I^2S
- 音频采样率转换加速器
- 音频 EQ 均衡加速器

神经网络矩阵加速器

- 面向 TinyML 场景，高效率完成矩阵卷积运算
- 最高处理能力达到 1.92GOPS
- 功耗效率高于 10TOPS/W

数字信号处理加速器

- 大核中有一个 FFT 加速器
- 大核中有一个 FIR 滤波器加速器
- 每个处理器各配备一个 CORDIC 三角函数协处理器

存储接口

- 4×MPI，支持 QSPI-NOR、SPI-NAND、QPI/OPI-PSRAM
- 2×SD/SDIO/eMMC，4 线、8 线各一套，支持 SD3.0，SDIO3.0，以及 eMMC4.51

系统时钟

- 振荡器
  - 48MHz 晶体振荡器
  - 低功耗 RC 振荡器：1MHz，48MHz
  - 超低功耗 RC 振荡器：10KHz
  - 超低功耗 32.768KHz 晶体振荡器，可选配
- PLL
  - 专用音频 PLL
  - 3×PLL，最高频率 384MHz，以 24MHz 为单位

安全

- AES 加速器
  - 对称加解密支持 AES128、AES192、AES256，SM3，SM4 算法
  - 加解密模式包括 ECB、CTR、CBC
  - AES 以 DMA 方式，对源数据处理后，写入目标地址
  - 支持外部 Key，也支持 Root Key
  - 支持 NOR Flash 加密数据读取时实时解密
- SHA1、SHA256 硬件加速
- 支持使用 7/8/16/32 位的完全可编程多项式计算 CRC，数据输入支持 8/16/32 位宽度，可由 CPU 或 DMA 驱动进行数据的 CRC 计算
- 真随机数发生器（TRNG）
- 支持安全启动（Secure Boot）
- 内置 1024-bit eFuse，可存储信任根（Root of Trust）和唯一 ID（UID）
- PSA Certified Level 1 认证

其它

- DMA
  - 通用 DMA：用于与外设间高效率数据搬运
  - extDMA：用于与外部存储间高效率数据搬运
- 定时器
  - 5×16b GPTIM，1×32b ATIM，4×32b BTIM，3×24b LPTIM
  - 1×RTC
  - 2× 看门狗 24b WDT，1× 独立看门狗 IWDT
- 模拟
  - 1×12-bit 通用 SAR ADC，共 8 通道
  - 1× 片上温度传感器
  - 2× 低功耗电压比较器
- 连接外设
  - 6×UART，7× I^2C，4×SPI，1×ISO7816
  - 1×USB2.0 FS
  - SIM 卡控制器
  - 外设任务控制器（PTC）
- 电源管理
  - 输入电压：1.7-3.6V，-40 到 85°C
  - 内置高效率 Buck 及低功耗 LDO
  - RTC 工作下的休眠功耗：600nA
  - 管脚唤醒配置时的休眠功耗：300nA

封装

- WBBGA175，120 个 GPIO，6.5×6.1×0.94mm
- QFN68L，44 个 GPIO，7×7×0.75mm

应用场景

智能穿戴

- 高端智能手表
- 智能手环
- 可穿戴医疗器材
- 健身器材

工业

- 高性价比显示方案
- 图形化人机交互设备
- 工业传感器控制中心
- 工业设备监测
- 工业仪器仪表

车载

- 电动车中控设备
- 汽车钥匙
- 穿戴式汽车遥控设备

家庭自动化

- 中小型智能家电
- 智能门锁

通用

- 低功耗传感器中心
- 蓝牙 mesh

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1 芯片总览

1.1 系统架构

SF32LB56x 是一系列用于超低功耗人工智能物联网（AIoT）场景下的高集成度、高性能 MCU 芯片。芯片采用了基于 Arm Cortex-M33 STAR-MC1 处理器的大小核架构，其中：

- 性能处理器/大核（HCPU）：最高主频 240MHz，配备 32KB 指令缓存（I-Cache）和 16KB 数据缓存（D-Cache），800KB SRAM（其中 128KB 为 Retention SRAM）；作为系统主控，能够高效访问片内和片外存储，主要用于系统控制、人机交互、高性能计算等。
- 超低功耗处理器/小核（LCPU）：最高主频 96MHz，配备 16KB 指令缓存（I-Cache）和 8KB 数据缓存（D-Cache），160KB SRAM（全部为 Retention SRAM）；主要作为系统的超低功耗传感器中心（Sensor Hub）和低功耗蓝牙连接的控制器，满足超低功耗场景下的各种数据采集、处理、传输与控制需求。

1.2 Cortex-M33 STAR-MC1 “星辰”处理器

Cortex-M33 STAR-MC1 处理器是安谋中国（Arm China）推出的“星辰”系列产品的第一款处理器，该处理器继承了 Cortex-M33 的主要特点，支持现有的 Armv8-M 架构的全部功能，具有有序（in order）三级流水线，可显著降低系统功耗，具有部分双发射 16 位指令能力，并进一步改进了协处理器接口，增加了对缓存（Cache）的支持。

Cortex-M33 STAR-MC1 性能达到 1.5DMIPS/MHz 和 4.02Coremark/MHz，与上一代同档位 Arm 处理器相比，在相同主频下，Cortex-M33 STAR-MC1 的性能提升 20%。

Cortex-M33 STAR-MC1 提供了协处理器（Coprocessor）接口，以便根据不同场景需求进一步提高定制计算的能力。通过 MCR（Move from Coprocessor to Register）和 MRC（Move from Register to Coprocessor）指令，可以在 Cortex-M33 STAR-MC1 和协处理器之间转移寄存器数据和计算结果数据，非常适合所需数据量不大、计算复杂但相对碎片化、延迟较小的运算。在协处理器计算的同时，Cortex-M33 STAR-MC1 处理器仍然可以并行执行其它指令，从而明显提高执行效率。

此外，该处理器还支持数字信号处理（DSP）指令集和浮点数运算单元（FPU）。

Cortex-M33 STAR-MC1 引入了紧耦合内存（TCM）和缓存（Cache）技术，增强了各种不同特点的内置和外置存储系统的使用灵活性，确保在各种不同场景下处理器响应的实时性和计算效率。

1.3 性能处理器（大核）系统（HPSYS）

1.3.1 总线架构

HPSYS 内部提供了基于 AHB 协议的总线矩阵，支持多个主设备并行访问多个从设备地址空间。

如图1-1所示，总线主设备位于上侧，从设备地址空间位于右侧，交叉处的黑色圆点代表总线连通。

HCPU 能够访问 HPSYS 的所有地址空间，并能通过 HP2LP 跨核访问 LPSYS 的所有地址空间。

DMAC1 能够访问 HPSYS 的所有地址空间，并能通过 HP2LP 跨域访问 LPSYS 的所有地址空间。

LPSYS 的部分主设备能够通过 LP2HP 跨域访问 HPSYS 的地址空间。

HPSYS_ITCM 仅能由 HCPU 和 DMAC1 访问。DTCM 与 HPSYS_RAM0 共享 128KB 地址空间，可由 HCPU 及其它主设备访问。

多个主设备同时访问同一个从设备地址空间时，基于轮询仲裁原则决定访问次序。

图中边框不相连的多个主设备同时访问不同从设备地址空间时，互相不受影响。边框相连的两个主设备同时发起访问时，基于固定优先级或轮询仲裁原则决定访问次序。

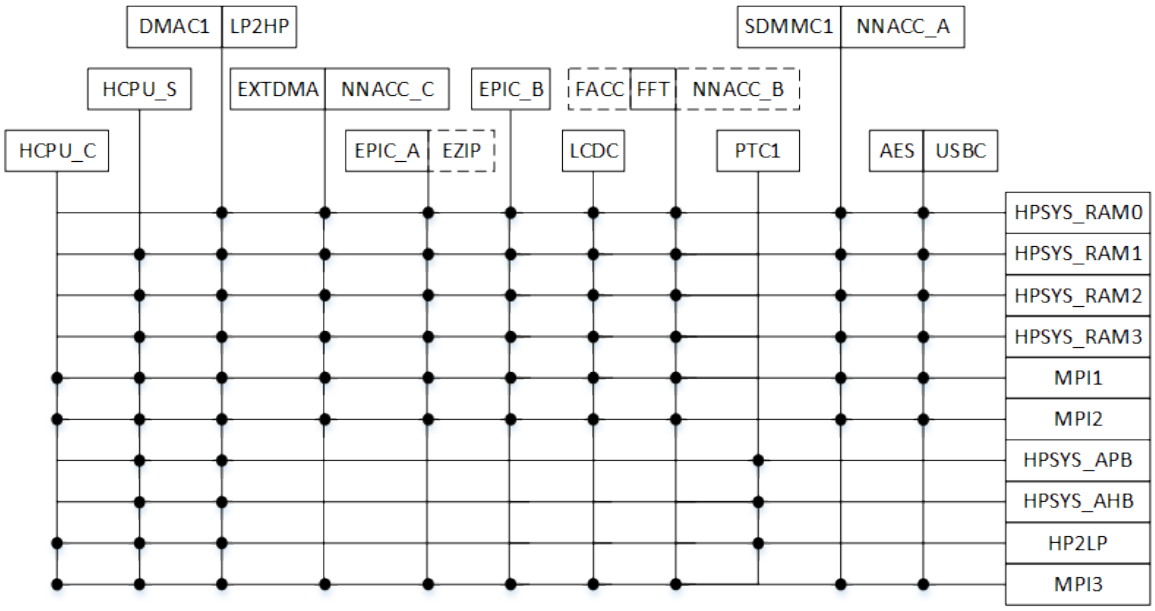

图 1-1: 性能处理器（大核）系统总线架构

1.3.2 存储器类型

1.3.2.1 Cache

HCPU 配置有 32KB 2-way I-Cache（一级指令缓存）和 16KB 4-way D-Cache（一级数据缓存），可大幅提升 XIP 时 CPU 执行效率。软件需合理配置 MPU（Memory Protection Unit）设置 cache 地址段和非 cache 地址段，兼顾效率和易用性。

1.3.2.2 TCM

HCPU 配置有 128KB zero-wait-cycle D-TCM，地址空间为 0x2000_0000-0x2001_FFFF，可用于放置对实时性要求较高的代码和数据。该 TCM memory 也挂在总线上，可以被其他 AHB master 访问。当系统进入低功耗模式时，此 memory 可保持数据。

1.3.2.3 SRAM

HPSYS 总线上共有 800KB SRAM，其中包括：

- 0x2000_0000-0x2001_FFFF，128KB zero-wait-cycle SRAM（与 D-TCM 共享），所有 AHB master 均可访问，最高频率为 240MHz，并具备 retention 功能。
- 0x2002_0000-0x200C_7FFF，672KB SRAM，wait-cycle 为 0 或 1，所有 AHB master 均可访问，最高频率为 240MHz。

1.3.2.4 片外 RAM

HPSYS 支持外挂 OPI DDR pSRAM，地址空间为 0x6000_0000-0x63FF_FFFF，实际可访问地址由外挂颗粒容量决定。接口最高频率为 DDR 168MHz，数据位宽为 8-bit。

1.3.2.5 片外 Flash

HPSYS 支持外挂 NOR/NAND FLASH，其中：

- 0x6000_0000-0x63FF_FFFF 地址段可挂合封 FLASH，推荐使用频率为 96MHz
- 0x6400_0000-0x9FFF_FFFF 地址段可挂外置 FLASH，推荐使用频率为 72MHz

1.3.3 地址映射

表 1-1: HPSYS 地址映射

Category	Memory /IP	Address space	HCPU				LCPU	
			Starting Address		Ending Address		Starting Address	Ending Address
HPSYS_ITCM		**64KB**	**0x0000_0000**		**0x0000_FFFF**		**NA**	**NA**
	ROM	64KB	0x0000_0000		0x0000_FFFF		-	-
	Reserved	-	-		-		-	-
External Memory		**1024MB**	**0x1000_0000**	**0x6000_0000**	**0x1BFF_FFFF**	**0x9FFF_FFFF**	**0x6000_0000**	**0x9FFF_FFFF**
	MPI1 Memory	4MB	0x1000_0000	0x6000_0000	0x103F_FFFF	0x603F_FFFF	0x6000_0000	0x603F_FFFF
	MPI2 Memory	60MB	0x1040_0000	0x6040_0000	0x13FF_FFFF	0x63FF_FFFF	0x6040_0000	0x63FF_FFFF
	MPI3 Memory	128MB/960MB	0x1400_0000	0x6400_0000	0x1BFF_FFFF	0x9FFF_FFFF	0x6400_0000	0x9FFF_FFFF
HPSYS_RAM		**800KB**	**0x2000_0000**		**0x200C_7FFF**		**0x2A00_0000**	**0x2A0C_7FFF**
	RAM0 (Retention)	128KB	0x2000_0000		0x2001_FFFF		0x2A00_0000	0x2A01_FFFF
	RAM1	128KB	0x2002_0000		0x2003_FFFF		0x2A02_0000	0x2A03_FFFF
	RAM2	256KB	0x2004_0000		0x2007_FFFF		0x2A04_0000	0x2A07_FFFF
	RAM3	288KB	0x2008_0000		0x200C_7FFF		0x2A08_0000	0x2A0C_7FFF
HPSYS_APB1		**256KB**	**0x4000_0000**		**0x4003_FFFF**		**0x4000_0000**	**0x4003_FFFF**
	RCC1	4KB	0x4000_0000		0x4000_0FFF		0x4000_0000	0x4000_0FFF
	DMAC1	4KB	0x4000_1000		0x4000_1FFF		0x4000_1000	0x4000_1FFF
	MAILBOX1	4KB	0x4000_2000		0x4000_2FFF		0x4000_2000	0x4000_2FFF
	PINMUX1	4KB	0x4000_3000		0x4000_3FFF		0x4000_3000	0x4000_3FFF
	USART1	4KB	0x4000_4000		0x4000_4FFF		0x4000_4000	0x4000_4FFF
	USART2	4KB	0x4000_5000		0x4000_5FFF		0x4000_5000	0x4000_5FFF
	EZIP1	4KB	0x4000_6000		0x4000_6FFF		0x4000_6000	0x4000_6FFF
	EPIC	4KB	0x4000_7000		0x4000_7FFF		0x4000_7000	0x4000_7FFF
	LCDC1	4KB	0x4000_8000		0x4000_8FFF		0x4000_8000	0x4000_8FFF
	I2S1	4KB	0x4000_9000		0x4000_9FFF		0x4000_9000	0x4000_9FFF
	Reserved	4KB	0x4000_A000		0x4000_AFFF		0x4000_A000	0x4000_AFFF
	SYSCFG1	4KB	0x4000_B000		0x4000_BFFF		0x4000_B000	0x4000_BFFF
	EFUSEC	4KB	0x4000_C000		0x4000_CFFF		0x4000_C000	0x4000_CFFF
	AES	4KB	0x4000_D000		0x4000_DFFF		0x4000_D000	0x4000_DFFF
	Reserved	4KB	0x4000_E000		0x4000_EFFF		0x4000_E000	0x4000_EFFF
	TRNG	4KB	0x4000_F000		0x4000_FFFF		0x4000_F000	0x4000_FFFF

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表 1-1 HPSYS 地址映射（续）

Category	Memory /IP	Address space	HCPU		LCPU	
			Starting Address	Ending Address	Starting Address	Ending Address
	GPTIM1	4KB	0x4001_0000	0x4001_0FFF	0x4001_0000	0x4001_0FFF
	GPTIM2	4KB	0x4001_1000	0x4001_1FFF	0x4001_1000	0x4001_1FFF
	BTIM1	4KB	0x4001_2000	0x4001_2FFF	0x4001_2000	0x4001_2FFF
	BTIM2	4KB	0x4001_3000	0x4001_3FFF	0x4001_3000	0x4001_3FFF
	WDT1	4KB	0x4001_4000	0x4001_4FFF	0x4001_4000	0x4001_4FFF
	SPI1	4KB	0x4001_5000	0x4001_5FFF	0x4001_5000	0x4001_5FFF
	SPI2	4KB	0x4001_6000	0x4001_6FFF	0x4001_6000	0x4001_6FFF
	EXTDMA	4KB	0x4001_7000	0x4001_7FFF	0x4001_7000	0x4001_7FFF
	Reserved	4KB	0x4001_8000	0x4001_8FFF	0x4001_8000	0x4001_8FFF
	NNACC1	4KB	0x4001_9000	0x4001_9FFF	0x4001_9000	0x4001_9FFF
	PDM1	4KB	0x4001_A000	0x4001_AFFF	0x4001_A000	0x4001_AFFF
	PDM2	4KB	0x4001_B000	0x4001_BFFF	0x4001_B000	0x4001_BFFF
	I2C1	4KB	0x4001_C000	0x4001_CFFF	0x4001_C000	0x4001_CFFF
	I2C2	4KB	0x4001_D000	0x4001_DFFF	0x4001_D000	0x4001_DFFF
	Reserved	4KB	0x4001_E000	0x4001_EFFF	0x4001_E000	0x4001_EFFF
	Reserved	4KB	0x4001_F000	0x4001_FFFF	0x4001_F000	0x4001_FFFF
	PTC1	4KB	0x4002_0000	0x4002_0FFF	0x4002_0000	0x4002_0FFF
	BUSMON1	4KB	0x4002_1000	0x4002_1FFF	0x4002_1000	0x4002_1FFF
	I2C3	4KB	0x4002_2000	0x4002_2FFF	0x4002_2000	0x4002_2FFF
	ATIM1	4KB	0x4002_3000	0x4002_3FFF	0x4002_3000	0x4002_3FFF
	Reserved	4KB	0x4002_4000	0x4002_4FFF	0x4002_4000	0x4002_4FFF
	AUDPRC	4KB	0x4002_5000	0x4002_5FFF	0x4002_5000	0x4002_5FFF
	AUDCODEC	4KB	0x4002_6000	0x4002_6FFF	0x4002_6000	0x4002_6FFF
	FFT1	4KB	0x4002_7000	0x4002_7FFF	0x4002_7000	0x4002_7FFF
	FACC1	4KB	0x4002_8000	0x4002_8FFF	0x4002_8000	0x4002_8FFF
	USART3	4KB	0x4002_9000	0x4002_9FFF	0x4002_9000	0x4002_9FFF
	Reserved	4KB	0x4002_A000	0x4002_AFFF	0x4002_A000	0x4002_AFFF
	CAN1	4KB	0x4002_B000	0x4002_BFFF	0x4002_B000	0x4002_BFFF
	Reserved	4KB	0x4002_C000	0x4002_CFFF	0x4002_C000	0x4002_CFFF
	SCI	4KB	0x4002_D000	0x4002_DFFF	0x4002_D000	0x4002_DFFF
	Reserved	4KB	0x4002_E000	0x4002_EFFF	0x4002_E000	0x4002_EFFF
	I2C4	4KB	0x4002_F000	0x4002_FFFF	0x4002_E000	0x4002_FFFF
	Reserved	64KB	0x4003_0000	0x4003_FFFF	0x4003_0000	0x4003_FFFF
HPSYS_APB2		**256KB**	**0x4004_0000**	**0x4007_FFFF**	**0x4004_0000**	**0x4007_FFFF**
	HPSYS_AON	4KB	0x4004_0000	0x4004_0FFF	0x4004_0000	0x4004_0FFF
	LPTIM1	4KB	0x4004_1000	0x4004_1FFF	0x4004_1000	0x4004_1FFF
	Reserved	4KB	0x4004_2000	0x4004_2FFF	0x4004_2000	0x4004_2FFF
	Reserved	52KB	0x4004_3000	0x4004_FFFF	0x4004_3000	0x4004_FFFF
	Reserved	64KB	0x4005_0000	0x4005_FFFF	0x4005_0000	0x4005_FFFF
	Reserved	64KB	0x4006_0000	0x4006_FFFF	0x4006_0000	0x4006_FFFF
	Reserved	64KB	0x4007_0000	0x4007_FFFF	0x4007_0000	0x4007_FFFF
HPSYS_AHB		**256KB**	**0x4008_0000**	**0x400B_FFFF**	**0x4008_0000**	**0x400B_FFFF**
	GPIO1	4KB	0x4008_0000	0x4008_0FFF	0x4008_0000	0x4008_0FFF
	MPI1	4KB	0x4008_1000	0x4008_1FFF	0x4008_1000	0x4008_1FFF
	MPI2	4KB	0x4008_2000	0x4008_2FFF	0x4008_2000	0x4008_2FFF
	MPI3	4KB	0x4008_3000	0x4008_3FFF	0x4008_3000	0x4008_3FFF
	Reserved	4KB	0x4008_4000	0x4008_4FFF	0x4008_4000	0x4008_4FFF
	SDMMC1	4KB	0x4008_5000	0x4008_5FFF	0x4008_5000	0x4008_5FFF
	SDMMC2	4KB	0x4008_6000	0x4008_6FFF	0x4008_6000	0x4008_6FFF
	USBC	4KB	0x4008_7000	0x4008_7FFF	0x4008_7000	0x4008_7FFF
	CRC1	4KB	0x4008_8000	0x4008_8FFF	0x4008_8000	0x4008_8FFF
	Reserved	28KB	0x4008_9000	0x4008_FFFF	0x4008_9000	0x4008_FFFF
	GFX_RAM	64KB	0x4009_0000	0x4009_FFFF	0x4009_0000	0x4009_FFFF
	Reserved	128KB	0x400A_0000	0x400B_FFFF	0x400A_0000	0x400B_FFFF

1.3.4 中断列表

表 1-2: HCPU 中断列表

IRQ #	IRQ Source	IRQ #	IRQ Source	IRQ #	IRQ Source	IRQ #	IRQ Source
NMI	WDT1	IRQ[25]	LCPU_IRQ[25]	IRQ[51]	DMAC1_CH2	IRQ[77]	EXTDMA
IRQ[0]	AON	IRQ[26]	LCPU_IRQ[26]	IRQ[52]	DMAC1_CH3	IRQ[78]	I2C4
IRQ[1]	LCPU_IRQ[1]	IRQ[27]	LCPU_IRQ[27]	IRQ[53]	DMAC1_CH4	IRQ[79]	SDMMC1
IRQ[2]	LCPU_IRQ[2]	IRQ[28]	LCPU_IRQ[28]	IRQ[54]	DMAC1_CH5	IRQ[80]	SDMMC2
IRQ[3]	LCPU_IRQ[3]	IRQ[29]	LCPU_IRQ[29]	IRQ[55]	DMAC1_CH6	IRQ[81]	NNACC1
IRQ[4]	LCPU_IRQ[4]	IRQ[30]	LCPU_IRQ[30]	IRQ[56]	DMAC1_CH7	IRQ[82]	PDM1
IRQ[5]	LCPU_IRQ[5]	IRQ[31]	LCPU_IRQ[31]	IRQ[57]	DMAC1_CH8	IRQ[83]	CAN1
IRQ[6]	LCPU_IRQ[6]	IRQ[32]	LCPU_IRQ[32]	IRQ[58]	LCPU2HCPU	IRQ[84]	GPIO1
IRQ[7]	LCPU_IRQ[7]	IRQ[33]	LCPU_IRQ[33]	IRQ[59]	UART1	IRQ[85]	MPI1
IRQ[8]	LCPU_IRQ[8]	IRQ[34]	LCPU_IRQ[34]	IRQ[60]	SPI1	IRQ[86]	MPI2
IRQ[9]	LCPU_IRQ[9]	IRQ[35]	LCPU_IRQ[35]	IRQ[61]	I2C1	IRQ[87]	MPI3
IRQ[10]	LCPU_IRQ[10]	IRQ[36]	LCPU_IRQ[36]	IRQ[62]	EPIC	IRQ[88]	FFT1
IRQ[11]	LCPU_IRQ[11]	IRQ[37]	LCPU_IRQ[37]	IRQ[63]	LCDC1	IRQ[89]	EZIP1
IRQ[12]	LCPU_IRQ[12]	IRQ[38]	LCPU_IRQ[38]	IRQ[64]	I2S1	IRQ[90]	AUDPRC
IRQ[13]	LCPU_IRQ[13]	IRQ[39]	LCPU_IRQ[39]	IRQ[65]	rsvd	IRQ[91]	PDM2
IRQ[14]	LCPU_IRQ[14]	IRQ[40]	LCPU_IRQ[40]	IRQ[66]	EFUSEC	IRQ[92]	USBC
IRQ[15]	LCPU_IRQ[15]	IRQ[41]	LCPU_IRQ[41]	IRQ[67]	AES	IRQ[93]	I2C3
IRQ[16]	LCPU_IRQ[16]	IRQ[42]	LCPU_IRQ[42]	IRQ[68]	PTC1	IRQ[94]	ATIM1
IRQ[17]	LCPU_IRQ[17]	IRQ[43]	LCPU_IRQ[43]	IRQ[69]	TRNG	IRQ[95]	UART3
IRQ[18]	LCPU_IRQ[18]	IRQ[44]	LCPU_IRQ[44]	IRQ[70]	GPTIM1	IRQ[96]	AUD_HP
IRQ[19]	LCPU_IRQ[19]	IRQ[45]	LCPU_IRQ[45]	IRQ[71]	GPTIM2	IRQ[97]	SCI
IRQ[20]	LCPU_IRQ[20]	IRQ[46]	LPTIM1	IRQ[72]	BTIM1	IRQ[98]	FACC1
IRQ[21]	LCPU_IRQ[21]	IRQ[47]	rsvd	IRQ[73]	BTIM2	IRQ[99]	rsvd
IRQ[22]	LCPU_IRQ[22]	IRQ[48]	rsvd	IRQ[74]	UART2	\	\
IRQ[23]	LCPU_IRQ[23]	IRQ[49]	RTC	IRQ[75]	SPI2	\	\
IRQ[24]	LCPU_IRQ[24]	IRQ[50]	DMAC1_CH1	IRQ[76]	I2C2	\	\

1.4 低功耗处理器（小核）系统（LPSYS）

1.4.1 总线架构

LPSYS 内部提供了基于 AHB 协议的总线矩阵，支持多个主设备并行访问多个从设备地址空间。

如图1-2所示，总线主设备位于上侧，从设备地址空间位于右侧，交叉处的黑色圆点代表总线连通。

LCPU 与 DMAC2 能够访问 LPSYS 的所有地址空间，并能通过 LP2HP 跨域访问除 HPSYS_ITCM 以外 HPSYS 的所有地址空间。

HPSYS 的部分主设备能够通过 HP2LP 跨域访问 LPSYS 的所有地址空间。

LPSYS_ITCM 与 LPSYS_DTCM 能够被 LCPU 和 DMAC2 访问，也能够被 HPSYS 的部分主设备跨域访问。

多个主设备同时访问同一个从设备地址空间时，基于轮询仲裁原则决定访问次序。

图中边框不相连的多个主设备同时访问不同从设备地址空间时，互相不受影响。边框相连的多个主设备同时发起访问时，基于固定优先级或轮询仲裁原则决定访问次序。

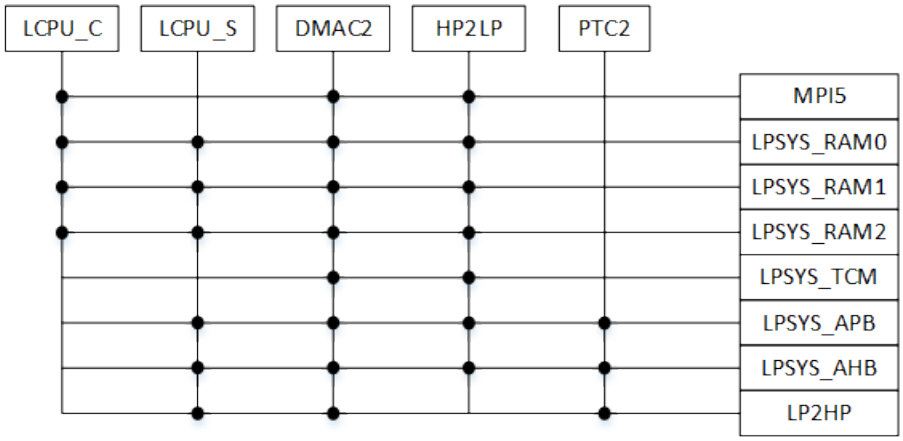

图 1-2: 低功耗处理器（小核）系统总线架构

1.4.2 存储器类型

1.4.2.1 Cache

LCPU 配置有 16KB 2-way I-Cache（一级指令缓存）和 8KB 4-way D-Cache（一级数据缓存）。

1.4.2.2 TCM

LCPU 配置有 16KB zero-wait-cycle I-TCM，地址空间为 0x003F_C000 -0x003F_FFFF。该 TCM memory 为 LCPU 专用，HCPU 可通过地址段 0x20BF_C000 -0x20BF_FFFF 对其进行初始化。建议放置对实时性（或者时延确定性）要求较高的代码和数据。

LCPU 同时配置有 16KB zero-wait-cycle D-TCM，地址空间为 0x203F_C000 -0x203F_FFFF。该 TCM memory 为 LCPU 专用，HCPU 可通过相同地址空间对其进行初始化。

1.4.2.3 SRAM

LPSYS 总线上共有 128KB SRAM，wait-cycle 为 0 或 1，地址空间为 0x2040_0000-0x2041_FFFF。0.9V 时最高频率为 48MHz，1.1V 时最高频率为 96M。

1.4.2.4 片外 Flash

LPSYS 默认外挂 NOR FLASH 用于系统启动，地址空间为 0x1C00_0000 -0x1FFF_FFFF。

1.4.3 地址映射

表 1-3: LPSYS 地址映射

Category	Memory /IP	Address space	HCPU		LCPU	
			Starting Address	Ending Address	Starting Address	Ending Address
LPSYS_ITCM		**4MB**	**0x2080_0000**	**0x20BF_FFFF**	**0x0000_0000**	**0x003F_FFFF**
	ROM	384KB	0x2080_0000	0x2085_FFFF	0x0000_0000	0x0005_FFFF
	Reserved	-	-	-	-	-
	RAM	16KB	0x20BF_C000	0x20BF_FFFF	0x003F_C000	0x003F_FFFF
LPSYS_DTCM		**4MB**	**0x2000_0000**	**0x203F_FFFF**	**0x2000_0000**	**0x203F_FFFF**
	Reserved	-	-	-	-	-
	RAM	16KB	0x203F_C000	0x203F_FFFF	0x203F_C000	0x203F_FFFF
External Memory		**64MB**	**0x1C00_0000**	**0x1FFF_FFFF**	**0x1C00_0000**	**0x1FFF_FFFF**
	MPI5 Memory	64MB	0x1C00_0000	0x1FFF_FFFF	0x1C00_0000	0x1FFF_FFFF

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表 1-3 LPSYS 地址映射（续）

Category	Memory /IP	Address space	HCPU				LCPU			
			Starting Address		Ending Address		Starting Address		Ending Address	
LPSYS_RAM		**128KB**	**0x20C0_0000**	**0x2040_0000**	**0x20C1_FFFF**	**0x2041_FFFF**	**0x0040_0000**	**0x2040_0000**	**0x0041_FFFF**	**0x2041_FFFF**
	RAM0	64KB	0x20C0_0000	0x2040_0000	0x20C0_FFFF	0x2040_FFFF	0x0040_0000	0x2040_0000	0x0040_FFFF	0x2040_FFFF
	RAM1	32KB	0x20C1_0000	0x2041_0000	0x20C1_7FFF	0x2041_7FFF	0x0041_0000	0x2041_0000	0x0041_7FFF	0x2041_7FFF
	RAM2 (EM)	32KB	0x20C1_8000	0x2041_8000	0x20C1_FFFF	0x2041_FFFF	0x0041_8000	0x2041_8000	0x0041_FFFF	0x2041_FFFF
LPSYS_APB1		**192KB**	**0x5000_0000**		**0x5003_FFFF**		**0x5000_0000**		**0x5003_FFFF**	
	RCC2	4KB	0x5000_0000		0x5000_0FFF		0x5000_0000		0x5000_0FFF	
	DMAC2	4KB	0x5000_1000		0x5000_1FFF		0x5000_1000		0x5000_1FFF	
	MAILBOX2	4KB	0x5000_2000		0x5000_2FFF		0x5000_2000		0x5000_2FFF	
	PINMUX2	4KB	0x5000_3000		0x5000_3FFF		0x5000_3000		0x5000_3FFF	
	PATCH	4KB	0x5000_4000		0x5000_4FFF		0x5000_4000		0x5000_4FFF	
	USART4	4KB	0x5000_5000		0x5000_5FFF		0x5000_5000		0x5000_5FFF	
	USART5	4KB	0x5000_6000		0x5000_6FFF		0x5000_6000		0x5000_6FFF	
	USART6	4KB	0x5000_7000		0x5000_7FFF		0x5000_7000		0x5000_7FFF	
	Reserved	4KB	0x5000_8000		0x5000_8FFF		0x5000_8000		0x5000_8FFF	
	SPI3	4KB	0x5000_9000		0x5000_9FFF		0x5000_9000		0x5000_9FFF	
	SPI4	4KB	0x5000_A000		0x5000_AFFF		0x5000_A000		0x5000_AFFF	
	WDT2	4KB	0x5000_B000		0x5000_BFFF		0x5000_B000		0x5000_BFFF	
	I2C5	4KB	0x5000_C000		0x5000_CFFF		0x5000_C000		0x5000_CFFF	
	I2C6	4KB	0x5000_D000		0x5000_DFFF		0x5000_D000		0x5000_DFFF	
	I2C7	4KB	0x5000_E000		0x5000_EFFF		0x5000_E000		0x5000_EFFF	
	SYSCFG2	4KB	0x5000_F000		0x5000_FFFF		0x5000_F000		0x5000_FFFF	
	GPTIM3	4KB	0x5001_0000		0x5001_0FFF		0x5001_0000		0x5001_0FFF	
	GPTIM4	4KB	0x5001_1000		0x5001_1FFF		0x5001_1000		0x5001_1FFF	
	GPTIM5	4KB	0x5001_2000		0x5001_2FFF		0x5001_2000		0x5001_2FFF	
	BTIM3	4KB	0x5001_3000		0x5001_3FFF		0x5001_3000		0x5001_3FFF	
	BTIM4	4KB	0x5001_4000		0x5001_4FFF		0x5001_4000		0x5001_4FFF	
	Reserved	4KB	0x5001_5000		0x5001_5FFF		0x5001_5000		0x5001_5FFF	
	GPADC	4KB	0x5001_6000		0x5001_6FFF		0x5001_6000		0x5001_6FFF	
	Reserved	4KB	0x5001_7000		0x5001_7FFF		0x5001_7000		0x5001_7FFF	
	AUDADC	4KB	0x5001_8000		0x5001_8FFF		0x5001_8000		0x5001_8FFF	
	LPCOMP	4KB	0x5001_9000		0x5001_9FFF		0x5001_9000		0x5001_9FFF	
	TSEN	4KB	0x5001_A000		0x5001_AFFF		0x5001_A000		0x5001_AFFF	
	PTC2	4KB	0x5001_B000		0x5001_BFFF		0x5001_B000		0x5001_BFFF	
	Reserved	4KB	0x5001_C000		0x5001_CFFF		0x5001_C000		0x5001_CFFF	
	BUSMON2	4KB	0x5001_D000		0x5001_DFFF		0x5001_D000		0x5001_DFFF	
	Reserved	4KB	0x5001_E000		0x5001_EFFF		0x5001_E000		0x5001_EFFF	
	Reserved	4KB	0x5001_F000		0x5001_FFFF		0x5001_F000		0x5001_FFFF	
	Reserved	64KB	0x5002_0000		0x5002_FFFF		0x5002_0000		0x5002_FFFF	
	Reserved	64KB	0x5003_0000		0x5003_FFFF		0x5003_0000		0x5003_FFFF	
LPSYS_APB2		**64KB**	**0x5004_0000**		**0x5007_FFFF**		**0x5004_0000**		**0x5007_FFFF**	
	LPSYS_AON	4KB	0x5004_0000		0x5004_0FFF		0x5004_0000		0x5004_0FFF	
	LPTIM2	4KB	0x5004_1000		0x5004_1FFF		0x5004_1000		0x5004_1FFF	
	LPTIM3	4KB	0x5004_2000		0x5004_2FFF		0x5004_2000		0x5004_2FFF	
	Reserved	4KB	0x5004_3000		0x5004_3FFF		0x5004_3000		0x5004_3FFF	
	Reserved	24KB	0x5004_4000		0x5004_9FFF		0x5004_4000		0x5004_9FFF	
	PMUC	4KB	0x5004_A000		0x5004_AFFF		0x5004_A000		0x5004_AFFF	
	RTC	4KB	0x5004_B000		0x5004_BFFF		0x5004_B000		0x5004_BFFF	
	IWDT	4KB	0x5004_C000		0x5004_CFFF		0x5004_C000		0x5004_CFFF	
	Reserved	12KB	0x5004_D000		0x5004_FFFF		0x5004_D000		0x5004_FFFF	
	Reserved	64KB	0x5005_0000		0x5005_FFFF		0x5005_0000		0x5005_FFFF	
	Reserved	64KB	0x5006_0000		0x5006_FFFF		0x5006_0000		0x5006_FFFF	
	EUROPA	4KB	0x5007_0000		0x5007_0FFF		0x5007_0000		0x5007_0FFF	
	Reserved	60KB	0x5007_1000		0x5007_FFFF		0x5007_1000		0x5007_FFFF	
LPSYS_AHB		**256KB**	**0x5008_0000**		**0x500B_FFFF**		**0x5008_0000**		**0x500B_FFFF**	
	GPIO2	4KB	0x5008_0000		0x5008_0FFF		0x5008_0000		0x5008_0FFF	
	MPI5	4KB	0x5008_1000		0x5008_1FFF		0x5008_1000		0x5008_1FFF	
	RFC	8KB	0x5008_2000		0x5008_3FFF		0x5008_2000		0x5008_3FFF	
	PHY	4KB	0x5008_4000		0x5008_4FFF		0x5008_4000		0x5008_4FFF	
	CRC2	4KB	0x5008_5000		0x5008_5FFF		0x5008_5000		0x5008_5FFF	
	Reserved	40KB	0x5008_6000		0x5008_FFFF		0x5008_6000		0x5008_FFFF	
	MAC	64KB	0x5009_0000		0x5009_FFFF		0x5009_0000		0x5009_FFFF	
	Reserved	128KB	0x500A_0000		0x500B_FFFF		0x500A_0000		0x500B_FFFF	
PHY_DUMP		**64KB**	**0x500C_0000**		**0x500C_FFFF**		**0x500C_0000**		**0x500C_FFFF**	
	PHY_DUMP	64KB	0x500C_0000		0x500C_FFFF		0x500C_0000		0x500C_FFFF	

1.4.4 中断列表

表 1-4: LCPU 中断列表

IRQ #	IRQ Source	IRQ #	IRQ Source	IRQ #	IRQ Source	IRQ #	IRQ Source
NMI	**WDT2**	IRQ[12]	**UART4**	IRQ[25]	**BTIM3**	IRQ[38]	**FFT2**
IRQ[0]	**AON**	IRQ[13]	**UART5**	IRQ[26]	**BTIM4**	IRQ[39]	**rsvd**
IRQ[1]	**BLE**	IRQ[14]	**UART6**	IRQ[27]	**AUD_LP**	IRQ[40]	**rsvd**
IRQ[2]	**DMAC2_CH1**	IRQ[15]	**BT**	IRQ[28]	**GPADC**	IRQ[41]	**LPCOMP**
IRQ[3]	**DMAC2_CH2**	IRQ[16]	**SPI3**	IRQ[29]	**rsvd**	IRQ[42]	**LPTIM2**
IRQ[4]	**DMAC2_CH3**	IRQ[17]	**SPI4**	IRQ[30]	**HPSYS0**	IRQ[43]	**LPTIM3**
IRQ[5]	**DMAC2_CH4**	IRQ[18]	**I2S3**	IRQ[31]	**HPSYS1**	IRQ[44]	**HPSYS2**
IRQ[6]	**DMAC2_CH5**	IRQ[19]	**I2C5**	IRQ[32]	**TSEN**	IRQ[45]	**HPSYS3**
IRQ[7]	**DMAC2_CH6**	IRQ[20]	**I2C6**	IRQ[33]	**PTC2**	IRQ[46]	**HCPU2LCPU**
IRQ[8]	**DMAC2_CH7**	IRQ[21]	**I2C7**	IRQ[34]	**rsvd**	IRQ[47]	**RTC**
IRQ[9]	**DMAC2_CH8**	IRQ[22]	**GPTIM3**	IRQ[35]	**GPIO2**	\	\
IRQ[10]	**PATCH**	IRQ[23]	**GPTIM4**	IRQ[36]	**MPI5**	\	\
IRQ[11]	**DM**	IRQ[24]	**GPTIM5**	IRQ[37]	**rsvd**	\	\

1.5 总线访问权限

表 1-5: 总线访问权限

	AHB 从设备							
AHB 主控	HP_ITCM	HP_RAM 0~3	MPI1~3	HP_AHB HP_APB	LP_DTCM LP_ITCM	LP_RAM 0~2	MPI5	LP_AHB LP_APB
HCPU	√	√	√(1)	√	√(2)	√(3)	√	√
DMAC1	√(6)	√	√	√	√(2)	√(3)	√	√
EXTDMA	x	√	√	x	x	x	x	x
AES	x	√	√	x	x	x	x	x
LCDC1	x	√	√	x	x	x	x	x
EZIP	x	√	√	x	x	x	x	x
EPIC	x	√	√	x	x	x	x	x
USBC	x	√	√	x	x	x	x	x
NNACC1	x	√	√	x	x	x	x	x
SDMMC1	x	√	√	x	x	x	x	x
FACC1	x	√	√	x	x	x	x	x
FFT1	x	√	√	x	x	x	x	x
PTC1	x	x	x	√	x	x	x	√
LCPU	√(6)	√(4)	√	√	√	√(5)	√	√
DMAC2	√(6)	√(4)	√	√	√	√	√	√
PTC2	x	√(4)	x	√	x	x	x	√

* (1)HCPU 既可以通过 0x10000000 起始地址访问 MPI 内容，也可以通过 0x60000000 起始地址访问 MPI 内容。
(2)HPSYS 的主控访问 LPSYS 的 ITCM，起始地址是 0x20800000，与 LCPU 访问的地址不同。
(3)HPSYS 的主控访问 LPSYS 的 SRAM，起始地址既可以从 0x20400000 开始，也可以从 0x20C00000 开始。
(4)LPSYS 的主控访问 HPSYS 的 SRAM，起始地址从 0x2a000000 开始，也就是说增加了 0x0a000000 的偏移。
(5)LCPU 访问 LPSYS 的 SRAM，起始地址既可以从 0x00400000 开始，也可以从 0x20400000 开始。
(6) 其它主控访问 HCPU 的 ROM，起始地址从 0xa0000000 开始，也就是说增加了 0xa0000000 的偏移。

2 时钟与复位

2.1 简介

时钟与复位模块用于控制芯片时钟与复位，可实现时钟选择、时钟分频、各模块使能、各模块复位等功能。

2.2 复位源

芯片的复位源主要分为板级复位，看门狗复位，软件复位，唤醒复位四类。每一类有若干种复位源，每种复位源的作用域不同。

2.2.1 板级复位源

板级复位源主要包括：

上电复位 POR(Power On Reset)。芯片上电时自动产生的复位，能够将芯片整体初始化，所有模块状态都复位成默认值。

欠压复位 BOR(Brown-Out Reset)。芯片供电电压低于一定阈值时自动产生的复位，能够将芯片整体初始化，所有模块状态都复位成默认值。

电源按键 (PWRKEY) 复位。如果芯片的电源按键 PB32 持续高电平超过 10 秒，会发生 PWRKEY 复位，将除 RTC 与 IWDT 以外的所有模块复位。通过 PMUC 的 WSR_PWRKEY 标志可以查询是否发生过 PWRKEY 复位，通过 PMUC 的 WCR_PWRKEY 可以清除该标志。

2.2.2 看门狗复位源

看门狗复位源主要包括：

全局看门狗 IWDT。如果该看门狗超时，可产生 IWDT 复位，将除 RTC 与 IWDT 以外的所有模块复位。通过 PMUC 的 WSR_IWDT 标志可以查询是否发生过 IWDT 复位，通过 IWDT 的 WDT_ICR 清除该标志。

HPSYS 看门狗 WDT1。如果该看门狗超时，可产生 WDT1 复位，复位 HCPU 以及 HPSYS 除 HPSYS_AON 以外的各外设。当 PMUC 的 WER_WDT1 寄存器为 1 时，也可扩大复位作用域，将除 PMUC，RTC 与 IWDT 以外的所有模块复位。复位作用域扩大后，可以通过 PMUC 的 WSR_WDT1 标志可以查询是否发生过 WDT1 复位，通过 PMUC 的 WCR_WDT1 清除该标志。

LPSYS 看门狗 WDT2。如果该看门狗超时，可产生 WDT2 复位，复位 LCPU 以及 LPSYS 除 LPSYS_AON 以外的各外设。当 PMUC 的 WER_WDT2 寄存器为 1 时，也可扩大复位作用域，将除 PMUC，RTC 与 IWDT 以外的所有模块复位。复位作用域扩大后，可以通过 PMUC 的 WSR_WDT2 标志可以查询是否发生过 WDT2 复位，通过 PMUC 的 WCR_WDT2 清除该标志。

2.2.3 软件复位源

软件重启 Reboot。软件通过将 PMUC 的 CR_REBOOT 写 1，可以触发软件重启。重启后除 PMUC，RTC 与 IWDT 以外的所有模块复位。软件重启后 PMUC 的 CR_REBOOT 保持为 1，可以作为发生过软件重启的标志。如果需要再次触发软件重启，需要首先将 CR_REBOOT 置 0。

HCPU 系统复位。软件通过配置 HCPU 内部寄存器发送 SYSRESETREQ，能够复位 HPSYS 内部除 HPSYS_AON 以外的各模块，包括 HCPU、EPIC、DMAC1 等。外部调试器连接上 HCPU 后发送的系统复位等同 HCPU 系统复位。

LCPU 系统复位。软件通过配置 LCPU 内部寄存器发送 SYSRESETREQ，能够复位 LPSYS 内部除 LPSYS_AON 以外的所有模块，包括 LCPU、DMAC2、MAC 等。外部调试器连接上 LCPU 后发送的系统复位等同 LCPU 系统复位。

模块 RCC 复位。可以通过 HPSYS_RCC 或 LPSYS_RCC 内的 RSTRx 寄存器实现单个模块的复位。

2.2.4 唤醒复位源

Hibernate 唤醒。芯片进入 hibernate 模式，唤醒时会将除 PMUC，RTC 与 IWDT 以外的所有模块复位。

HPSYS standby 唤醒。HPSYS 进入 standby 模式，唤醒时会复位 HPSYS 内部除 HPSYS_AON 以外的各模块，包括 HCPU、EPIC、DMAC1 等。

LPSYS standby 唤醒。LPSYS 进入 standby 模式，唤醒时会复位 LPSYS 内部除 LPSYS_AON 以外的各模块，包括 LCPU、DMAC2、MAC 等。

表 2-1: 芯片主要复位源

复位作用域		板级复位			看门狗复位		
		POR	BOR	PWRKEY	IWDT	WDT1	WDT2
HPSYS	HCPU	√	√	√	√	√	√(2)
	SRAM ret	√	√	√	√	√(1)	√(2)
	SRAM noret	√	√	√	√	√(1)	√(2)
	HPSYS 外设	√	√	√	√	√	√(2)
	HPAON	√	√	√	√	√(1)	√(2)
LPSYS	LCPU	√	√	√	√	√(1)	√
	SRAM ret	√	√	√	√	√(1)	√(2)
	SRAM noret	√	√	√	√	√(1)	√(2)
	LPSYS 外设	√	√	√	√	√(1)	√
	LPAON	√	√	√	√	√(1)	√(2)
AON	PMUC	√	√	√	√	x	x
	RTC	√	√	x	x	x	x
	IWDT	√	√	x	x	x	x

* (1)PMUC 的 WER_WDT1 寄存器为 1 时，扩大复位作用域
(2)PMUC 的 WER_WDT2 寄存器为 1 时，扩大复位作用域

表 2-2: 芯片主要复位源-续

复位作用域		软件复位			唤醒复位		
		Reboot	HCPU sysrst	LCPU sysrst	hibernate 唤醒	HPSYS standby 唤醒	LPSYS standby 唤醒
HPSYS	HCPU	√	√	x	√	√	x
	SRAM ret	√	x	x	√	x	x
	SRAM noret	√	x	x	√	√	x
	HPSYS 外设	√	√	x	√	√	x
	HPAON	√	x	x	√	x	x
LPSYS	LCPU	√	x	√	√	x	√
	SRAM ret	√	x	x	√	x	x
	SRAM noret	√	x	x	√	x	√
	LPSYS 外设	√	x	√	√	x	√
	LPAON	√	x	x	√	x	x
AON	PMUC	x	x	x	x	x	x
	RTC	x	x	x	x	x	x
	IWDT	x	x	x	x	x	x

2.3 时钟源

芯片内部主要时钟源如下表。各功能模块时钟均基于这些时钟源产生。

表 2-3: 时钟源

时钟	频率	依赖关系
clk_lrc10	~10kHz	无
clk_lxt32	32.768kHz	32k 晶振
clk_hrc48	~48MHz	无
clk_hxt48	48MHz	48M 晶振
dll1/2/3	48~384MHz	clk_hxt48
clk_audpll	44.1MHz	clk_hxt48
clk_dbl96	96MHz	clk_hxt48

clk_lrc10 是芯片内部产生的低功耗 RC 振荡器时钟，频率约为 10kHz。该时钟频率会受外部环境影响，使用时可通过测量流程获取当前频率。芯片启动后该时钟作为低功耗模块 (如 PMUC) 的默认工作时钟自动开启。clk_lrc10 相关配置寄存器是 PMUC 的 LRC_CR。

clk_lxt32 是基于外部 32k 晶振产生的低功耗时钟，频率为 32.768kHz。该时钟为可选时钟，在需要精确计时的场景下推荐使用。clk_lxt32 相关配置默认关闭，寄存器是 PMUC 的 LXT_CR。

clk_hrc48 是芯片内部产生的 RC 振荡器时钟。芯片启动时该时钟作为 HCPU 的默认工作时钟自动开启，但此时频率未经过校准，是小于 48MHz 的未知值。校准前，应先将 HCPU 的工作时钟切换到其它时钟 (如 clk_hxt48) 上，再执行校准流程。校准之后，clk_hrc48 频率是 48MHz。clk_hrc48 配置寄存器是 PMUC 的 HRC_CR，校准相关寄存器是 HPSYS_RCC 中的 HRCCAL1 和 HRCCAL2。当芯片 HPSYS 与 LPSYS 均处于低功耗模式时，该时钟默认关闭。

clk_hxt48 是基于外部 48M 晶振产生的时钟，频率为 48MHz。芯片启动时该时钟自动开启，是用于产生更高频率时钟的基础时钟，也是蓝牙工作所需的基础时钟。当系统不需要更高频率时钟，且蓝牙处于睡眠状态时，该时钟可以关闭。当芯片 HPSYS 与 LPSYS 均处于低功耗模式时，该时钟默认关闭。clk_hrc48 相关配置寄存器是 PMUC 的 HXT_CR1/2/3。

clk_dll1/2/3 是芯片内部的 DLL 模块基于 clk_hxt48 产生的高频率时钟。这些时钟默认关闭，在需要时分别开启，可独立产生不同频率。DLL 模块产生的时钟频率以 24MHz 为阶梯可配置，配置寄存器分别为 HPSYS_RCC 中的 DLL1CR,DLL2CR 和 DLL3CR。当芯片 HPSYS 处于低功耗模式时，这些时钟默认关闭。

clk_audpll 是芯片内部的 PLL 模块基于 clk_hxt48 产生的时钟，是音频相关模块的工作时钟，频率可调，通常设为 44.1MHz。该时钟默认关闭，配置寄存器位于 AUDCODEC_LP 模块。

clk_dbl96 是芯片内部的 DBL 模块基于 clk_hxt48 产生的频率固定为 96MHz 的时钟。该时钟默认关闭，相关配置寄存器是 PMUC 的 DLB96_CR。

2.4 HPSYS 时钟结构

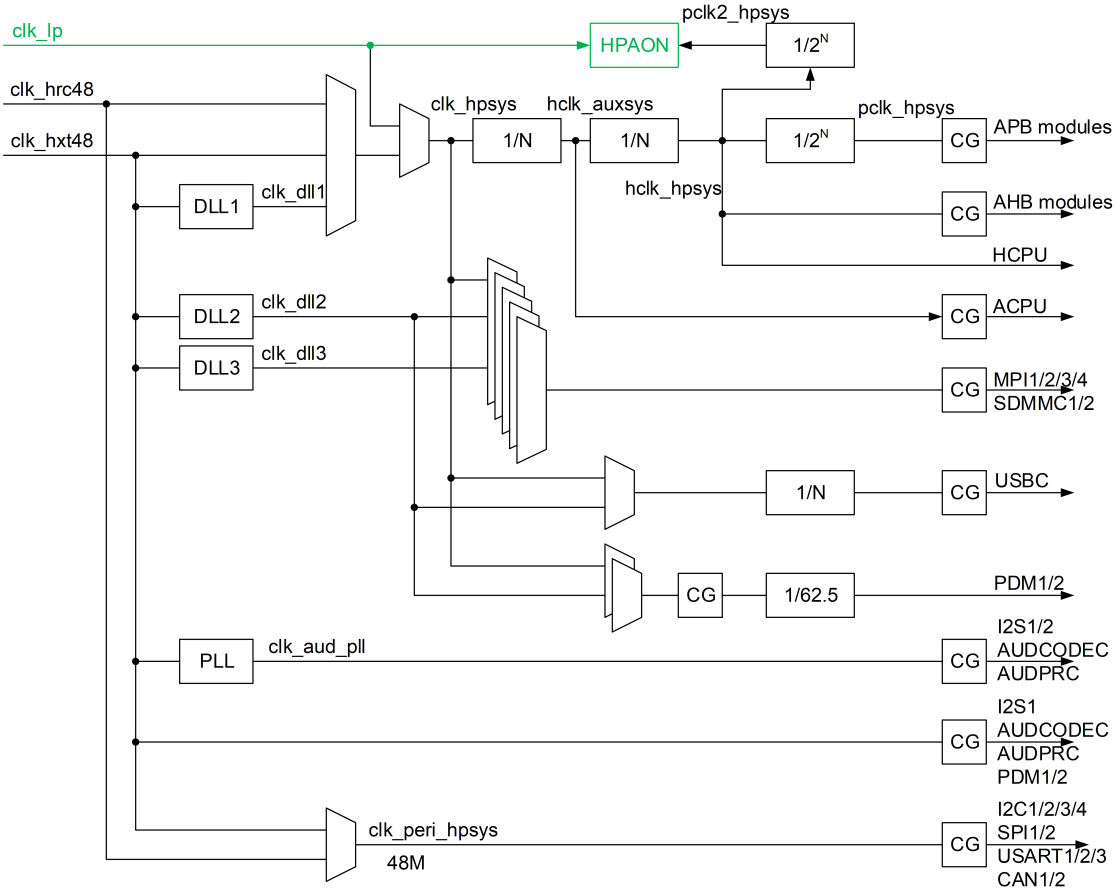

图 2-1: HPSYS 时钟结构

HPSYS 的系统时钟 clk_hpsys 可在 clk_hrc48, clk_hxt48 和 clk_dll1 中选择。选择寄存器为 HPSYS_RCC 中的 CSR_SEL_SYS。clk_hpsys 支持的最高频率是 240MHz。

hclk_hpsys 由 clk_hpsys 1 比 N 分频产生，分频比为 HPSYS_RCC 中的 CFGR_HDIV。hclk 支持的最高频率是 240MHz，是 HCPU、EPIC、DMAC1 等 AHB 模块，以及 AHB 总线和 SRAM 的工作时钟。

pclk_hpsys 由 hclk_hpsys 1 比 2^N 分频产生，分频比为 2^{CFGR_PDIV1}。pclk_hpsys 支持的最高频率是 120MHz，是 GPTIM1/2、BTIM1/2 等 APB 模块的工作时钟，以及 APB 总线时钟。当 hclk_hpsys 或 pclk_hpsys 频率发生变化时，GPTIM1/2、BTIM1/2 等模块的工作时钟频率随之改变，功能会受到影响。因此在相关模块工作时，应当使得 hclk_hpsys 和 pclk_hpsys 频率保持不变。

pclk2_hpsys 由 hclk_hpsys 1 比 2^N 分频产生，分频比为 2^{CFGR_PDIV2}。pclk2_hpsys 支持的最高频率是 7.5MHz，是 HPAON 模块的寄存器访问时钟。

clk_lp 是由 clk_lrc10 和 clk_lxt32 中选择产生的低功耗时钟 (参考 LPSYS 时钟结构图)，是 HPAON 模块的工作时钟。

MPI1/2/3 的工作时钟可在 clk_hpsys,clk_dll2 和 clk_dll3 中选择。选择寄存器为 HPSYS_RCC 中的 CSR_SEL_MPI1/2/3。

SDMMC1 的工作时钟可在 clk_hpsys, clk_dll2 和 clk_dll3 中选择。选择寄存器为 HPSYS_RCC 中的 CSR_SEL_SDMMC。

USB 的工作时钟可在 clk_hpsys 和 clk_dll2 中选择，选择寄存器为 HPSYS_RCC 中的 CSR_SEL_USB，并经 1 比 N 分频产生，分频比为 USBCR_DIV。需确保分频以后 USB 的工作时钟是 60MHz，否则 USB 无法正常工作。

USART1/2/3、SPI1/2、CAN1、I2C1/2/3/4 等外设的工作时钟 clk_peri_hpsys 可在 clk_hrc48 和 clk_hxt48 中选择，频率为 48MHz。选择寄存器为 HPSYS_RCC 中的 CSR_SEL_PERI。clk_peri_hpsys 独立于系统时钟，因此在系统动态调节频率时不受影响。

音频模块 I2S1、AUDPRC、AUDCODEC_HP(DAC) 可在两路工作时钟中选择一路使用，选择寄存器位于这些模块内部。其中一路工作时钟是 clk_hxt48，另一路是 clk_audpll。

PDM1/2 可在两路工作时钟中选择一路使用，选择寄存器位于 PDM 内部。其中一路工作时钟由 clk_hxt48 产生；另一路由 clk_audpll 16 分频产生。

2.5 HPSYS 模块使能

HPSYS_RCC 中的 ENR1 和 ENR2 寄存器控制 HPSYS 各模块使能。模块对应比特为 1 时，该模块寄存器可以访问，模块能够工作。模块对应比特为 0 时，该模块的工作时钟与总线时钟均关闭，模块停止工作，寄存器也无法访问，但寄存器值不会被复位。

2.6 HPSYS 模块复位

HPSYS_RCC 中的 RSTR1 和 RSTR2 寄存器控制 HPSYS 各模块复位。模块对应比特为 1 时，该模块寄存器与内部状态均被复位。模块对应比特为 0 时，模块停止复位。

2.7 HPSYS_RCC 寄存器

表 2-4: HPSYS_RCC 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00			**RSTR1**	Reset Register 1
[31]	rw	1'h0	PTC1	0 - no reset; 1 - reset
[30:29]			RSVD	
[28]	rw	1'h0	I2C2	0 - no reset; 1 - reset
[27]	rw	1'h0	I2C1	0 - no reset; 1 - reset
[26]	rw	1'h0	PDM2	0 - no reset; 1 - reset
[25]	rw	1'h0	PDM1	0 - no reset; 1 - reset
[24]	rw	1'h0	NNACC1	0 - no reset; 1 - reset
[23]			RSVD	
[22]	rw	1'h0	EXTDMA	0 - no reset; 1 - reset
[21]	rw	1'h0	SPI2	0 - no reset; 1 - reset
[20]	rw	1'h0	SPI1	0 - no reset; 1 - reset
[19]			RSVD	
[18]	rw	1'h0	BTIM2	0 - no reset; 1 - reset
[17]	rw	1'h0	BTIM1	0 - no reset; 1 - reset
[16]	rw	1'h0	GPTIM2	0 - no reset; 1 - reset

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表 2-4: HPSYS_RCC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[15]	rw	1'h0	GPTIM1	0 - no reset; 1 - reset
[14]	rw	1'h0	TRNG	0 - no reset; 1 - reset
[13]	rw	1'h0	CRC1	0 - no reset; 1 - reset
[12]	rw	1'h0	AES	0 - no reset; 1 - reset
[11]	rw	1'h0	EFUSEC	0 - no reset; 1 - reset
[10]	rw	1'h0	SYSCFG1	0 - no reset; 1 - reset
[9]			RSVD	
[8]	rw	1'h0	I2S1	0 - no reset; 1 - reset
[7]	rw	1'h0	LCDC1	0 - no reset; 1 - reset
[6]	rw	1'h0	EPIC	0 - no reset; 1 - reset
[5]	rw	1'h0	EZIP1	0 - no reset; 1 - reset
[4]	rw	1'h0	USART2	0 - no reset; 1 - reset
[3]	rw	1'h0	USART1	0 - no reset; 1 - reset
[2]	rw	1'h0	PINMUX1	0 - no reset; 1 - reset
[1]	rw	1'h0	MAILBOX1	0 - no reset; 1 - reset
[0]	rw	1'h0	DMAC1	0 - no reset; 1 - reset
0x04			**RSTR2**	Reset Register 2
[31:26]			RSVD	
[25]	rw	1'h0	I2C4	0 - no reset; 1 - reset
[24:21]			RSVD	
[20]	rw	1'h0	AUDPRC	0 - no reset; 1 - reset
[19]	rw	1'h0	AUDCODEC	0 - no reset; 1 - reset
[18]			RSVD	
[17]	rw	1'h0	CAN1	0 - no reset; 1 - reset
[16]	rw	1'h0	SCI	0 - no reset; 1 - reset
[15]	rw	1'h0	FACC1	0 - no reset; 1 - reset
[14]	rw	1'h0	FFT1	0 - no reset; 1 - reset
[13]			RSVD	
[12]	rw	1'h0	USART3	0 - no reset; 1 - reset
[11:10]			RSVD	
[9]	rw	1'h0	ATIM1	0 - no reset; 1 - reset
[8]	rw	1'h0	I2C3	0 - no reset; 1 - reset
[7]			RSVD	
[6]	rw	1'h0	USBC	0 - no reset; 1 - reset
[5]	rw	1'h0	SDMMC2	0 - no reset; 1 - reset
[4]	rw	1'h0	SDMMC1	0 - no reset; 1 - reset
[3]	rw	1'h0	MPI3	0 - no reset; 1 - reset
[2]	rw	1'h0	MPI2	0 - no reset; 1 - reset
[1]	rw	1'h0	MPI1	0 - no reset; 1 - reset
[0]	rw	1'h0	GPIO1	0 - no reset; 1 - reset
0x08			**ENR1**	Enable Register 1
[31]	rw	1'h0	PTC1	0 - disabled; 1 - enabled
[30:29]			RSVD	
[28]	rw	1'h1	I2C2	0 - disabled; 1 - enabled
[27]	rw	1'h1	I2C1	0 - disabled; 1 - enabled
[26]	rw	1'h0	PDM2	0 - disabled; 1 - enabled
[25]	rw	1'h0	PDM1	0 - disabled; 1 - enabled
[24]	rw	1'h0	NNACC1	0 - disabled; 1 - enabled

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表 2-4: HPSYS_RCC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[23]			RSVD	
[22]	rw	1'h1	EXTDMA	0 - disabled; 1 - enabled
[21]	rw	1'h1	SPI2	0 - disabled; 1 - enabled
[20]	rw	1'h1	SPI1	0 - disabled; 1 - enabled
[19]			RSVD	
[18]	rw	1'h1	BTIM2	0 - disabled; 1 - enabled
[17]	rw	1'h1	BTIM1	0 - disabled; 1 - enabled
[16]	rw	1'h1	GPTIM2	0 - disabled; 1 - enabled
[15]	rw	1'h1	GPTIM1	0 - disabled; 1 - enabled
[14]	rw	1'h1	TRNG	0 - disabled; 1 - enabled
[13]	rw	1'h1	CRC1	0 - disabled; 1 - enabled
[12]	rw	1'h1	AES	0 - disabled; 1 - enabled
[11]	rw	1'h1	EFUSEC	0 - disabled; 1 - enabled
[10]	rw	1'h1	SYSCFG1	0 - disabled; 1 - enabled
[9]			RSVD	
[8]	rw	1'h0	I2S1	0 - disabled; 1 - enabled
[7]	rw	1'h1	LCDC1	0 - disabled; 1 - enabled
[6]	rw	1'h0	EPIC	0 - disabled; 1 - enabled
[5]	rw	1'h0	EZIP1	0 - disabled; 1 - enabled
[4]	rw	1'h1	USART2	0 - disabled; 1 - enabled
[3]	rw	1'h1	USART1	0 - disabled; 1 - enabled
[2]	rw	1'h1	PINMUX1	0 - disabled; 1 - enabled
[1]	rw	1'h1	MAILBOX1	0 - disabled; 1 - enabled
[0]	rw	1'h1	DMAC1	0 - disabled; 1 - enabled
0x0C			**ENR2**	Enable Register 2
[31:26]			RSVD	
[25]	rw	1'h0	I2C4	0 - disabled; 1 - enabled
[24:21]			RSVD	
[20]	rw	1'h0	AUDPRC	0 - disabled; 1 - enabled
[19]	rw	1'h0	AUDCODEC	0 - disabled; 1 - enabled
[18]			RSVD	
[17]	rw	1'h0	CAN1	0 - disabled; 1 - enabled
[16]	rw	1'h0	SCI	0 - disabled; 1 - enabled
[15]	rw	1'h0	FACC1	0 - disabled; 1 - enabled
[14]	rw	1'h0	FFT1	0 - disabled; 1 - enabled
[13]			RSVD	
[12]	rw	1'h1	USART3	0 - disabled; 1 - enabled
[11:10]			RSVD	
[9]	rw	1'h0	ATIM1	0 - disabled; 1 - enabled
[8]	rw	1'h1	I2C3	0 - disabled; 1 - enabled
[7]			RSVD	
[6]	rw	1'h0	USBC	0 - disabled; 1 - enabled
[5]	rw	1'h0	SDMMC2	0 - disabled; 1 - enabled
[4]	rw	1'h0	SDMMC1	0 - disabled; 1 - enabled
[3]	rw	1'h1	MPI3	0 - disabled; 1 - enabled
[2]	rw	1'h1	MPI2	0 - disabled; 1 - enabled
[1]	rw	1'h1	MPI1	0 - disabled; 1 - enabled
[0]	rw	1'h1	GPIO1	0 - disabled; 1 - enabled

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表 2-4: HPSYS_RCC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
0x10			**CSR**	Clock Select Register
[31:18]			RSVD	
[17:16]	rw	2'h0	SEL_SDMMC	select SDMMC1 function clock 0 - clk_hpsys; 1 - reserved; 2 - clk_dll2; 3 - clk_dll3
[15]	rw	1'b0	SEL_USBC	select USB source clock 0 - clk_hpsys; 1 - clk_dll3
[14:13]			RSVD	
[12]	rw	1'h0	SEL_PERI	select clk_peri_hpsys source used by USART/SPI/CAN/I2C 0 - clk_hrc48; 1 - clk_hxt48
[11:10]			RSVD	
[9:8]	rw	2'h0	SEL_MPI3	selet MPI3 function clock 0 - clk_hpsys; 1 - reserved; 2 - clk_dll2; 3 - clk_dll3
[7:6]	rw	2'h0	SEL_MPI2	selet MPI2 function clock 0 - clk_hpsys; 1 - reserved; 2 - clk_dll2; 3 - clk_dll3
[5:4]	rw	2'h0	SEL_MPI1	selet MPI1 function clock 0 - clk_hpsys; 1 - reserved; 2 - clk_dll2; 3 - clk_dll3
[3]			RSVD	
[2]	rw	1'h0	SEL_SYS_LP	select clk_hpsys source 0 - selected by SEL_SYS; 1 - clk_lp
[1:0]	rw	2'h0	SEL_SYS	select clk_hpsys source 0 - clk_hrc48; 1 - clk_hxt48; 2 - reserved; 3 - clk_dll1
0x14			**CFGR**	Clock Configuration Register
[31:15]			RSVD	
[14:12]	rw	3'b111	PDIV2	pclk2_hpsys = hclk_hpsys / (2^{PDIV2}), by default divided by 128
[11]			RSVD	
[10:8]	rw	3'b001	PDIV1	pclk_hpsys = hclk_hpsys / (2^{PDIV1}), by default divided by 2
[7:0]	rw	8'h1	HDIV	hclk_hpsys = clk_hpsys / HDIV if HDIV=0, hclk_hpsys = clk_hpsys
0x18			**USBCR**	USBC Register
[31:3]			RSVD	
[2:0]	rw	3'h4	DIV	USB function clock is USB source clock divided by DIV. After divider, USB function clock must be 60MHz.
0x1C			**DLL1CR**	DLL1 Control Register
[31]	r	1'b0	READY	0: dll not ready 1: dll ready
[30:28]	rw	3'b0	LOCK_DLY	
[27:25]	rw	3'b0	PU_DLY	
[24:21]	rw	4'b0	DTEST_TR	
[20]	rw	1'b0	DTEST_EN	
[19]	rw	1'b0	BYPASS	
[18]	rw	1'b0	VST_SEL	
[17]	rw	1'b0	PRCHG_EXT	
[16]	rw	1'b1	PRCHG_EN	
[15]	rw	1'b1	MCU_PRCHG	
[14]	rw	1'b1	MCU_PRCHG_EN	
[13]	rw	1'b1	OUT_DIV2_EN	0: dll output not divided 1: dll output divided by 2
[12]	rw	1'b1	IN_DIV2_EN	

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表 2-4: HPSYS_RCC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[11:8]	rw	4'ha	LDO_VREF	
[7]	rw	1'b0	MODE48M_EN	
[6]	rw	1'b1	XTALIN_EN	
[5:2]	rw	4'h0	STG	DLL lock freqency is decided by STG. DLL output frequency is (STG+1)*24MHz e.g. STG=9,DLL output is 240M
[1]	rw	1'b0	SW	
[0]	rw	1'b0	EN	0: dll disabled 1: dll enabled
0x20			**DLL2CR**	DLL2 Control Register
[31]	r	1'b0	READY	0: dll not ready 1: dll ready
[30:28]	rw	3'b0	LOCK_DLY	
[27:25]	rw	3'b0	PU_DLY	
[24:21]	rw	4'b0	DTEST_TR	
[20]	rw	1'b0	DTEST_EN	
[19]	rw	1'b0	BYPASS	
[18]	rw	1'b0	VST_SEL	
[17]	rw	1'b0	PRCHG_EXT	
[16]	rw	1'b1	PRCHG_EN	
[15]	rw	1'b1	MCU_PRCHG	
[14]	rw	1'b1	MCU_PRCHG_EN	
[13]	rw	1'b1	OUT_DIV2_EN	0: dll output not divided 1: dll output divided by 2
[12]	rw	1'b1	IN_DIV2_EN	
[11:8]	rw	4'ha	LDO_VREF	
[7]	rw	1'b0	MODE48M_EN	
[6]	rw	1'b1	XTALIN_EN	
[5:2]	rw	4'h0	STG	DLL lock freqency is decided by STG. DLL output frequency is (STG+1)*24MHz e.g. STG=9,DLL output is 240M
[1]	rw	1'b0	SW	
[0]	rw	1'b0	EN	0: dll disabled 1: dll enabled
0x24			**DLL3CR**	DLL3 Control Register
[31]	r	1'b0	READY	0: dll not ready 1: dll ready
[30:28]	rw	3'b0	LOCK_DLY	
[27:25]	rw	3'b0	PU_DLY	
[24:21]	rw	4'b0	DTEST_TR	
[20]	rw	1'b0	DTEST_EN	
[19]	rw	1'b0	BYPASS	
[18]	rw	1'b0	VST_SEL	
[17]	rw	1'b0	PRCHG_EXT	
[16]	rw	1'b1	PRCHG_EN	
[15]	rw	1'b1	MCU_PRCHG	
[14]	rw	1'b1	MCU_PRCHG_EN	

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表 2-4: HPSYS_RCC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[13]	rw	1'b1	OUT_DIV2_EN	0: dll output not divided 1: dll output divided by 2
[12]	rw	1'b1	IN_DIV2_EN	
[11:8]	rw	4'ha	LDO_VREF	
[7]	rw	1'b0	MODE48M_EN	
[6]	rw	1'b1	XTALIN_EN	
[5:2]	rw	4'h0	STG	DLL lock freqency is decided by STG. DLL output frequency is (STG+1)*24MHz e.g. STG=9,DLL output is 240M
[1]	rw	1'b0	SW	
[0]	rw	1'b0	EN	0: dll disabled 1: dll enabled
0x28			**HRCCAL1**	HRC Calibration Register 1
[31]	r	1'b0	CAL_DONE	Calibration done. After a new calibration started, results should be processed only when cal_done asserted.
[30]	rw	1'b0	CAL_EN	Calibration enble. Set to 0 to clear result, then set to 1 to start a new calibration
[29:16]			RSVD	
[15:0]	rw	16'h8000	CAL_LENGTH	Target clk_hxt48 cycles during calibration
0x2C			**HRCCAL2**	HRC Calibration Register 2
[31:16]	r	16'h0	HXT_CNT	Total clk_hxt48 cycles during calibration
[15:0]	r	16'h0	HRC_CNT	Total clk_hrc48 cycles during calibration
0x30			**DBGCLKR**	Debug Clock Register
[31:28]			RSVD	
[27:26]	rw	2'b0	DLL3_OUT_STR	for debug only
[25]	rw	1'b0	DLL3_CG_EN	for debug only
[24]	rw	1'b0	DLL3_OUT_RSTB	for debug only
[23]	rw	1'b0	DLL3_LOOP_EN	for debug only
[22]	rw	1'b0	DLL3_OUT_EN	for debug only
[21]	rw	1'b0	DLL3_LDO_EN	for debug only
[20]	rw	1'b0	DLL3_DBG	for debug only
[19:18]	rw	2'b0	DLL2_OUT_STR	for debug only
[17]	rw	1'b0	DLL2_CG_EN	for debug only
[16]	rw	1'b0	DLL2_OUT_RSTB	for debug only
[15]	rw	1'b0	DLL2_LOOP_EN	for debug only
[14]	rw	1'b0	DLL2_OUT_EN	for debug only
[13]	rw	1'b0	DLL2_LDO_EN	for debug only
[12]	rw	1'b0	DLL2_DBG	for debug only
[11:10]	rw	2'b0	DLL1_OUT_STR	for debug only
[9]	rw	1'b0	DLL1_CG_EN	for debug only
[8]	rw	1'b0	DLL1_OUT_RSTB	for debug only
[7]	rw	1'b0	DLL1_LOOP_EN	for debug only
[6]	rw	1'b0	DLL1_OUT_EN	for debug only
[5]	rw	1'b0	DLL1_LDO_EN	for debug only
[4]	rw	1'b0	DLL1_DBG	for debug only
[3]			RSVD	
[2]	rw	1'b0	CLK_EN	for debug only

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表 2-4: HPSYS_RCC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[1:0]	rw	2'b0	CLK_SEL	for debug only
0x34			**DBGR**	Debug Register
[31:4]			RSVD	
[3]	rw	1'h0	FORCE_GPIO	for debug only
[2]	rw	1'h0	FORCE_BUS	for debug only
[1]	rw	1'h0	SYSCLK_SWLP	for debug only
[0]	rw	1'h0	SYSCLK_AON	for debug only
0x38			**DWCFGR**	Deep WFI mode Clock Configuration Register
[31:30]			RSVD	
[29]	rw	1'b0	DLL3_OUT_RSTB	for debug only
[28]	rw	1'b0	DLL3_OUT_EN	for debug only
[27]	rw	1'b0	DLL2_OUT_RSTB	for debug only
[26]	rw	1'b0	DLL2_OUT_EN	for debug only
[25]	rw	1'b0	DLL1_OUT_RSTB	for debug only
[24]	rw	1'b0	DLL1_OUT_EN	for debug only
[23:19]			RSVD	
[18]	rw	1'h1	SEL_SYS_LP	select clk_hpsys source during deep WFI 0 - selected by SEL_SYS; 1 - clk_lp
[17:16]	rw	2'h0	SEL_SYS	select clk_hpsys source during deep WFI 0 - clk_hrc48; 1 - clk_hxt48; 2 - reserved; 3 - clk_dll1
[15]	rw	1'h1	DIV_EN	enable PDIV1, PDIV2 and HDIV reconfiguration during deep WFI
[14:12]	rw	3'b001	PDIV2	pclk2_hpsys = hclk_hpsys / (2^{PDIV2}) during deep WFI
[11]			RSVD	
[10:8]	rw	3'b001	PDIV1	pclk_hpsys = hclk_hpsys / (2^{PDIV1}) during deep WFI
[7:0]	rw	8'h1	HDIV	hclk_hpsys = clk_hpsys / HDIV during deep WFI

2.8 LPSYS 时钟结构

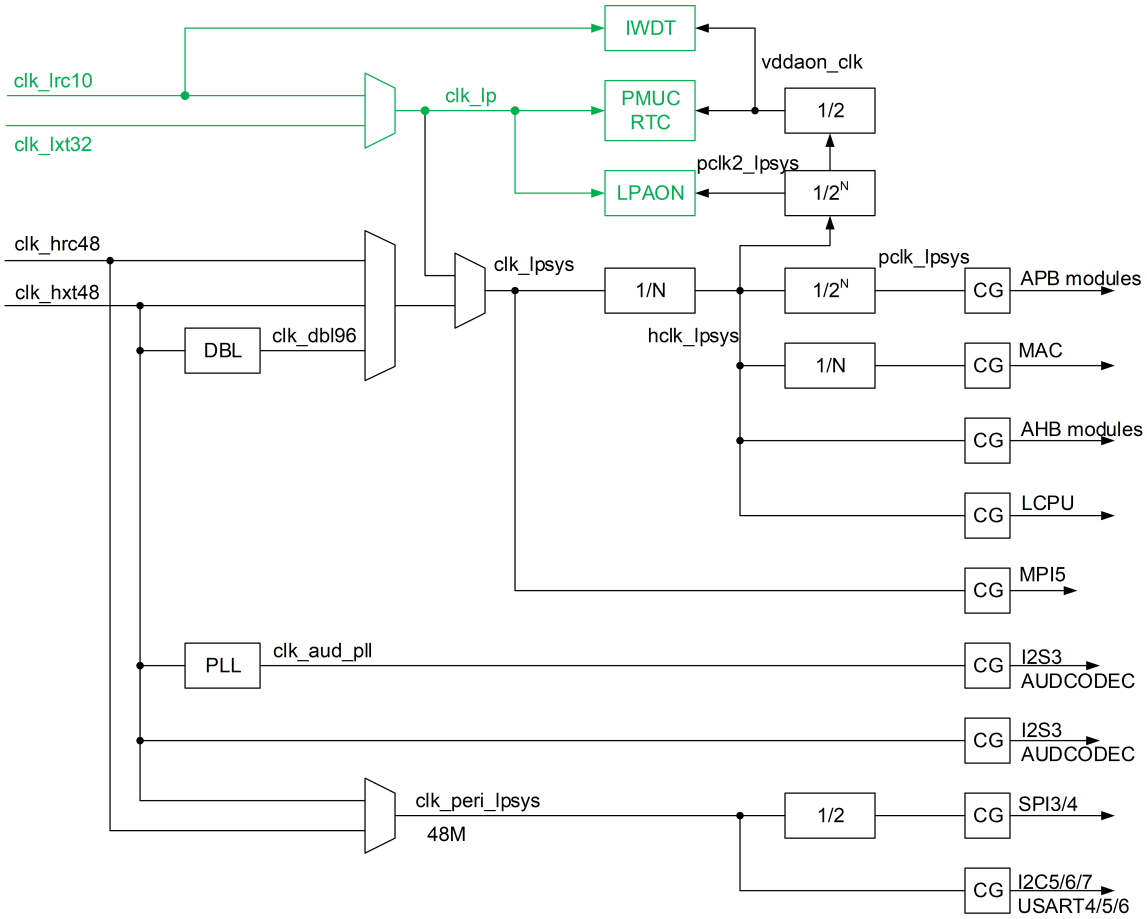

图 2-2: LPSYS 时钟结构

LPSYS 的系统时钟 clk_lpsys 可在 clk_hrc48，clk_hxt48 和 clk_dbl96 中选择，选择寄存器为 LPSYS_RCC 中的 CSR_SEL_SYS。clk_lpsys 支持的最高频率是 48MHz(基础模式) 或 96MHz(增强模式)。

hclk_lpsys 由 clk_lpsys 1 比 N 分频产生，分频比为 LPSYS_RCC 中的 CFGR_HDIV1。hclk_lpsys 支持的最高频率是 48MHz(基础模式) 或 96MHz(增强模式)，是 LCPU、DMAC2 等 AHB 模块，以及 AHB 总线和 SRAM 的工作时钟。LPSYS_RCC 中的 CFGR_HDIV2 用于调节 SRAM 的等待周期，当 hclk_lpsys 频率大于 24MHz 时，CFGR_HDIV2 应当为 1，否则为 0。

hclk_lpsys 经过 1 比 N 分频，产生蓝牙 MAC 所需时钟，分频比为 LPSYS_RCC 中的 CFGR_MACDIV。

pclk_lpsys 由 hclk_lpsys 1 比 2^N 分频产生，分频比为 2^{CFGR_PDIV1}。pclk_lpsys 支持的最高频率是 24MHz(基础模式) 或 48MHz(增强模式)，是 GPTIM3/4/5、BTIM3/4、GPADC 等 APB 模块的工作时钟，以及 APB 总线时钟。当 hclk_lpsys 或 pclk_lpsys 频率发生变化时，GPTIM3/4/5、BTIM3/4、GPADC 等模块的工作时钟频率随之改变，功能会受到影响。因此在相关模块工作时，应当使得 hclk_lpsys 和 pclk_lpsys 频率保持不变。

pclk2_lpsys 由 hclk_lpsys 1 比 2^N 分频产生，分频比为 2^{CFGR_PDIV2}。pclk2_lpsys 支持的最高频率是 6MHz，是 LPAON、PMUC、IWDT、RTC 等模块的寄存器访问时钟。

低功耗时钟 clk_lp 可在 clk_lrc10 和 clk_lxt32 中选择，是 LPAON、PMUC、RTC 等低功耗模块的工作时钟，以及蓝牙的睡眠时钟。clk_lp 选择寄存器为 PMUC 模块的 CR_SEL_LPCLK。

IWDT 的工作时钟固定为 clk_lrc10，不受 CR_SEL_LPCLK 影响。

MPI5 的工作时钟由 clk_lpsys 产生。

USART4/5/6、I2C5/6/7 等外设的工作时钟 clk_peri_lpsys 可在 clk_hrc48 和 clk_hxt48 中选择，频率为 48MHz，选择寄存器为 LPSYS_RCC 中的 CSR_SEL_PERI。SPI3/4 的工作时钟为 clk_peri_lpsys 的二分频，即 24MHz。clk_peri_lpsys 独立于系统时钟，因此在系统动态调节频率时不受影响。

音频模块 AUDCODEC_LP(ADC) 可在两路工作时钟中选择一路使用，选择寄存器位于模块内部。其中一路工作时钟是 clk_hxt48，另一路是 clk_audpll。

2.9 LPSYS 模块使能

LPSYS_RCC 中的 ENR1 和 ENR2 寄存器控制各模块使能。模块对应比特为 1 时，该模块寄存器可以访问，模块能够工作。模块对应比特为 0 时，该模块的工作时钟与总线时钟均关闭，模块停止工作，寄存器也无法访问，但寄存器值不会被复位。

2.10 LPSYS 模块复位

LPSYS_RCC 中的 RSTR1 和 RSTR2 寄存器控制各模块复位。模块对应比特为 1 时，该模块寄存器与内部状态均被复位。模块对应比特为 0 时，模块停止复位。

2.11 LPSYS_RCC 寄存器

表 2-5: LPSYS_RCC 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00			**RSTR1**	Reset Register 1
[31:30]			RSVD	
[29]	rw	1'h0	BUSMON2	0 - no reset; 1 - reset
[28]			RSVD	
[27]	rw	1'h0	PTC2	0 - no reset; 1 - reset
[26]	rw	1'h0	TSEN	0 - no reset; 1 - reset
[25]	rw	1'h0	LPCOMP	0 - no reset; 1 - reset
[24]	rw	1'h0	AUDCODEC	0 - no reset; 1 - reset
[23]			RSVD	
[22]	rw	1'h0	GPADC	0 - no reset; 1 - reset
[21]			RSVD	
[20]	rw	1'h0	BTIM4	0 - no reset; 1 - reset
[19]	rw	1'h0	BTIM3	0 - no reset; 1 - reset
[18]	rw	1'h0	GPTIM5	0 - no reset; 1 - reset
[17]	rw	1'h0	GPTIM4	0 - no reset; 1 - reset
[16]	rw	1'h0	GPTIM3	0 - no reset; 1 - reset
[15]	rw	1'h0	SYSCFG2	0 - no reset; 1 - reset

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表 2-5: LPSYS_RCC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[14]	rw	1'h0	I2C7	0 - no reset; 1 - reset
[13]	rw	1'h0	I2C6	0 - no reset; 1 - reset
[12]	rw	1'h0	I2C5	0 - no reset; 1 - reset
[11]			RSVD	
[10]	rw	1'h0	SPI4	0 - no reset; 1 - reset
[9]	rw	1'h0	SPI3	0 - no reset; 1 - reset
[8]			RSVD	
[7]	rw	1'h0	USART6	0 - no reset; 1 - reset
[6]	rw	1'h0	USART5	0 - no reset; 1 - reset
[5]	rw	1'h0	USART4	0 - no reset; 1 - reset
[4]	rw	1'h0	PATCH	0 - no reset; 1 - reset
[3]	rw	1'h0	PINMUX2	0 - no reset; 1 - reset
[2]	rw	1'h0	MAILBOX2	0 - no reset; 1 - reset
[1]	rw	1'h0	DMAC2	0 - no reset; 1 - reset
[0]	rw	1'h0	LCPU	0 - no reset; 1 - reset
0x04			**RSTR2**	Reset Register 2
[31:6]			RSVD	
[5]	rw	1'h0	CRC2	0 - no reset; 1 - reset
[4]	rw	1'h0	MAC	0 - no reset; 1 - reset
[3]	rw	1'h0	PHY	0 - no reset; 1 - reset
[2]	rw	1'h0	RFC	0 - no reset; 1 - reset
[1]	rw	1'h0	MPI5	0 - no reset; 1 - reset
[0]	rw	1'h0	GPIO2	0 - no reset; 1 - reset
0x08			**ENR1**	Enable Register 1
[31:30]			RSVD	
[29]	rw	1'h0	BUSMON2	0 - disabled; 1 - enabled
[28]			RSVD	
[27]	rw	1'h0	PTC2	0 - disabled; 1 - enabled
[26]	rw	1'h1	TSEN	0 - disabled; 1 - enabled
[25]	rw	1'h1	LPCOMP	0 - disabled; 1 - enabled
[24]	rw	1'h1	AUDCODEC	0 - disabled; 1 - enabled
[23]			RSVD	
[22]	rw	1'h1	GPADC	0 - disabled; 1 - enabled
[21]			RSVD	
[20]	rw	1'h1	BTIM4	0 - disabled; 1 - enabled
[19]	rw	1'h1	BTIM3	0 - disabled; 1 - enabled
[18]	rw	1'h1	GPTIM5	0 - disabled; 1 - enabled
[17]	rw	1'h1	GPTIM4	0 - disabled; 1 - enabled
[16]	rw	1'h1	GPTIM3	0 - disabled; 1 - enabled
[15]	RW	1'h1	SYSCFG2	0 - disabled; 1 - enabled
[14]	rw	1'h1	I2C7	0 - disabled; 1 - enabled
[13]	rw	1'h1	I2C6	0 - disabled; 1 - enabled
[12]	rw	1'h1	I2C5	0 - disabled; 1 - enabled
[11]			RSVD	
[10]	rw	1'h1	SPI4	0 - disabled; 1 - enabled
[9]	rw	1'h1	SPI3	0 - disabled; 1 - enabled
[8]			RSVD	
[7]	rw	1'h1	USART6	0 - disabled; 1 - enabled

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表 2-5: LPSYS_RCC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[6]	rw	1'h1	USART5	0 - disabled; 1 - enabled
[5]	rw	1'h1	USART4	0 - disabled; 1 - enabled
[4]	rw	1'h1	PATCH	0 - disabled; 1 - enabled
[3]	rw	1'h1	PINMUX2	0 - disabled; 1 - enabled
[2]	rw	1'h1	MAILBOX2	0 - disabled; 1 - enabled
[1]	rw	1'h1	DMAC2	0 - disabled; 1 - enabled
[0]			RSVD	
0x0C			**ENR2**	Enable Register 2
[31:6]			RSVD	
[5]	rw	1'h1	CRC2	0 - disabled; 1 - enabled
[4]	rw	1'h1	MAC	0 - disabled; 1 - enabled
[3]	rw	1'h1	PHY	0 - disabled; 1 - enabled
[2]	rw	1'h1	RFC	0 - disabled; 1 - enabled
[1]	rw	1'h1	MPI5	0 - disabled; 1 - enabled
[0]	rw	1'h1	GPIO2	0 - disabled; 1 - enabled
0x10			**CSR**	Clock Select Register
[31:5]			RSVD	
[4]	rw	1'h0	SEL_PERI	select clk_peri_lpsys source used by USART/SPI/I2C 0 - clk_hrc48; 1 - clk_hxt48
[3]			RSVD	
[2]	rw	1'h0	SEL_SYS_LP	select clk_lpsys source 0 - selected by SEL_SYS; 1 - clk_lp
[1:0]	rw	2'h0	SEL_SYS	select clk_lpsys source 0 - clk_hrc48; 1 - clk_hxt48; 2 - clk_dbl96; 3 - reserved
0x14			**CFGR**	Clock Configuration Register
[31:25]			RSVD	
[24:20]	rw	5'h8	MACFREQ	clock frequency of MAC clock
[19:16]	rw	4'h3	MACDIV	MAC clock divider MACCLK = hclk_lpsys / MACDIV
[15]			RSVD	
[14:12]	rw	3'b101	PDIV2	pclk2_lpsys = hclk_lpsys / (2^{PDIV2}), by default divided by 32
[11]			RSVD	
[10:8]	rw	3'b001	PDIV1	pclk_lpsys = hclk_lpsys / (2^{PDIV1}), by default divided by 2
[7]			RSVD	
[6]	rw	1'h0	HDIV2	should set to 0 if hclk_lpsys frequency no higher than 24MHz should set to 1 if hclk_lpsys frequency higher than 24MHz
[5:0]	rw	6'h2	HDIV1	hclk_lpsys = clk_lpsys / HDIV1 if HDIV1=0, hclk_lpsys = clk_lpsys
0x20			**DBGR**	Debug Register
[31:6]			RSVD	
[5]	rw	1'h0	SYSCLK_SWBT	If set to 1, clk_lpsys will: switch from clk_hrc48 to clk_hxt48 when MAC active; switch from clk_hxt48 to clk_hrc48 when MAC sleep;
[4]	rw	1'h0	FORCE_GPIO	for debug only
[3]	rw	1'h0	FORCE_MAC	for debug only
[2]	rw	1'h0	FORCE_BUS	for debug only
[1]	rw	1'h0	SYSCLK_SWLP	for debug only
[0]	rw	1'h0	SYSCLK_AON	for debug only

3 电源管理

3.1 简介

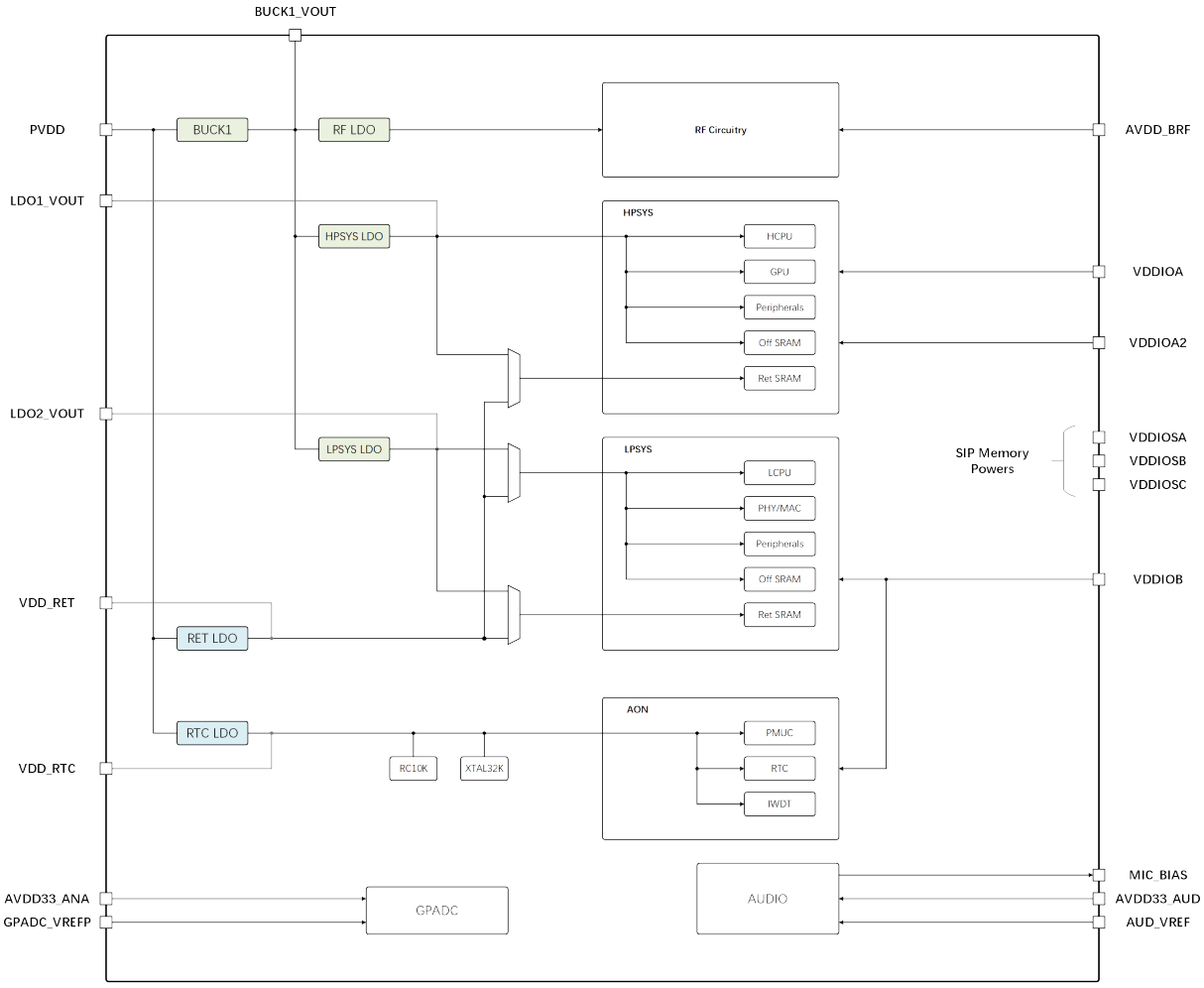

图 3-1: BGA 封装电源管理架构

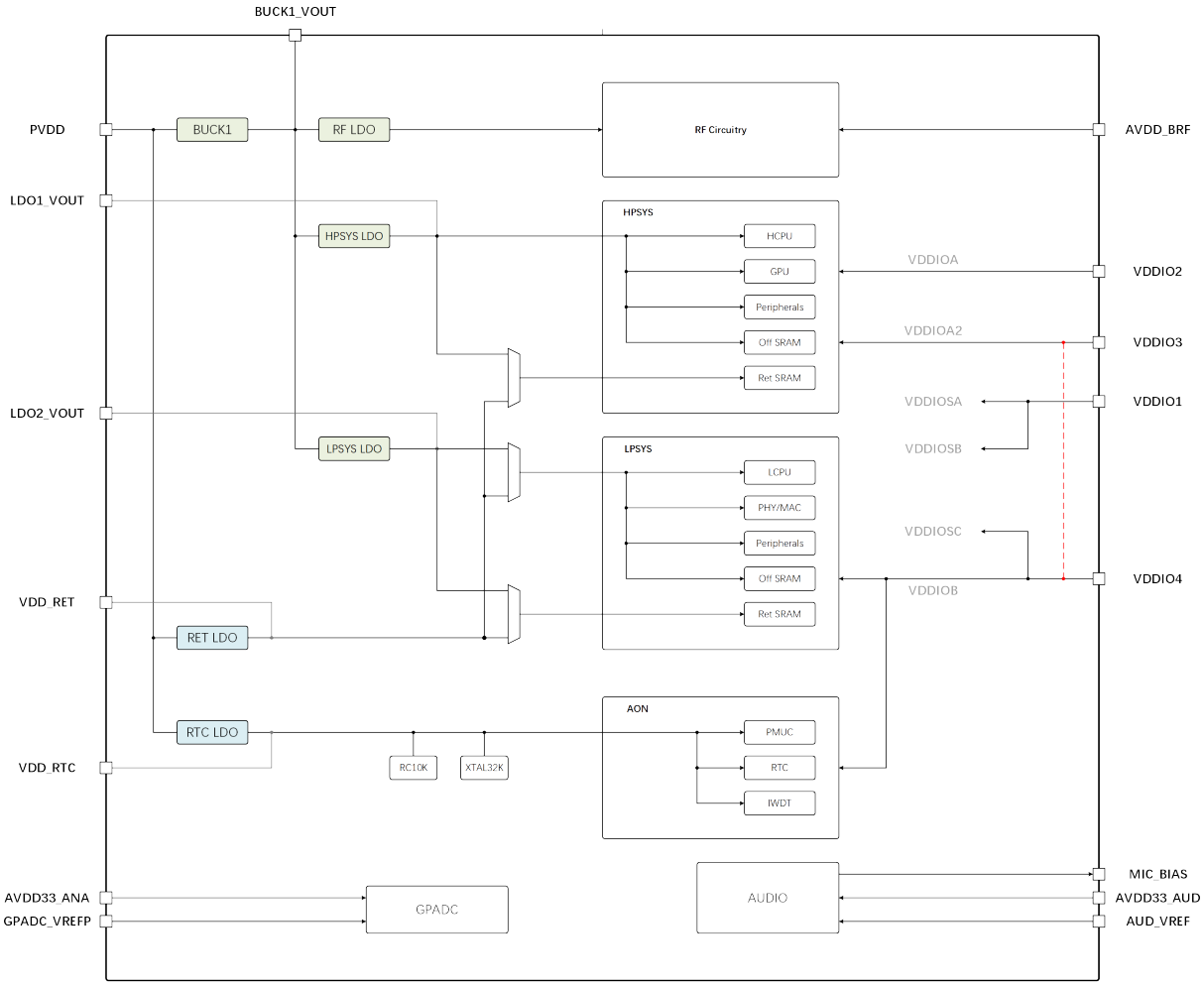

图 3-2: QFN 封装电源管理架构

说明：

QFN 封装相比于 BGA 封装，将部分 IO 电源和 SIP Memory 电源合并，其中：

- SF32LB561/563：VDDIOSA 和 VDDIOSB 合并为 VDDIO1，VDDIOSC 和 VDDIOB 合并为 VDDIO4
- SF32LB560：将上述 VDDIO4 进一步和 VDDIO3 合并为 VDDIO3（红色虚线）

3.2 PMUC 寄存器

表 3-1: PMUC 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00			**CR**	Control Register
[31:18]			RSVD	
[17:14]	rw	4'h1	PIN1_SEL	
[13:10]	rw	4'h0	PIN0_SEL	select one out of 14 Pins PBR[3:0], PA[4:0], PB[4:0]
[9:7]	rw	3'h0	PIN1_MODE	0 - high level, 1 - low level, 2 - pos edge, 3 - neg edge
[6:4]	rw	3'h0	PIN0_MODE	4/6 - both edge (high-active detection), 5/7 - both edge (low-active detection)
[3]			RSVD	
[2]	rw	1'h0	REBOOT	Write 1 to reboot; write 0 to clear after boot up

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表 3-1: PMUC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[1]	rw	1'h0	HIBER_EN	Write 1 to enter hibernate mode; write 0 to clear when exit from hibernate
[0]	rw	1'h0	SEL_LPCLK	0 - LRC10, 1 - LXT32
0x04			**WER**	Wakeup Enable register
[31:5]			RSVD	
[4]	rw	1'b0	PIN1	Set 1 to enable PIN1 as wakeup source
[3]	rw	1'b0	PIN0	Set 1 to enable PIN0 as wakeup source
[2]	rw	1'b0	WDT2	Set 1 to enable WDT2 as reboot cause
[1]	rw	1'b0	WDT1	Set 1 to enable WDT1 as reboot cause
[0]	rw	1'b0	RTC	Set 1 to enable RTC as wakeup source
0x08			**WSR**	Wakeup Status register
[31:7]			RSVD	
[6]	r	1'b0	PWRKEY	
[5]	r	1'b0	IWDT	
[4]	r	1'b0	PIN1	
[3]	r	1'b0	PIN0	
[2]	r	1'b0	WDT2	Indicates reboot by WDT2
[1]	r	1'b0	WDT1	Indicates reboot by WDT1
[0]	r	1'b0	RTC	Indicates the wakeup status from RTC. Note: the status is masked by WER
0x0C			**WCR**	Wakeup Clear register
[31]	w1c	1'b0	AON	Write 1 to clear the AON wakeup IRQ status
[30:7]			RSVD	
[6]	w1c	1'b0	PWRKEY	Write 1 to clear PWRKEY reset flag
[5]			RSVD	
[4]	w1c	1'b0	PIN1	Write 1 to clear PIN1 wakeup flag.
[3]	w1c	1'b0	PIN0	Write 1 to clear PIN0 wakeup flag. Only valid if PIN wakeup is configured as edge trigger
[2]	w1c	1'b0	WDT2	Write 1 to clear WDT2 reboot flag
[1]	w1c	1'b0	WDT1	Write 1 to clear WDT1 reboot flag
[0]			RSVD	
0x10			**VRTC_CR**	VRTC Control Register
[31:13]			RSVD	
[12:9]	rw	4'hf	BOR_VT_TRIM	
[8]	rw	1'h0	BOR_EN	Brownout Reset Enable
[7:4]	rw	4'h7	VRTC_TRIM	
[3:0]	rw	4'hc	VRTC_VBIT	
0x14			**VRET_CR**	VRET Control Register
[31]	r	1'h0	RDY	
[30:27]			RSVD	
[26:21]	rw	6'h20	DLY	VRET_LDO power up delay in number of CLK_LP cycles
[20:17]	r	4'h0	CAL_TRIM	
[16]	r	1'h0	CAL_RDY	
[15]	rw	1'h1	TRIM_RSTN	
[14]	rw	1'h0	TRIM_SEL	
[13:10]	rw	4'h7	TRIM	
[9:6]			RSVD	
[5:2]	rw	4'h7	VBIT	
[1]	rw	1'h0	BM	
[0]	rw	1'h1	EN	

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表 3-1: PMUC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
0x18			**LRC_CR**	RC10K Control Register
[31:9]			RSVD	
[8]	rw	1'h0	REFRES	
[7:6]	rw	2'h3	CHGCAP	
[5:4]	rw	2'h3	CHGCRT	
[3]	rw	1'h0	CMPBM2	
[2:1]	rw	2'h0	CMPBM1	
[0]	rw	1'h1	EN	Enabled by default
0x1C			**LXT_CR**	XTAL32K Control Register
[31]	r	1'h0	RDY	
[30:15]			RSVD	
[14]	rw	1'h1	CAP_SEL	
[13:10]	rw	4'hf	BMSTART	
[9]	rw	1'h1	BMSEL	
[8]	rw	1'h0	AMPCTRL_ENB	
[7:6]	rw	2'h2	AMP_BM	
[5:2]	rw	4'h2	BM	
[1]	rw	1'h0	RSN	
[0]	rw	1'h0	EN	
0x20			**BG1_CR**	BG1 Control Register
[31:24]			RSVD	
[23:20]	rw	4'h6	BG1_VREF_L	low voltage = 0.9V
[19:16]	rw	4'h9	BG1_VREF_M	middle voltage = 1.05V
[15:12]			RSVD	
[11]	rw	1'b0	LDOBG_EN	Force LDOBG enable
[10:9]	rw	2'b01	BG1_DLY	Bandgap power up delay in CLK_LP cycles
[8:5]	rw	4'hd	BG1_VREF12	
[4:1]	rw	4'hd	BG1_VREF06	
[0]	rw	1'h0	BG1_EN	Force BG1 enable
0x24			**BUCK1_CR1**	BUCK1 Control Register 1
[31]	rw	1'h0	BUCK1_FORCE_RDY	
[30]	rw	1'h0	BUCK1_H2M_EN	
[29]	rw	1'h0	BUCK1_H2L_EN	
[28]	rw	1'h0	BUCK1_M2L_EN	
[27]	rw	1'h0	BUCK1_L2M_EN	
[26]	r	1'h0	BUCK1_RDY	
[25]	rw	1'h1	BUCK1_ZCD_AON	
[24:22]	rw	3'h5	BUCK1_BM_ZCD	
[21:19]	rw	3'h4	BUCK1_BM_PWMCMP	
[18:16]	rw	3'h3	BUCK1_BM_COTCMP	
[15:13]	rw	3'h3	BUCK1_MOT	
[12]	rw	1'h0	BUCK1_SEL_LX22	
[11:8]	rw	4'h5	BUCK1_CS	
[7:4]	rw	4'h7	BUCK1_CCH	
[3:1]	rw	3'h5	BUCK1_ILIMIT	
[0]	rw	1'h1	BUCK1_EN	
0x28			**BUCK1_CR2**	BUCK1 Control Register 2
[31:24]			RSVD	

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表 3-1: PMUC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[23:16]	rw	8'h0	L2M_CNT	
[15:8]	rw	8'h0	L2H_CNT	
[7:0]	rw	8'h0	M2H_CNT	
0x2C			**HPSYS_LDO**	HPSYS LDO Control Register
[31:17]			RSVD	
[16]	r	1'b0	RDY	
[15:10]	rw	6'h8	DLY	HPSYS_LDO power up delay in CLK_LP cycles
[9:6]	rw	4'ha	VREF2	Lower voltage for deep sleep mode
[5:2]	rw	4'hb	VREF	
[1]	rw	1'b0	BP	
[0]	rw	1'b1	EN	
0x30			**LPSYS_LDO**	LPSYS LDO Control Register
[31:17]			RSVD	
[16]	r	1'b0	RDY	
[15:10]	rw	6'h8	DLY	LPSYS_LDO power up delay in CLK_LP cycles
[9:6]	rw	4'h5	VREF2	Lower voltage for deep sleep mode
[5:2]	rw	4'h5	VREF	
[1]	rw	1'b0	BP	
[0]	rw	1'b1	EN	
0x34			**HPSYS_SWR**	HPSYS Switch Register
[31]	r	1'b0	RDY	
[30:8]			RSVD	
[7]	rw	1'b0	NORET	Cut off VHPRET entirely during standby. No retention
[6:4]	rw	3'h3	DLY	wait for N cycles before asserting RDY
[3:2]			RSVD	
[1:0]	rw	2'b10	PSW	[0] - RET_LDO; [1] - HPSYS_LDO
0x38			**LPSYS_SWR**	LPSYS Switch Register
[31]	r	1'b0	RDY	
[30:8]			RSVD	
[7]	rw	1'b0	NORET	Cut off VLPMEM entirely during standby. No retention
[6:4]	rw	3'h3	DLY	
[3:2]	rw	2'b01	PSW_RET	PSW value during DS/SB
[1:0]	rw	2'b10	PSW	[0] - RET_LDO; [1] - LPSYS_LDO
0x3C			**PMU_TR**	PMU Test Register
[31:9]			RSVD	
[8:6]	rw	3'h0	PMU_DC_MR	macro select
[5:3]	rw	3'h0	PMU_DC_BR	block select
[2:0]	rw	3'h0	PMU_DC_TR	test point select
0x40			**PMU_RSVD1**	PMU Reserved Register 1
[31:24]	r	8'h0	RESERVE3	
[23:16]	rw	8'h0	RESERVE2	
[15:8]	rw	8'h0	RESERVE1	
[7:0]	rw	8'h0	RESERVE0	
0x44			**HXT_CR1**	HXT48 Control Register 1
[31:30]			RSVD	
[29:20]	rw	10'h1ca	CBANK_SEL	
[19]	rw	1'b1	GM_EN	
[18:17]	rw	2'h3	LDO_FLT_RSEL	

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表 3-1: PMUC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[16:13]	rw	4'ha	LDO_VREF	
[12:11]	rw	2'h1	BUF_RF_STR	
[10:9]	rw	2'h1	BUF_AUD_STR	
[8]	rw	1'b0	BUF_AUD_EN	
[7:6]	rw	2'h1	BUF_DLL_STR	
[5]	rw	1'b0	BUF_DLL_EN	
[4:3]	rw	2'h1	BUF_DIG_STR	
[2]	rw	1'b1	BUF_DIG_EN	
[1]	rw	1'b1	BUF_EN	
[0]	rw	1'b1	EN	
0x48			**HXT_CR2**	HXT48 Control Register 2
[31]	rw	1'b0	SLEEP_EN	
[30:29]	rw	2'h2	SDADC_CLKDIV2_SEL	
[28:27]	rw	2'h2	SDADC_CLKDIV1_SEL	
[26]	rw	1'b0	SDADC_CLKIN_EN	
[25:16]	rw	10'h32	IDAC	
[15]	rw	1'b0	IDAC_EN	
[14:13]	rw	2'h2	BUF_SEL3	
[12:11]	rw	2'h2	BUF_SEL2	
[10]	rw	1'h0	ACBUF_RSEL	
[9:8]	rw	2'h2	ACBUF_SEL	
[7:6]	rw	2'h1	AGC_VINDC	
[5:2]	rw	4'h8	AGC_VTH	
[1]	rw	1'b0	AGC_ISTART_SEL	
[0]	rw	1'b1	AGC_EN	
0x4C			**HXT_CR3**	HXT48 Control Register 3
[31]			RSVD	
[30:25]	rw	6'd31	DLY	
[24:23]	rw	2'h1	BUF_OSLO_STR	
[22:21]	rw	2'h1	BUF_DAC_STR	
[20:11]	rw	10'h32	OPT_IDAC	
[10]	rw	1'b0	OPT_IDAC_EN	
[9:0]	rw	10'h2da	OPT_CBANK_SEL	
0x50			**HRC_CR**	HRC48 Control Register
[31:24]			RSVD	
[23]	rw	1'b0	DLY	number of cycles for BG ready. 0 - one cycle of CLK_LP; 1 - two cycles of CLK_LP
[22:12]	rw	11'h400	CT	
[11]	rw	1'b0	MODE24M_EN	
[10:9]	rw	2'h1	BM	
[8:5]	rw	4'ha	LDO_VREF	
[4]	rw	1'b0	RST	
[3:2]	rw	2'h1	OUT_STR	
[1]	rw	1'b1	OUT_EN	
[0]	rw	1'b1	EN	
0x54			**RC1M_CR**	RC1M Control Register
[31:24]			RSVD	
[23]	rw	1'h0	RINGOSC_MODE	

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表 3-1: PMUC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[22:19]	rw	4'h4	RINGOSC_BM	
[18]	rw	1'h0	RINGOSC_EN	
[17]	rw	1'h0	SEL_SOURCE	
[16]	rw	1'h0	DLY	number of cycles for BG ready. 0 - one cycle of CLK_LP; 1 - two cycles of CLK_LP
[15:14]	rw	2'h1	RSEL	
[13:7]	rw	7'h27	CSEL	
[6:5]	rw	2'h1	BM_COMP	
[4:3]	rw	2'h1	BM_CHG	
[2]	rw	1'b0	RST	
[1]	rw	1'b0	OUT_EN	
[0]	rw	1'b0	EN	
0x58			**DBL96_CR**	DBL96 Control Register
[31:29]			RSVD	
[28:18]	rw	11'h1a6	DLY_SEL_EXT	
[17]	rw	1'b0	DLY_SEL_EXT_EN	
[16]	rw	1'b0	DLY_EXT_EN	
[15:12]	rw	4'h1	DLY_EN	
[11:8]	rw	4'b0	PH_EN	
[7]	rw	1'b0	LOOP_RSTB	
[6]	rw	1'b0	TOOSLO_EN	
[5]	rw	1'b0	TORF_EN	
[4:3]	rw	2'h1	TODIG_STR	
[2]	rw	1'b0	TODIG_EN	
[1]	rw	1'b0	OUT_EN	
[0]	rw	1'b0	EN	
0x5C			**DBL96_CALR**	DBL96 Calibration Register
[31:14]			RSVD	
[13]	r	1'h0	CAL_LOCK	
[12:2]	r	11'h0	CAL_OP	
[1]	rw	1'b0	CAL_CLOSE_EXT_EN	
[0]	rw	1'b0	CAL_EN	
0x60			**CAU_BGR**	CAU Bandgap Register
[31:11]			RSVD	
[10:7]	rw	4'ha	LPBG_VREF12	
[6:3]	rw	4'ha	LPBG_VREF06	
[2]	rw	1'b0	LPBG_EN	
[1]	rw	1'b0	HPBG_EN	
[0]	rw	1'b0	HPBG_VDDPSW_EN	
0x64			**CAU_TR**	CAU Test Register
[31:9]			RSVD	
[8:6]	rw	3'h0	CAU_DC_MR	
[5:3]	rw	3'h0	CAU_DC_BR	
[2:0]	rw	3'h0	CAU_DC_TR	
0x68			**CAU_RSVD**	CAU Reserved Register
[31:24]	r	8'h0	RESERVE3	
[23:16]	rw	8'h0	RESERVE2	
[15:8]	rw	8'h0	RESERVE1	

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表 3-1: PMUC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[7:0]	rw	8'h0	RESERVE0	
0x6C			**WKUP_CNT**	Wakeup Count Register
[31:16]	rw	16'hffff	PIN1_CNT	
[15:0]	rw	16'hffff	PIN0_CNT	

4 低功耗模式

4.1 简介

芯片支持多种低功耗模式，可满足不同场景下的低功耗需求。根据高性能处理器与低功耗处理器的任务分工，以及对功耗和唤醒时间的要求，可以将 HPSYS 和 LPSYS 分别配置为不同的低功耗模式，并配置各自独立的唤醒源，以达到功耗优化的目的。

4.2 主要工作模式汇总

芯片的主要工作模式见下表。除 active 模式外，其它模式均为低功耗模式。

表 4-1: 芯片工作模式

模式	子系统	CPU	外设	SRAM	IO	HP_AON LP_AON LPTIM	唤醒源	唤醒时间
Active		run	run	可访问	可翻转	run		
Sleep		stop	run	可访问	可翻转	run	任意中断	<1us
Deepsleep	HPSYS	stop	stop	不可访问，全保留	电平保持	run	RTC, 唤醒 PIN, IO(PA),LPTIM1, LPSYS, MAILBOX2	~250us
	LPSYS	stop	stop	不可访问，全保留	电平保持	run	RTC, 唤醒 PIN IO(PB),LPTIM2, HPSYS, MAILBOX1, 蓝牙,LPCOMP	~250us
Standby	HPSYS	reset	reset	不可访问，保留 64KB	电平保持	run	RTC, 唤醒 PIN, LPTIM1,LPSYS, MAILBOX2	~1.5ms
	LPSYS	reset	reset	不可访问，全保留	电平保持	run	RTC, 唤醒 PIN, 蓝牙,LPTIM2, HPSYS, MAILBOX1	~1.5ms
Hibernate		reset	reset	不可访问，不保留	高阻 (除唤醒 PIN)	reset	RTC, 唤醒 IO	>2ms

进入低功耗模式以后，子系统的时钟和供电可能关闭，部分模块的访问受到限制。

表 4-2: 低功耗模式下的访问权限

HPSYS	LPSYS	主控	HP_RAM MPI1~3	HP_AHB HP_APB	LP_RAM MPI5	LP_AHB LP_APB	PMUC RTC IWDT
active/sleep	active/sleep	HCPU/ACPU DMAC1/DMAC2	√	√	√	√	√
	deepsleep/standby		√	√	x	x	x
active/sleep	active/sleep	LCPU/DMAC3	√	√	√	√	√
deepsleep/standby			x	x	√	√	√

4.2.1 Active 模式

HPSYS 和 LPSYS 可独立处于 Active 模式。处于 Active 模式的子系统内 CPU 与外设正常运行，SRAM 可访问，IO 可正常翻转，资源可被其它子系统访问。为降低运行时的功耗，可以为 CPU 与外设选择合适的时钟源与时钟频率，并仅在外设工作时打开外设的模块使能。

所有低功耗模式仅能从 active 模式进入，并且退出时统一回到 active 模式。

4.2.2 Sleep 模式

HPSYS 和 LPSYS 可独立处于 Sleep 模式。处于 sleep 模式的子系统内 CPU 暂停执行指令，外设仍正常运行，SRAM 可访问，IO 可正常翻转，资源可被其它子系统访问。

HPSYS_AON 的 PMR_MODE 寄存器为 0 时，HCPU 执行 WFI 或 WFE 指令可使 HPSYS 进入 sleep 模式。HCPU 收到任何已使能的中断请求后退出 sleep 模式，从进入 sleep 模式之前的位置继续执行。

LPSYS_AON 的 PMR_MODE 寄存器为 0 时，LCPU 执行 WFI 或 WFE 指令可使 LPSYS 进入 sleep 模式。LCPU 收到任何已使能的中断请求后退出 sleep 模式，从进入 sleep 模式之前的位置继续执行。

4.2.3 Deepsleep 模式

HPSYS 子系统和 LPSYS 子系统可独立处于 deepsleep 模式。处于 deepsleep 模式的子系统大部分时钟均被关闭，仅保留低功耗时钟。CPU 与外设均停止运行。SRAM 不可访问，内容均可保留。配置为输出的 IO(除 PBR 外) 不可翻转，保持进入 deepsleep 模式之前的电平不变。其它子系统访问处于 deepsleep 模式的子系统时，会产生总线错误。

HPSYS 进入 deepsleep 模式的流程为：

1. 确保 HPSYS 各外设 (除 LPTIM1) 的工作任务已完成；
2. HCPU 处理完毕当前已上报的中断；
3. HCPU 通过 NVIC 寄存器关闭所有中断使能，避免产生 SysTick,SVCall 和 PendSV 等异常，并将 PRIMASK 置 1；
4. 时钟 clk_hpsys 切换到 clk_hrc48，关闭 clk_dll1/2/3 等高速时钟；
5. 在 HPSYS_AON 中设置唤醒源；
6. 将 HPSYS_AON 的 ISSR_HP_ACTIVE 置 0；
7. 将 HPSYS_AON 的 PMR_MODE 寄存器配置为 2；
8. HCPU 执行 WFI 指令。

LPSYS 进入 deepsleep 模式的流程为：

1. 确保 LPSYS 各外设 (除 LPTIM2/3) 的工作任务已完成；
2. LCPU 处理完毕当前已上报的中断；
3. LCPU 通过 NVIC 寄存器关闭所有中断使能，避免产生 SysTick,SVCall 和 PendSV 等异常，并将 PRIMASK 置 1；
4. 时钟 clk_lpsys 切换到 clk_hrc48，关闭 clk_dbl96 等高速时钟；
5. 在 LPSYS_AON 中设置唤醒源；
6. 将 LPSYS_AON 的 ISSR_LP_ACTIVE 置 0；
7. 将 LPSYS_AON 的 PMR_MODE 寄存器配置为 2；
8. LCPU 执行 WFI 指令。

上述流程执行之后，如果仍有中断未关闭而产生了中断或异常请求，本次进入 deepsleep 模式失败，CPU 会保留在 active 模式继续运行。如果发生这种情况，可以在处理完当前中断后重新尝试进入 deepsleep 模式。

为方便调试，在上述第 7 步向 PMR_MODE 寄存器写入 0x80000002，即可无视当前中断状态，强制进入 deepsleep 模式。

HPSYS 处于 deepsleep 模式时，包括 LCPU 在内的 LPSYS 所有主控模块对 HPSYS 任何地址空间 (包括 HPSYS_AON) 的访问都会返回总线错误。

LPSYS 处于 deepsleep 模式时，包括 HCPU 在内的 HPSYS 所有主控模块对 LPSYS 任何地址空间 (包括 LPSYS_AON)，以及对芯片低功耗域的任何地址空间 (如 PMUC,RTC,IWDT 等) 的访问都会返回总线错误。

HPSYS 处于 deepsleep 模式时，主要的唤醒源包括 RTC，唤醒 PIN，IO(PA)，LPTIM1，以及来自 LPSYS 的唤醒请求和 MAILBOX2。唤醒源通过 HPSYS_AON 的 WER 寄存器配置。

LPSYS 处于 deepsleep 模式时，主要的唤醒源包括 RTC，唤醒 PIN，IO(PB)，LPTIM2，蓝牙，LPCOMP，以及来自 HPSYS 的唤醒请求和 MAILBOX1。唤醒源通过 LPSYS_AON 的 WER 寄存器配置。

唤醒源生效时，子系统经过一段初始化时间 (约 250us) 后退出 deepsleep 模式，回到 active 模式。CPU，外设以及内存的状态均未丢失，CPU 从进入 deepsleep 模式之前的位置 (WFI 指令之后) 继续运行。

退出 deepsleep 模式时，子系统会产生 AON 中断。CPU 应首先运行相应恢复流程。

HPSYS 从 deepsleep 模式退出后，HCPU 的建议恢复流程为：

1. 将 HPSYS_AON 的 PMR_MODE 寄存器配置为 0；
2. 通过 NVIC 寄存器使能 AON 中断，并将 PRIMASK 置 0；
3. 在 AON 中断中，通过 HPSYS_AON 的 WSR 寄存器查询唤醒源并进行相应处理，并通过 HPSYS_AON 的 WCR 寄存器清除 AON 中断标志位；
4. 将 HPSYS_AON 的 ISSR_HP_ACTIVE 置 1；
5. 通过 NVIC 寄存器使能 HCPU 其它中断；
6. 如有需要，重新开启高速时钟。

LPSYS 从 deepsleep 模式退出后，LCPU 的建议恢复流程为：

1. 将 LPSYS_AON 的 PMR_MODE 寄存器配置为 0；
2. 通过 NVIC 寄存器使能 AON 中断，并将 PRIMASK 置 0；

3. 在 AON 中断中，通过 LPSYS_AON 的 WSR 寄存器查询唤醒源并进行相应处理，并通过 LPSYS_AON 的 WCR 寄存器清除 AON 中断标志位；
4. 将 LPSYS_AON 的 ISSR_LP_ACTIVE 置 1；
5. 通过 NVIC 寄存器使能 LCPU 其它中断；
6. 如有需要，重新开启高速时钟。

CPU 清除唤醒源标志时应当注意，只有 PIN 唤醒的标志是通过 HPSYS_AON 或 LPSYS_AON 的 WCR 寄存器清除，而其它唤醒源标志则需要配置产生唤醒源的对应模块来清除。

从 deepsleep 模式退出后，子系统时钟来自于 clk_hrc48，如果需要切换到其它时钟上，应当重新打开所需的时钟源。

从 deepsleep 模式退出后，子系统内各外设的寄存器内容不会被复位，各外设也保持进入 deepsleep 模式之前的状态

4.2.4 Standby 模式

HPSYS 和 LPSYS 可独立处于 standby 模式。处于 standby 模式的子系统内大部分时钟与供电均被关闭，仅保留低功耗模块的时钟与供电。CPU 与外设均被复位。SRAM 不可访问，HPSYS 可保留 128KB 的 DTCM 以及 16KB 专用备份存储，LPSYS 可保留全部 TCM 与 SRAM。配置为输出的 IO(除 PBR 外) 不可翻转，保持进入 standby 模式之前的电平不变。其它子系统访问处于 standby 模式的子系统时，会产生总线错误。

HPSYS 进入 standby 模式的流程为：

1. 确保 HPSYS 各外设 (除 LPTIM1) 的工作任务已完成；
2. 在 HPSYS 的 DTCM 或 PSRAM 中备份 SRAM 内容和外设状态；
3. HCPU 处理完毕当前已上报的中断；
4. HCPU 通过 NVIC 寄存器关闭所有中断使能，避免产生 SysTick,SVCall 和 PendSV 等异常，并将 PRIMASK 置 1；
5. 时钟 clk_hpsys 切换到 clk_hrc48；
6. 在 HPSYS_AON 中设置唤醒源；
7. 将 HPSYS_AON 的 ISSR_HP_ACTIVE 置 0；
8. 将 HPSYS_AON 的 ANACR 寄存器配置为 3；
9. 将 HPSYS_AON 的 PMR_MODE 寄存器配置为 3；
10. HCPU 执行 WFI 指令。

LPSYS 进入 standby 模式的流程为：

1. 确保 LPSYS 各外设 (除 LPTIM2/3) 的工作任务已完成；
2. 在 LPSYS 的 SRAM 中备份外设状态；
3. LCPU 处理完毕当前已上报的中断；
4. LCPU 通过 NVIC 寄存器关闭所有中断使能，避免产生 SysTick,SVCall 和 PendSV 等异常，并将 PRIMASK 置 1；
5. 时钟 clk_lpsys 切换到 clk_hrc48，关闭 clk_dbl96 等高速时钟；
6. 在 LPSYS_AON 中设置唤醒源；
7. 将 LPSYS_AON 的 ISSR_LP_ACTIVE 置 0；

8. 将 LPSYS_AON 的 ANACR 寄存器配置为 3；
9. 将 LPSYS_AON 的 PMR_MODE 寄存器配置为 3；
10. LCPU 执行 WFI 指令。

上述流程执行之后，如果仍有中断未关闭而产生了中断或异常请求，本次进入 standby 模式失败，CPU 会保留在 active 模式继续运行。如果发生这种情况，可以在处理完当前中断后重新尝试进入 standby 模式。

为方便调试，在上述第 9 步向 PMR_MODE 寄存器写入 0x80000003，即可无视当前中断状态，强制进入 standby 模式。

HPSYS 处于 standby 模式时，包括 LCPU 在内的 LPSYS 所有主控模块对 HPSYS 任何地址空间 (包括 HPSYS_AON) 的访问都会返回总线错误。

LPSYS 处于 standby 模式时，包括 HCPU 在内的 HPSYS 所有主控模块对 LPSYS 任何地址空间 (包括 LPSYS_AON)，以及对芯片低功耗域的任何地址空间 (如 PMUC,RTC,IWDT 等) 的访问都会返回总线错误。

HPSYS 处于 standby 模式时，主要的唤醒源包括 RTC，唤醒 PIN，LPTIM1，以及来自 LPSYS 的唤醒请求和 MAILBOX2。唤醒源通过 WER 寄存器配置。

LPSYS 处于 standby 模式时，主要的唤醒源包括 RTC，唤醒 PIN，LPTIM2，蓝牙，以及来自 HPSYS 的唤醒请求和 MAILBOX1。唤醒源通过 WER 寄存器配置。

唤醒源生效时，子系统经过一段初始化时间 (约 1.5ms) 后退出 standby 模式，回到 active 模式。CPU 和外设的状态均被复位，SRAM 部分保留，CPU 从 ROM 中的 0 地址开始运行，并查询 HPSYS_AON 或 LPSYS_AON 的 PMR_MODE 寄存器，选择不同的运行分支。

退出 standby 模式时，子系统会产生 AON 中断。CPU 从 ROM 程序中跳出后，应首先运行相应恢复流程。

HPSYS 从 standby 模式退出后，HCPU 的建议恢复流程为：

1. 将 HPSYS_AON 的 PMR_MODE 与 ANACR 寄存器配置为 0；
2. 通过 NVIC 寄存器使能 AON 中断；
3. 在 AON 中断中，通过 HPSYS_AON 的 WSR 寄存器查询唤醒源并进行相应处理，并通过 HPSYS_AON 的 WCR 寄存器清除 AON 中断标志位；
4. 将 HPSYS_AON 的 ISSR_HP_ACTIVE 置 1；
5. 重新开启高速时钟；
6. 从 HPSYS 的 DTCM 或 PSRAM 中恢复外设配置和 SRAM 内容；
7. 通过 NVIC 寄存器使能 HCPU 其它中断。

LPSYS 从 standby 模式退出后，LCPU 的建议恢复流程为：

1. 将 LPSYS_AON 的 PMR_MODE 与 ANACR 寄存器配置为 0；
2. 通过 NVIC 寄存器使能 AON 中断；
3. 在 AON 中断中，通过 LPSYS_AON 的 WSR 寄存器查询唤醒源并进行相应处理，并通过 LPSYS_AON 的 WCR 寄存器清除 AON 中断标志位；
4. 将 LPSYS_AON 的 ISSR_LP_ACTIVE 置 1；
5. 如有需要，重新开启高速时钟；
6. 从 LPSYS 的 SRAM 中恢复外设配置；
7. 通过 NVIC 寄存器使能 LCPU 其它中断。

CPU 清除唤醒源标志时应当注意，只有 PIN 唤醒的标志是通过 HPSYS_AON 或 LPSYS_AON 的 WCR 寄存器清除，而其它唤醒源标志则需要配置产生唤醒源的对应模块来清除。

从 standby 模式退出后，子系统的系统时钟来自于 clk_hrc48，如果需要切换到其它时钟上，应当重新打开所需的时钟源。

从 standby 模式退出后，除低功耗外设 (如 LPTIM) 外，子系统内各外设均被复位，使用前应当恢复配置或重新初始化。外设状态可以在进入 standby 模式之前备份在具有 retention 功能的 SRAM 或 PSRAM 中，备份的内容在进出 standby 模式后不会被清除。

4.2.5 Hibernate 模式

Hibernate 模式是芯片的最低功耗模式。该模式下芯片大部分时钟与供电均被关闭，仅保留部分低功耗模块的时钟与供电。CPU，外设，HPSYS(包括 HPSYS_AON)，LPSYS(包括 LPSYS_AON) 所有寄存器均被复位。所有 SRAM 内容不保留。不支持唤醒 PIN 功能的 IO 进入高阻状态。

进入 hibernate 模式的流程为：

1. 在 PMUC 的 WER 寄存器中设置唤醒源；
2. 将 PMUC 的 CR_HIBER_EN 置 1。

进入 hibernate 模式后，仅有 PMUC，RTC 和 IWDT 模块在工作，这些模块的寄存器不会丢失。

Hibernate 模式的唤醒源包括 RTC 和唤醒 PIN。支持唤醒 PIN 功能的 IO 仍可保持上下拉电阻生效 (配置位于 RTC 寄存器，因此不会丢失)。

唤醒源生效时，芯片经过一段初始化时间 (>2ms) 后退出 hibernate 模式，回到 active 模式。HCPU 从 ROM 中的 0 地址开始运行。此时 PMUC 的 CR_HIBER_EN 寄存器仍然为 1，CPU 可据此获知此次启动是从 hibernate 模式退出，可进行相应处理并将 CR_HIBER_EN 清 0。

从 hibernate 模式退出后，子系统的系统时钟来自于 clk_hrc48，如果需要切换到其它时钟上，应当重新打开所需的时钟源。

从 hibernate 模式退出后，除 PMUC，RTC 和 IWDT 外，其它模块均被复位，使用前应当重新初始化。

4.2.6 跨系统访问方法

HPSYS 子系统与 LPSYS 子系统可各自独立进入总线被禁止访问的 deepsleep 或 standby 低功耗模式，因此在互相访问时必须遵循特定方法。其中被访问方应当设置总线保护机制，而访问发起方应当遵循预唤醒流程。

被访问方子系统进出低功耗模式时应设置总线保护机制。具体而言，HPSYS 进入 deepsleep 或 standby 模式时，HCPU 应将 HPSYS_AON 的 ISSR_HP_ACTIVE 置为 0，此后包括 LCPU 在内的 LPSYS 所有主控模块对 HPSYS 任何地址空间 (包括 HPSYS_AON) 的访问都会返回总线错误，只有当 HPSYS 从低功耗模式退出，并且将 ISSR_HP_ACTIVE 置为 1 后才能正常访问。LPSYS 进入 deepsleep 或 standby 模式时，LCPU 应将 LPSYS_AON 的 ISSR_LP_ACTIVE 置为 0，此后 HCPU 对 LPSYS 任何地址空间 (包括 LPSYS_AON)，以及对芯片低功耗域的任何地址空间 (如 PMUC,RTC,IWDT 等) 的访问都会返回总线错误，只有当 LPSYS 从低功耗模式恢复，并且将 ISSR_LP_ACTIVE 置为 1 后才能正常访问。这种总线错误体现为 CPU 的 HardFault 异常。如果不设置上述总线保护机制，当主控模块进行不适当的跨系统访问时，可能出现总线数据错误或总线卡死等无法恢复的异常情况。

为支持预唤醒机制，被访问方还应预先使能跨系统唤醒源，即将 HPSYS_AON 的 WER_LP2HP_REQ 和 LPSYS_AON 的 WER_HP2LP_REQ 置 1。

子系统在发起跨系统访问时，应当遵循预唤醒流程。一个例外是，当芯片上电启动或从 hibernate 模式退出以后，HPSYS 子系统与 LPSYS 子系统均处于 active 模式，此时互相访问地址空间是允许的。除此以外，一旦被访问子系统的 CPU 程序配置了低功耗模式，跨系统的访问前均应当进行预唤醒。

HCPU 访问 LPSYS 子系统以及低功耗域 (如 PMUC,RTC,IWDT 等) 的预唤醒流程如下：

1. 将 HPSYS_AON 的 ISSR_HP2LP_REQ 置 1；
2. 等待 1ms；
3. 检查 HPSYS_AON 的 ISSR_LP_ACTIVE，如果为 1 进入步骤 4，否则重复步骤 2 3；
4. 开始访问 LPSYS 或低功耗域，访问时间及次数不受限，此时 LPSYS 不会进入 deepsleep 或 standby 模式；
5. 访问结束后，将 HPSYS_AON 的 ISSR_HP2LP_REQ 置 0，允许 LPSYS 进入 deepsleep 或 standby 模式

LCPU 访问 HPSYS 子系统的预唤醒流程如下：

1. 将 LPSYS_AON 的 ISSR_LP2HP_REQ 置 1；
2. 等待 1ms；
3. 检查 LPSYS_AON 的 ISSR_HP_ACTIVE，如果为 1 进入步骤 4，否则重复步骤 2 3；
4. 开始访问 HPSYS 子系统，访问时间及次数不受限，此时 HPSYS 不会进入 deepsleep 或 standby 模式；
5. 访问结束后，将 LPSYS_AON 的 ISSR_LP2HP_REQ 置 0，允许 HPSYS 进入 deepsleep 或 standby 模式。

4.2.7 跨系统数据交互方法

HPSYS 子系统与 LPSYS 子系统进行数据交互时，除通过预唤醒流程访问以外，还可采用基于 MAILBOX 的跨系统数据交互机制。

为支持跨系统数据交互机制，被访问方应预先使能 MAILBOX 唤醒源，即将 HPSYS_AON 的 WER_LP2HP_IRQ 和 LPSYS_AON 的 WER_HP2LP_IRQ 置 1。

跨系统数据交互流程如下：

1. 访问方准备数据信令，保存在本系统的 SRAM 中；
2. 访问方配置本系统的 MAILBOX 模块，由 MAILBOX 发出跨系统唤醒信号，随后可进入 sleep 模式；
3. 被访问方收到 MAILBOX 中断后，从访问方的 SRAM 中获取数据信令；
4. 被访问方解析信令内容，从访问方 SRAM 中读取数据或向访问方 SRAM 中写入数据，并写入数据完成标志，之后可重新进入低功耗模式；
5. 访问方监测到数据完成标志，结束访问。

4.2.8 低功耗模式下的调试器行为

芯片进入低功耗模式以后，调试难度增加，最主要的表现是调试器断开或无法连接。调试器默认通过 PB13 和 PB15 两个 IO 连接到 HCPU 上，当 LPSYS_AON 的寄存器 PMR_FORCE_LCPU 置 1 时切换连接到 LCPU 上。当芯片发生重启或从 hibernate 模式退出，使得 LPSYS_AON 的寄存器复位后，调试器会重新连接到 HCPU 上。

调试器连接 HCPU 时，出现如下情况会断开且无法重新连接：

1. 调试器切换到 LCPU 上；

2. PB13 或 PB15 的 IO 功能被更改；
3. LPSYS 处于 deepsleep 或 standby 模式；
4. LPSYS_AON 的 ANACR_PB_ISO 寄存器为 1(LPSYS 进入低功耗模式时由 LCPU 配置)；
5. HPSYS 处于 deepsleep 或 standby 模式；
6. 芯片处于 hibernate 模式。

在调试 HCPU 时，为避免 LPSYS 进出低功耗模式时影响调试器，建议 LPSYS 维持在 active 或 sleep 模式。HPSYS 从 deepsleep 或 standby 模式唤醒，并且 HPSYS_AON 的 ISSR_HP_ACTIVE 置 1 以后，调试器可以重新连接 HCPU 并访问 HPSYS 地址空间。

调试器连接 LCPU 时，出现如下情况会断开且无法重新连接：

1. 调试器切换到 HCPU 上；
2. PB13 或 PB15 的 IO 功能被更改；
3. LPSYS 处于 deepsleep 或 standby 模式；
4. LPSYS_AON 的 ANACR_PB_ISO 寄存器为 1(LPSYS 进入低功耗模式时由 LCPU 配置)；
5. 芯片处于 hibernate 模式。

LPSYS 从 deepsleep 或 standby 模式唤醒，并且 LPSYS_AON 的 ANACR_PB_ISO 置 0，ISSR_LP_ACTIVE 置 1 以后，调试器可以重新连接 LCPU 并访问 LPSYS 地址空间。

4.2.9 判断当前低功耗模式

通过测量芯片的电源管脚电压，可以判断当前处于何种低功耗模式。当 HPSYS 处于 active，sleep 或 deepsleep 模式时，LDO1_VOUT 电压保持 1.1V。当 HPSYS 处于 standby 模式时，LDO1_VOUT 电压无法保持，会逐渐下降到 0V。当 LPSYS 处于 active，sleep 或 deepsleep 模式时，LDO2_VOUT 电压保持 0.9V(基础模式) 或 1.1V(增强模式)。当 LPSYS 处于 standby 模式时，LDO2_VOUT 电压无法保持，会逐渐下降到 0V。当芯片进入 hibernate 模式时，LDO1_VOUT，LDO2_VOUT 和 VDD_RET 都下降到 0V。

表 4-3: 低功耗模式下的电源管脚电压

HPSYS	LPSYS	LDO1_VOUT	LDO2_VOUT	VDD_RET	VDD_RTC
active/sleep/deepsleep	active/sleep/deepsleep	1.1V	0.9V/1.1V	0.7V	1.1V
	standby	1.1V	0V	0.7V	1.1V
standby	active/sleep/deepsleep	0V	0.9V/1.1V	0.7V	1.1V
	standby	0V	0V	0.7V	1.1V
hibernate		0V	0V	0V	1.1V
power off		0V	0V	0V	0V

4.3 HPSYS_AON 寄存器

表 4-4: HPSYS_AON 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00			**PMR**	Power Mode Register
[31]	w1s	1'b0	FORCE_SLEEP	Set 1 to force enter low power mode. Will be cleared automatically
[30]	rw	1'b0	FORCE_HCPU	for debug only
[29:2]			RSVD	
[1:0]	rw	2'h0	MODE	Power Mode: 2'h0 - active; 2'h1 - light sleep; 2'h2 - deep sleep; 2'h3 - standby
0x04			**CR1**	Control Register 1
[31]	rw	1'h0	GTIM_EN	Enable global timer
[30:24]			RSVD	
[23:21]	rw	3'h0	PIN7_MODE	mode for wakeup PIN7 (PA52)
[20:18]	rw	3'h0	PIN6_MODE	mode for wakeup PIN6 (PA51)
[17:15]	rw	3'h0	PIN5_MODE	mode for wakeup PIN5 (PA50)
[14:12]	rw	3'h0	PIN4_MODE	mode for wakeup PIN4 (PB36)
[11:9]	rw	3'h0	PIN3_MODE	mode for wakeup PIN3 (PB35)
[8:6]	rw	3'h0	PIN2_MODE	mode for wakeup PIN2 (PB34)
[5:3]	rw	3'h0	PIN1_MODE	mode for wakeup PIN1 (PB33)
[2:0]	rw	3'h0	PIN0_MODE	mode for wakeup PIN0 (PB32) 0 - high level, 1 - low level, 2 - pos edge, 3 - neg edge, 4/5/6/7: pos or neg edge
0x08			**CR2**	Control Register 2
[31:18]			RSVD	
[17:15]	rw	3'h0	PIN13_MODE	mode for wakeup PIN13 (PBR3)
[14:12]	rw	3'h0	PIN12_MODE	mode for wakeup PIN12 (PBR2)
[11:9]	rw	3'h0	PIN11_MODE	mode for wakeup PIN11 (PBR1)
[8:6]	rw	3'h0	PIN10_MODE	mode for wakeup PIN10 (PBR0)
[5:3]	rw	3'h0	PIN9_MODE	mode for wakeup PIN9 (PA54)
[2:0]	rw	3'h0	PIN8_MODE	mode for wakeup PIN8 (PA53) 0 - high level, 1 - low level, 2 - pos edge, 3 - neg edge, 4/5/6/7: pos or neg edge
0x0C			**ACR**	Active Mode Control register
[31]	r	1'b0	HXT48_RDY	Indicate hxt48 is ready
[30]	r	1'b0	HRC48_RDY	Indicate hrc48 is ready
[29:6]			RSVD	
[5]	rw	1'b0	DS_ULPMEM	for debug only
[4]	rw	1'b0	PD_LPMEM	for debug only
[3]	rw	1'b0	EXTPWR_REQ	Request power for LPSYS during Active mode
[2]	rw	1'b1	PWR_REQ	Request power for HPSYS during Active mode
[1]	rw	1'b1	HXT48_REQ	Request hxt48 in active mode
[0]	rw	1'b1	HRC48_REQ	Request hrc48 in active mode
0x10			**LSCR**	Light Sleep Ctrl Register
[31:4]			RSVD	
[3]	rw	1'b0	EXTPWR_REQ	Request power for LPSYS during Light Sleep mode
[2]	rw	1'b1	PWR_REQ	Request power for HPSYS during Light Sleep mode
[1]	rw	1'b1	HXT48_REQ	Request hxt48 in Light Sleep mode
[0]	rw	1'b1	HRC48_REQ	Request hrc48 in Light Sleep mode
0x14			**DSCR**	Deep Sleep Ctrl Register
[31:4]			RSVD	
[3]	rw	1'b0	EXTPWR_REQ	Request power for LPSYS during Deep Sleep mode

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表 4-4: HPSYS_AON 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[2]	rw	1'b1	PWR_REQ	Request power for HPSYS during Deep Sleep mode
[1]	rw	1'b0	HXT48_REQ	Request hxt48 in Deep Sleep mode
[0]	rw	1'b0	HRC48_REQ	Request hrc48 in Deep Sleep mode
0x18			**SBCR**	Standby Mode Ctrl Register
[31:4]			RSVD	
[3]	rw	1'b0	EXTPWR_REQ	Request power for LPSYS during Standby mode
[2]	rw	1'b0	PWR_REQ	Request power for HPSYS during Standby mode
[1]	rw	1'b0	HXT48_REQ	Request hxt48 in Standby mode
[0]	rw	1'b0	HRC48_REQ	Request hrc48 in Standby mode
0x1C			**WER**	Wakeup Enable register
[31:22]			RSVD	
[21]	rw	1'b0	PIN13	Set 1 to enable PBR3 as wakeup source
[20]	rw	1'b0	PIN12	Set 1 to enable PBR2 as wakeup source
[19]	rw	1'b0	PIN11	Set 1 to enable PBR1 as wakeup source
[18]	rw	1'b0	PIN10	Set 1 to enable PBR0 as wakeup source
[17]	rw	1'b0	PIN9	Set 1 to enable PA54 as wakeup source
[16]	rw	1'b0	PIN8	Set 1 to enable PA53 as wakeup source
[15]	rw	1'b0	PIN7	Set 1 to enable PA52 as wakeup source
[14]	rw	1'b0	PIN6	Set 1 to enable PA51 as wakeup source
[13]	rw	1'b0	PIN5	Set 1 to enable PA50 as wakeup source
[12]	rw	1'b0	PIN4	Set 1 to enable PB36 as wakeup source
[11]	rw	1'b0	PIN3	Set 1 to enable PB35 as wakeup source
[10]	rw	1'b0	PIN2	Set 1 to enable PB34 as wakeup source
[9]	rw	1'b0	PIN1	Set 1 to enable PB33 as wakeup source
[8]	rw	1'b0	PIN0	Set 1 to enable PB32 as wakeup source
[7]	rw	1'b0	LP2HP_IRQ	Set 1 to enable MAILBOX2 as wakeup source
[6]	rw	1'b0	LP2HP_REQ	Set 1 to enable LPSYS request as wakeup source
[5:3]			RSVD	
[2]	rw	1'b0	LPTIM1	Set 1 to enable LPTIM1 as wakeup source
[1]	rw	1'b0	GPIO1	Set 1 to enable IO(PA) as wakeup source
[0]	rw	1'b0	RTC	Set 1 to enable RTC as wakeup source
0x20			**WSR**	Wakeup Status register
[31:22]			RSVD	
[21]	r	1'b0	PIN13	Indicates the wakeup status from PBR3 request. Note: the status is masked by WER
[20]	r	1'b0	PIN12	Indicates the wakeup status from PBR2 request. Note: the status is masked by WER
[19]	r	1'b0	PIN11	Indicates the wakeup status from PBR1 request. Note: the status is masked by WER
[18]	r	1'b0	PIN10	Indicates the wakeup status from PBR0 request. Note: the status is masked by WER
[17]	r	1'b0	PIN9	Indicates the wakeup status from PA54 request. Note: the status is masked by WER
[16]	r	1'b0	PIN8	Indicates the wakeup status from PA53 request. Note: the status is masked by WER
[15]	r	1'b0	PIN7	Indicates the wakeup status from PA52 request. Note: the status is masked by WER

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表 4-4: HPSYS_AON 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[14]	r	1'b0	PIN6	Indicates the wakeup status from PA51 request. Note: the status is masked by WER
[13]	r	1'b0	PIN5	Indicates the wakeup status from PA50 request. Note: the status is masked by WER
[12]	r	1'b0	PIN4	Indicates the wakeup status from PB36 request. Note: the status is masked by WER
[11]	r	1'b0	PIN3	Indicates the wakeup status from PB35 request. Note: the status is masked by WER
[10]	r	1'b0	PIN2	Indicates the wakeup status from PB34 request. Note: the status is masked by WER
[9]	r	1'b0	PIN1	Indicates the wakeup status from PB33 request. Note: the status is masked by WER
[8]	r	1'b0	PIN0	Indicates the wakeup status from PB32 request. Note: the status is masked by WER
[7]	r	1'b0	LP2HP_IRQ	Indicates the wakeup status from MAILBOX2. Note: the status is masked by WER
[6]	r	1'b0	LP2HP_REQ	Indicates the wakeup status from LPSYS request. Note: the status is masked by WER
[5:3]			RSVD	
[2]	r	1'b0	LPTIM1	Indicates the wakeup status from LPTIM1. Note: the status is masked by WER
[1]	r	1'b0	GPIO1	Indicates the wakeup status from IO(PA). Note: the status is masked by WER
[0]	r	1'b0	RTC	Indicates the wakeup status from RTC. Note: the status is masked by WER
0x24			**WCR**	Wakeup Clear register
[31]	w1c	1'b0	AON	Write 1 to clear the AON wakeup IRQ status
[30:22]			RSVD	
[21]	w1c	1'b0	PIN13	Write 1 to clear PBR3 wakeup source. Only valid if PIN wakeup is configured as edge trigger
[20]	w1c	1'b0	PIN12	Write 1 to clear PBR2 wakeup source. Only valid if PIN wakeup is configured as edge trigger
[19]	w1c	1'b0	PIN11	Write 1 to clear PBR1 wakeup source. Only valid if PIN wakeup is configured as edge trigger
[18]	w1c	1'b0	PIN10	Write 1 to clear PBR0 wakeup source. Only valid if PIN wakeup is configured as edge trigger
[17]	w1c	1'b0	PIN9	Write 1 to clear PA54 wakeup source. Only valid if PIN wakeup is configured as edge trigger
[16]	w1c	1'b0	PIN8	Write 1 to clear PA53 wakeup source. Only valid if PIN wakeup is configured as edge trigger
[15]	w1c	1'b0	PIN7	Write 1 to clear PA52 wakeup source. Only valid if PIN wakeup is configured as edge trigger
[14]	w1c	1'b0	PIN6	Write 1 to clear PA51 wakeup source. Only valid if PIN wakeup is configured as edge trigger
[13]	w1c	1'b0	PIN5	Write 1 to clear PA50 wakeup source. Only valid if PIN wakeup is configured as edge trigger
[12]	w1c	1'b0	PIN4	Write 1 to clear PB36 wakeup source. Only valid if PIN wakeup is configured as edge trigger
[11]	w1c	1'b0	PIN3	Write 1 to clear PB35 wakeup source. Only valid if PIN wakeup is configured as edge trigger
[10]	w1c	1'b0	PIN2	Write 1 to clear PB34 wakeup source. Only valid if PIN wakeup is configured as edge trigger

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表 4-4: HPSYS_AON 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[9]	w1c	1'b0	PIN1	Write 1 to clear PB33 wakeup source. Only valid if PIN wakeup is configured as edge trigger
[8]	w1c	1'b0	PIN0	Write 1 to clear PB32 wakeup source. Only valid if PIN wakeup is configured as edge trigger
[7:0]			RSVD	
0x28			**ISSR**	Inter System Wakeup Register
[31:6]			RSVD	
[5]	r	1'h1	LP_ACTIVE	read 1 indicates LPSYS is active
[4]	rw	1'h1	HP_ACTIVE	write 1 to indicates HPSYS is active
[3:2]			RSVD	
[1]	r	1'b0	LP2HP_REQ	indicate LPSYS request exists
[0]	rw	1'b0	HP2LP_REQ	write 1 to request LPSYS to stay in active mode
0x2C			**ANACR**	Analog Control Register
[31:2]			RSVD	
[1]	rw	1'b0	VHP_ISO	Set 1 to force off all HPSYS related analog modules
[0]	rw	1'b0	PA_ISO	Set 1 to force IO(PA) into retention mode
0x30			**GTIMR**	Global Timer Register
[31:0]	r	32'h0	CNT	Global timer value
0x34			**RESERVE0**	Reserved Register 0
[31:0]	rw	32'b0	DATA	for debug only
0x38			**RESERVE1**	Reserved Register 1
[31:0]	rw	32'b0	DATA	for debug only

4.4 LPSYS_AON 寄存器

表 4-5: LPSYS_AON 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00			**PMR**	Power Mode Register
[31]	w1s	1'b0	FORCE_SLEEP	Set 1 to force enter low power mode. Will be cleared automatically
[30]	rw	1'b0	FORCE_LCPU	0: SWD connected to HCPU 1: SWD connected to LCPU
[29:3]			RSVD	
[2]	rw	1'b1	CPUWAIT	Stall CPU out of reset. Should be cleared before LCPU run
[1:0]	rw	2'h0	MODE	Power Mode: 2'h0 - active; 2'h1 - light sleep; 2'h2 - deep sleep; 2'h3 - standby
0x04			**CR1**	Control Register 1
[31]	rw	1'h0	GTIM_EN	Enable global timer
[30:28]	rw	3'h0	PBR_SEL1	for debug only
[27:25]	rw	3'h0	PBR_SEL0	for debug only
[24]			RSVD	
[23:21]	rw	3'h0	PIN7_MODE	mode for wakeup PIN7 (PA52)
[20:18]	rw	3'h0	PIN6_MODE	mode for wakeup PIN6 (PA51)
[17:15]	rw	3'h0	PIN5_MODE	mode for wakeup PIN5 (PA50)
[14:12]	rw	3'h0	PIN4_MODE	mode for wakeup PIN4 (PB36)
[11:9]	rw	3'h0	PIN3_MODE	mode for wakeup PIN3 (PB35)
[8:6]	rw	3'h0	PIN2_MODE	mode for wakeup PIN2 (PB34)
[5:3]	rw	3'h0	PIN1_MODE	mode for wakeup PIN1 (PB33)

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表 4-5: LPSYS_AON 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[2:0]	rw	3'h0	PIN0_MODE	mode for wakeup PIN0 (PB32) 0 - high level, 1 - low level, 2 - pos edge, 3 - neg edge, 4/5/6/7: pos or neg edge
0x08			**CR2**	Control Register 2
[31:18]			RSVD	
[17:15]	rw	3'h0	PIN13_MODE	mode for wakeup PIN13 (PBR3)
[14:12]	rw	3'h0	PIN12_MODE	mode for wakeup PIN12 (PBR2)
[11:9]	rw	3'h0	PIN11_MODE	mode for wakeup PIN11 (PBR1)
[8:6]	rw	3'h0	PIN10_MODE	mode for wakeup PIN10 (PBR0)
[5:3]	rw	3'h0	PIN9_MODE	mode for wakeup PIN9 (PA54)
[2:0]	rw	3'h0	PIN8_MODE	mode for wakeup PIN8 (PA53) 0 - high level, 1 - low level, 2 - pos edge, 3 - neg edge, 4/5/6/7: pos or neg edge
0x0C			**ACR**	Active Mode Control register
[31]	r	1'b0	HXT48_RDY	Indicate hxt48 is ready
[30]	r	1'b0	HRC48_RDY	Indicate hrc48 is ready
[29:11]			RSVD	
[10]	rw	1'b0	DS_DTCM	for debug only
[9]	rw	1'b0	DS_ITCM	for debug only
[8]	rw	1'b0	DS_RAM2	for debug only
[7]	rw	1'b0	DS_RAM1	for debug only
[6]	rw	1'b0	DS_RAM0	for debug only
[5]			RSVD	
[4]	rw	1'b0	EXTPWR_REQ	Request power for HPSYS during Active mode
[3]	rw	1'b1	PWR_REQ	Request power for LPSYS during Active mode
[2]	rw	1'b1	HXT48_REQ	Request hxt48 in active mode
[1]	rw	1'b1	HRC48_REQ	Request hrc48 in active mode
[0]			RSVD	
0x10			**LSCR**	Light Sleep Ctrl Register
[31:5]			RSVD	
[4]	rw	1'b0	EXTPWR_REQ	Request power for HPSYS during Light Sleep mode
[3]	rw	1'b1	PWR_REQ	Request power for LPSYS during Light Sleep mode
[2]	rw	1'b1	HXT48_REQ	Request hxt48 in Light Sleep mode
[1]	rw	1'b1	HRC48_REQ	Request hrc48 in Light Sleep mode
[0]			RSVD	
0x14			**DSCR**	Deep Sleep Ctrl Register
[31:5]			RSVD	
[4]	rw	1'b0	EXTPWR_REQ	Request power for HPSYS during Deep Sleep mode
[3]	rw	1'b0	PWR_REQ	Request power for LPSYS during Deep Sleep mode
[2]	rw	1'b0	HXT48_REQ	Request hxt48 in Deep Sleep mode
[1]	rw	1'b0	HRC48_REQ	Request hrc48 in Deep Sleep mode
[0]			RSVD	
0x18			**SBCR**	Standby Mode Ctrl Register
[31:11]			RSVD	
[10]	rw	1'h0	PD_DTCM	for debug only
[9]	rw	1'h0	PD_ITCM	for debug only
[8]	rw	1'h0	PD_RAM2	for debug only
[7]	rw	1'h0	PD_RAM1	for debug only
[6]	rw	1'h0	PD_RAM0	for debug only
[5]			RSVD	

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表 4-5: LPSYS_AON 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[4]	rw	1'b0	EXTPWR_REQ	Request power for HPSYS during Standby mode
[3]	rw	1'b0	PWR_REQ	Request power for LPSYS during Standby mode
[2]	rw	1'b0	HXT48_REQ	Request hxt48 in Standby mode
[1]	rw	1'b0	HRC48_REQ	Request hrc48 in Standby mode
[0]			RSVD	
0x1C			**WER**	Wakeup Enable register
[31:22]			RSVD	
[21]	rw	1'b0	PIN13	Set 1 to enable PBR3 as wakeup source
[20]	rw	1'b0	PIN12	Set 1 to enable PBR2 as wakeup source
[19]	rw	1'b0	PIN11	Set 1 to enable PBR1 as wakeup source
[18]	rw	1'b0	PIN10	Set 1 to enable PBR0 as wakeup source
[17]	rw	1'b0	PIN9	Set 1 to enable PA54 as wakeup source
[16]	rw	1'b0	PIN8	Set 1 to enable PA53 as wakeup source
[15]	rw	1'b0	PIN7	Set 1 to enable PA52 as wakeup source
[14]	rw	1'b0	PIN6	Set 1 to enable PA51 as wakeup source
[13]	rw	1'b0	PIN5	Set 1 to enable PA50 as wakeup source
[12]	rw	1'b0	PIN4	Set 1 to enable PB36 as wakeup source
[11]	rw	1'b0	PIN3	Set 1 to enable PB35 as wakeup source
[10]	rw	1'b0	PIN2	Set 1 to enable PB34 as wakeup source
[9]	rw	1'b0	PIN1	Set 1 to enable PB33 as wakeup source
[8]	rw	1'b0	PIN0	Set 1 to enable PB32 as wakeup source
[7]	rw	1'b0	HP2LP_IRQ	Set 1 to enable MAILBOX1 as wakeup source
[6]	rw	1'b0	HP2LP_REQ	Set 1 to enable HPSYS request as wakeup source
[5]	rw	1'b0	BT	Set 1 to enable BT as wakeup source
[4]	rw	1'b0	LPCOMP2	Set 1 to enable LPCOMP2 as wakeup source
[3]	rw	1'b0	LPCOMP1	Set 1 to enable LPCOMP1 as wakeup source
[2]	rw	1'b0	LPTIM2	Set 1 to enable LPTIM2 as wakeup source
[1]	rw	1'b0	GPIO2	Set 1 to enable IO(PB) as wakeup source
[0]	rw	1'b0	RTC	Set 1 to enable RTC as wakeup source
0x20			**WSR**	Wakeup Status register
[31:22]			RSVD	
[21]	r	1'b0	PIN13	Indicates the wakeup status from PBR3 request. Note: the status is masked by WER
[20]	r	1'b0	PIN12	Indicates the wakeup status from PBR2 request. Note: the status is masked by WER
[19]	r	1'b0	PIN11	Indicates the wakeup status from PBR1 request. Note: the status is masked by WER
[18]	r	1'b0	PIN10	Indicates the wakeup status from PBR0 request. Note: the status is masked by WER
[17]	r	1'b0	PIN9	Indicates the wakeup status from PA54 request. Note: the status is masked by WER
[16]	r	1'b0	PIN8	Indicates the wakeup status from PA53 request. Note: the status is masked by WER
[15]	r	1'b0	PIN7	Indicates the wakeup status from PA52 request. Note: the status is masked by WER
[14]	r	1'b0	PIN6	Indicates the wakeup status from PA51 request. Note: the status is masked by WER

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表 4-5: LPSYS_AON 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[13]	r	1'b0	PIN5	Indicates the wakeup status from PA50 request. Note: the status is masked by WER
[12]	r	1'b0	PIN4	Indicates the wakeup status from PB36 request. Note: the status is masked by WER
[11]	r	1'b0	PIN3	Indicates the wakeup status from PB35 request. Note: the status is masked by WER
[10]	r	1'b0	PIN2	Indicates the wakeup status from PB34 request. Note: the status is masked by WER
[9]	r	1'b0	PIN1	Indicates the wakeup status from PB33 request. Note: the status is masked by WER
[8]	r	1'b0	PIN0	Indicates the wakeup status from PB32 request. Note: the status is masked by WER
[7]	r	1'b0	HP2LP_IRQ	Indicates the wakeup status from MAILBOX1. Note: the status is masked by WER
[6]	r	1'b0	HP2LP_REQ	Indicates the wakeup status from HPSYS request. Note: the status is masked by WER
[5]	r	1'b0	BT	Indicates the wakeup status from BT. Note: the status is masked by WER
[4]	r	1'b0	LPCOMP2	Indicates the wakeup status from LPCOMP2. Note: the status is masked by WER
[3]	r	1'b0	LPCOMP1	Indicates the wakeup status from LPCOMP1. Note: the status is masked by WER
[2]	r	1'b0	LPTIM2	Indicates the wakeup status from LPTIM2. Note: the status is masked by WER
[1]	r	1'b0	GPIO2	Indicates the wakeup status from IO(PB). Note: the status is masked by WER
[0]	r	1'b0	RTC	Indicates the wakeup status from RTC. Note: the status is masked by WER
0x24			**WCR**	Wakeup Clear register
[31]	w1c	1'b0	AON	Write 1 to clear the AON wakeup IRQ status
[30:22]			RSVD	
[21]	w1c	1'b0	PIN13	Write 1 to clear PBR3 wakeup source. Only valid if PIN wakeup is configured as edge trigger
[20]	w1c	1'b0	PIN12	Write 1 to clear PBR2 wakeup source. Only valid if PIN wakeup is configured as edge trigger
[19]	w1c	1'b0	PIN11	Write 1 to clear PBR1 wakeup source. Only valid if PIN wakeup is configured as edge trigger
[18]	w1c	1'b0	PIN10	Write 1 to clear PBR0 wakeup source. Only valid if PIN wakeup is configured as edge trigger
[17]	w1c	1'b0	PIN9	Write 1 to clear PA54 wakeup source. Only valid if PIN wakeup is configured as edge trigger
[16]	w1c	1'b0	PIN8	Write 1 to clear PA53 wakeup source. Only valid if PIN wakeup is configured as edge trigger
[15]	w1c	1'b0	PIN7	Write 1 to clear PA52 wakeup source. Only valid if PIN wakeup is configured as edge trigger
[14]	w1c	1'b0	PIN6	Write 1 to clear PA51 wakeup source. Only valid if PIN wakeup is configured as edge trigger
[13]	w1c	1'b0	PIN5	Write 1 to clear PA50 wakeup source. Only valid if PIN wakeup is configured as edge trigger
[12]	w1c	1'b0	PIN4	Write 1 to clear PB36 wakeup source. Only valid if PIN wakeup is configured as edge trigger
[11]	w1c	1'b0	PIN3	Write 1 to clear PB35 wakeup source. Only valid if PIN wakeup is configured as edge trigger
[10]	w1c	1'b0	PIN2	Write 1 to clear PB34 wakeup source. Only valid if PIN wakeup is configured as edge trigger

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表 4-5: LPSYS_AON 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[9]	w1c	1'b0	PIN1	Write 1 to clear PB33 wakeup source. Only valid if PIN wakeup is configured as edge trigger
[8]	w1c	1'b0	PIN0	Write 1 to clear PB32 wakeup source. Only valid if PIN wakeup is configured as edge trigger
[7:0]			RSVD	
0x28			**ISSR**	Inter System Status Register
[31:6]			RSVD	
[5]	r	1'h1	HP_ACTIVE	read 1 indicates HPSYS is active
[4]	rw	1'h1	LP_ACTIVE	write 1 to indicates LPSYS is active
[3:2]			RSVD	
[1]	r	1'b0	HP2LP_REQ	indicate HPSYS request exists
[0]	rw	1'b0	LP2HP_REQ	write 1 to request HPSYS to stay in active mode
0x2C			**TARGET**	BT sleep time target
[31:28]			RSVD	
[27:0]	rw	28'h0	SLEEP_TARGET	bt sleep time target in cycles of clk_lp
0x30			**ACTUAL**	BT actual sleep time
[31:28]			RSVD	
[27:0]	r	28'h0	SLEEP_CNT	bt actual sleep time in cycles of clk_lp. If not woken up by software or external interrupt, sleep_cnt counts up every clk_lp cycle, until reaches sleep_target
0x34			**PRE_WKUP**	time before bt awake
[31:26]			RSVD	
[25:16]	rw	10'h18	WKUP_TIME	cycles of clk_lp for LPSYS ready before bt awake.
[15:10]			RSVD	
[9:0]	rw	10'h20	XTAL_TIME	cycles of clk_lp for hxt48 ready before bt awake.
0x38			**SLP_CFG**	BT sleep configuration
[31:4]			RSVD	
[3]	rw	1'h0	XTAL_FORCE_OFF	for debug only
[2]	rw	1'h0	XTAL_ALWAYS_ON	for debug only
[1:0]			RSVD	
0x3C			**SLP_CTRL**	BT sleep control
[31:7]			RSVD	
[6]	r	1'h1	BT_WKUP	bt wakeup source. 1 means bt has not enter sleep or has enter wakeup procedure
[5]	r	1'h1	XTAL_REQ	xtal request status. 1 means bt is requiring xtal.
[4]	r	1'h0	SLEEP_STATUS	bt sleep status. 1 means bt is sleeping and sleep_cnt is counting up
[3:2]			RSVD	
[1]	w1s	1'h0	WKUP_REQ	software request to wakeup bt. Will be cleared automatically
[0]	w1s	1'h0	SLEEP_REQ	bt sleep request. Will be cleared automatically
0x40			**ANACR**	Analog Control Register
[31:2]			RSVD	
[1]	rw	1'b0	VLP_ISO	Set 1 to force off all LPSYS related analog modules
[0]	rw	1'b0	PB_ISO	Set 1 to force IO(PB) into retention mode
0x44			**GTIMR**	Global Timer Register
[31:0]	r	32'h0	CNT	Global timer value
0x48			**RESERVE0**	Reserved Register 0
[31:0]	rw	32'b0	DATA	for debug only
0x4C			**RESERVE1**	Reserved Register 1
[31:0]	rw	32'b0	DATA	for debug only
0x100			**SPR**	Stack Pointer Register

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表 4-5: LPSYS_AON 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:0]	rw	32'h20120000	SP	LCPU stack pointer address
0x104			**PCR**	Pointer Counter Register
[31:0]	rw	32'h00100875	PC	LCPU PC pointer address

5 输入输出

5.1 简介

芯片最多支持 120 个可配置 IO 管脚，包括 79 个位于 HPSYS 的通用 IO(PA00~PA78)，37 个位于 LPSYS 的通用 IO(PB00~PB36)，以及 6 个低功耗 IO(PBR00~PBR03)。不同封装的芯片能够使用的 IO 管脚数量不同。每个通用 IO 可独立选择输入输出功能，并独立配置驱动强度和上下拉电阻。当配置为 GPIO 功能时，每个通用 IO 均可根据电平的高低或翻转触发中断，并可将系统从某些低功耗模式中唤醒。

5.2 IO 结构

单个通用 IO 的结构如下图。

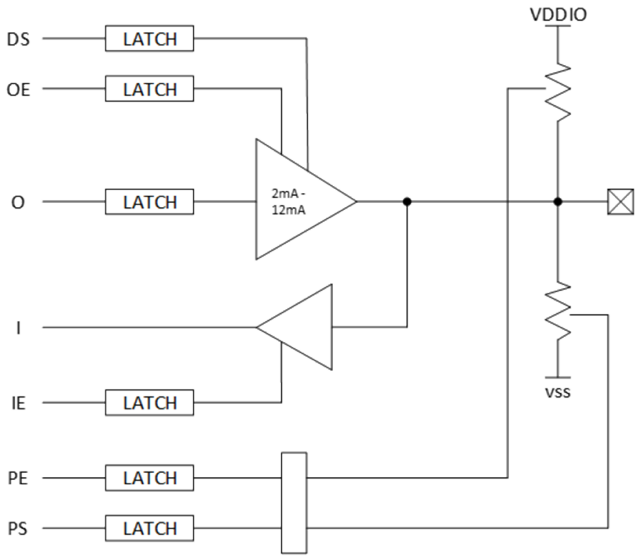

图 5-1: IO 结构

DS 用于配置驱动强度，由 PINMUX 对应 IO 的 DS0 和 DS1 寄存器指定。{DS1,DS0} 的值由 0 到 3，驱动强度逐渐增大。

IO 输出由 O 和 OE 确定，根据 PINMUX 对应 IO 的 FSEL 寄存器选择不同功能，自动映射到相应功能的输出。

IO 输入使能由 PINMUX 对应 IO 的 IE 寄存器控制。当 IE 为高时，输入电平 I 根据 PINMUX 对应 IO 的 FSEL 寄存器自动映射到相应功能的输入；当 IE 为低时，相应功能无法获取到 IO 的输入电平。

PE 和 PS 用于控制 IO 的上下拉电阻，由 PINMUX 对应 IO 的 PE 和 PS 寄存器指定。PE 为 0 时上下拉电阻均不生效。PE 为 1，PS 为 0 时，下拉电阻有效。PE 为 1，PS 为 1 时，上拉电阻有效。上下拉电阻的阻值约为 10k~40k 欧姆，与 IO 外部电路以及接口电平相关。

5.3 输入输出选择

通过配置 PINMUX 对应 IO 的 FSEL 寄存器，可以将可配置 IO 的输入输出映射为若干功能中的一种。每个 IO 能够映射的功能可以在 GPIO 管脚列表中查询。如果该功能为输入，或输入输出双向，还需要将对应 IO 的 IE 寄存器置 1。

每个通用 IO 均可映射为 GPIO 功能，此时 IO 的输出由 GPIO 模块控制。无论 IO 映射为哪种功能，IO 输入均能够从 GPIO 模块中读取，并可产生 GPIO 中断。

当某个 PA 映射为 PA_I2C_UART 功能时，该 IO 可以作为 HPSYS 中任意一个 I2C 或 USART 的接口信号使用。具体作为哪个接口信号还需要在 HPSYS_CFG 寄存器中指定。例如若要让 PA07 作为 USART2 的 TXD 使用，需设置 PINMUX 寄存器的 PAD_PA07_FSEL 为 4(对应 PA_I2C_UART)，并设置 HPSYS_CFG 寄存器的 USART2_PINR_TXD_PIN 为 7(对应 PA07)。应注意若将多个接口信号指定到同一个 IO 会引起功能错误。

当某个 PA 映射为 PA_TIM 功能时，该 IO 可以作为 HPSYS 中任意一个 GPTIM 的接口信号使用。具体作为哪个接口信号还需要在 HPSYS_CFG 寄存器中指定。例如若要让 PA60 作为 GPTIM2 的 CH3 使用，需设置 PINMUX 寄存器的 PAD_PA60_FSEL 为 5(对应 PA_TIM)，并设置 HPSYS_CFG 寄存器的 GPTIM2_PINR_CH3_PIN 为 60(对应 PA60)。应注意若将多个接口信号指定到同一个 IO 会引起功能错误。

当某个 PB 映射为 PB_I2C_UART 功能时，该 IO 可以作为 LPSYS 中任意一个 I2C 或 USART 的接口信号使用。具体作为哪个接口信号还需要在 LPSYS_CFG 寄存器中指定。例如若要让 PB28 作为 I2C5 的 SDA 使用，需设置 PINMUX 寄存器的 PAD_PB28_FSEL 为 2(对应 PB_I2C_UART)，并设置 LPSYS_CFG 寄存器的 I2C5_PINR_SDA_PIN 为 28(对应 PB28)。应注意若将多个接口信号指定到同一个 IO 会引起功能错误。

当某个 PB 映射为 PB_TIM 功能时，该 IO 可以作为 LPSYS 中任意一个 GPTIM 的接口信号使用。具体作为哪个接口信号还需要在 LPSYS_CFG 寄存器中指定。例如若要让 PB12 作为 GPTIM5 的 ETR 使用，需设置 PINMUX 寄存器的 PAD_PB12_FSEL 为 3(对应 PB_TIM)，并设置 LPSYS_CFG 寄存器的 ETR_PINR_ETR5_PIN 为 12(对应 PB12)。应注意若将多个接口信号指定到同一个 IO 会引起功能错误。

5.4 IO 高阻

芯片上电以后，IO 默认存在上拉或下拉电阻 (PE 默认值为 1)，需由软件将 IO 配置为所需状态。如果要让 IO 配置为高阻，需将 PE 设置为 0，IO 设置为 GPIO 功能，并且 GPIO 输出使能关闭。

5.5 I2C 模式

部分 IO 可配置为 I2C 模式。该模式针对 I2C 功能进行了优化，支持更大的负载电流 (20mA)，并内置模拟滤波器用于滤除毛刺。将 PINMUX 对应 IO 的 MODE 寄存器置 1 可使能 I2C 模式。I2C 模式应仅在 IO 映射为 I2C 功能时开启。

可配置为 I2C 模式的 IO 包括：

PA17，PA18，PA48，PA49，PB00，PB01，PB23，PB24。

5.6 GPIO 输出

当 IO 配置为 GPIO 功能时，IO 的 O 和 OE 控制信号由 GPIO 寄存器控制，从而产生 IO 的输出。HPSYS 的通用 IO(PA00~PA78) 由 HPSYS_GPIO 控制，LPSYS 的通用 IO(PB00~PB36) 由 LPSYS_GPIO 控制。GPIO 寄存器的每个比特对应一个通用 IO，例如 HPSYS_GPIO 中 DOER0 的比特 0 对应 PA00，比特 31 对应 PA31；DOER1 的比特 0 对应 PA32，比特 31 对应 PA63；DOER2 的比特 0 对应 PA64，比特 14 对应 PA78。

DOERx 寄存器直接控制 IO 的 OE 信号，为 1 时 IO 的输出导通，为 0 时 IO 的输出关断。软件可以直接配置 DOERx 寄存器，也可以配置 DOESRx 或 DOECRx 进行位操作以免影响其它 IO。

DORx 寄存器直接控制 IO 的 O 信号，为 1 时 IO 的输出为高电平，为 0 时 IO 的输出为低电平。软件可以直接配置 DORx 寄存器，也可以配置 DOSRx 或 DOCRx 进行位操作以免影响其它 IO。

GPIO 推挽输出的配置方法为：

推挽输出 0，需使 IO 的 OE 为 1 ，O 为 0，即 DOERx 对应比特配置为 1，DORx 对应比特配置为 0。

推挽输出 1，需使 IO 的 OE 为 1 ，O 为 1，即 DOERx 对应比特配置为 1，DORx 对应比特配置为 1。

当需要产生开漏输出时，应当首先根据翻转速率需求，使能 IO 内部上拉电阻 (PE=1,PS=1)，或在芯片外部连接上拉电阻。

GPIO 开漏输出的配置方法为：

开漏输出 0，需使 IO 的 OE 为 1 ，O 为 0，即 DOERx 对应比特配置为 1，DORx 对应比特配置为 0。

开漏输出 1，需使 IO 的 OE 为 0，即 DOERx 的对应比特配置为 0。

5.7 GPIO 输入

无论 IO 映射为哪种功能，IO 输入均能够从 GPIO 寄存器 DIRx 中读取，并可根据配置产生 GPIO 中断。

IO 中断使能应仅在需要时打开。软件可以直接配置 IERx 寄存器，也可以配置 IESRx 或 IECRx 进行位操作以免影响其它 IO。

即使 IO 未配置为 GPIO 功能，IO 中断仍可产生，因此当不需要 IO 产生中断时，应当确保其中断使能关闭。

GPIO 中断产生的条件包括 IO 输入信号为高电平/低电平/上升沿/下降沿/双边沿等，如下表所示。

IPH	IPL	ITR=0	ITR=1
0	0	不触发	不触发
0	1	低电平	下降沿
1	0	高电平	上升沿
1	1	无效配置	双边沿

ITR 用于选择中断条件类型。软件可以直接配置 ITRx 寄存器，也可以配置 ITSRx 或 ITCRx 进行位操作以免影响其它 IO。

IPH 用于使能高电平或上升沿中断条件。软件可以直接配置 IPHRx 寄存器，也可以配置 IPHSRx 或 IPHCRx 进行

位操作以免影响其它 IO。

IPL 用于使能低电平或下降沿中断条件。软件可以直接配置 IPLRx 寄存器，也可以配置 IPLSRx 或 IPLCRx 进行位操作以免影响其它 IO。

产生中断的 IO 可通过 ISRx 查询。向 ISRx 的相应比特写 1 可以清除中断状态。

5.8 大核域 GPIO（PA）列表

表 5-1: 大核域 GPIO（PA）管脚列表

Pin Number			Pin Name	Type	Sel #	Function
SF32LB560	SF32LB561 SF32LB563	SF32LB565 SF32LB566 SF32LB567				
QFN68L	QFN68L	BGA175				
-	-	R9	PA00	I/O	0	GPIO_A0
					2	WLAN_ACTIVE
					3	ATIM1_CH1
					4	PA_I2C_UART
					5	PA_TIM
					6	SCI_CLK
					Others	Reserved
-	-	P9	PA01	I/O	0	GPIO_A1
					2	BT_ACTIVE
					3	ATIM1_CH1N
					4	PA_I2C_UART
					5	PA_TIM
					6	SCI_DIO
					7	SPI1_DI
					Others	Reserved
-	-	M9	PA02	I/O	0	GPIO_A2
					2	BT_COLLISION
					4	PA_I2C_UART
					5	PA_TIM
					6	SCI_RST
					7	SPI1_CS
					Others	Reserved
-	-	L9	PA03	I/O	0	GPIO_A3
					3	ATIM1_CH2
					4	PA_I2C_UART
					5	PA_TIM
					6	CAN1_TXD
					7	SPI1_DO
					8	SPI1_DIO
					Others	Reserved
-	-	N8	PA04	I/O	0	GPIO_A4
					2	BT_PRIORITY
					3	ATIM1_CH2N
					4	PA_I2C_UART
					5	PA_TIM

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表 5-1: 大核域 GPIO（PA）管脚列表（续）

Pin Number			Pin Name	Type	Sel #	Function
SF32LB560	SF32LB561 SF32LB563	SF32LB565 SF32LB566 SF32LB567				
QFN68L	QFN68L	BGA175				
					6	CAN1_RXD
					7	SPI1_CLK
					Others	Reserved
-	26	P8	PA05	I/O	0	GPIO_A5
					4	PA_I2C_UART
					5	PA_TIM
					Others	Reserved

续表下页...

表 5-1: 大核域 GPIO（PA）管脚列表（续）

Pin Number			Pin Name	Type	Sel #	Function
SF32LB560	SF32LB561 SF32LB563	SF32LB565 SF32LB566 SF32LB567				
QFN68L	QFN68L	BGA175				
24	24	M8	PA06	I/O	0	GPIO_A6
					1	SD2_DIO2
					2	MPI3_CS
					3	I2S1_MCLK
					4	PA_I2C_UART
					5	PA_TIM
					Others	Reserved
23	23	L7	PA07	I/O	0	GPIO_A7
					1	SD2_DIO3
					2	MPI3_DIO1
					3	I2S1_SDI
					4	PA_I2C_UART
					5	PA_TIM
					Others	Reserved
22	22	R7	PA08	I/O	0	GPIO_A8
					1	SD2_CLK
					2	MPI3_DIO2
					3	I2S1_SDO
					4	PA_I2C_UART
					5	PA_TIM
					Others	Reserved
21	21	P7	PA09	I/O	0	GPIO_A9
					1	SD2_CMD
					2	MPI3_DIO0
					3	I2S1_BCK
					4	PA_I2C_UART
					5	PA_TIM
					Others	Reserved
20	20	J7	PA10	I/O	0	GPIO_A10
					1	SD2_DIO0
					2	MPI3_CLK
					3	I2S1_LRCK
					4	PA_I2C_UART
					5	PA_TIM
					Others	Reserved
19	19	M6	PA11	I/O	0	GPIO_A11
					1	SD2_DIO1
					2	MPI3_DIO3
					4	PA_I2C_UART
					5	PA_TIM
					Others	Reserved

续表下页...

表 5-1: 大核域 GPIO（PA）管脚列表（续）

Pin Number			Pin Name	Type	Sel #	Function
SF32LB560	SF32LB561 SF32LB563	SF32LB565 SF32LB566 SF32LB567				
QFN68L	QFN68L	BGA175				
-	-	R6	PA12	I/O	0	GPIO_A12
					1	SD1_DIO2
					2	MPI3_CS
					4	PA_I2C_UART
					5	PA_TIM
					Others	Reserved
-	-	N5	PA13	I/O	0	GPIO_A13
					1	SD1_DIO6
					2	BT_ACTIVE
					3	ATIM1_CH3
					4	PA_I2C_UART
					5	PA_TIM
					6	LCDC1_DPI_R1
					Others	Reserved
-	-	M5	PA14	I/O	0	GPIO_A14
					1	SD1_DIO7
					2	WLAN_ACTIVE
					3	ATIM1_CH3N
					4	PA_I2C_UART
					5	PA_TIM
					6	LCDC1_DPI_R0
					Others	Reserved
-	-	R5	PA15	I/O	0	GPIO_A15
					1	SD1_DIO1
					2	MPI3_DIO3
					4	PA_I2C_UART
					5	PA_TIM
					Others	Reserved
-	-	L5	PA16	I/O	0	GPIO_A16
					3	ATIM1_CH4
					4	PA_I2C_UART
					5	PA_TIM
					6	LCDC1_DPI_R2
					Others	Reserved
17	17	P5	PA17	I/O	0	GPIO_A17
					2	#USB11_DP
					3	ATIM1_BKIN
					4	PA_I2C_UART
					5	PA_TIM
					Others	Reserved

续表下页...

表 5-1: 大核域 GPIO（PA）管脚列表（续）

Pin Number			Pin Name	Type	Sel #	Function
SF32LB560	SF32LB561 SF32LB563	SF32LB565 SF32LB566 SF32LB567				
QFN68L	QFN68L	BGA175				
16	16	P4	PA18	I/O	0	GPIO_A18
					2	#USB11_DM
					3	ATIM1_BKIN2
					4	PA_I2C_UART
					5	PA_TIM
					Others	Reserved
-	-	P3	PA19	I/O	0	GPIO_A19
					1	SD1_DIO5
					2	BT_PRIORITY
					3	ATIM1_ETR
					4	PA_I2C_UART
					5	PA_TIM
					6	LCDC1_DPI_R4
					Others	Reserved
-	-	P1	PA20	I/O	0	GPIO_A20
					1	SD1_DIO3
					2	MPI3_DIO1
					3	SPI1_CLK
					4	PA_I2C_UART
					5	PA_TIM
					7	I2S1_LRCK
					8	PDM1_DATA
					Others	Reserved
-	-	R2	PA21	I/O	0	GPIO_A21
					1	SD1_DIO4
					2	BT_COLLISION
					4	PA_I2C_UART
					5	PA_TIM
					6	LCDC1_DPI_R5
					Others	Reserved
-	-	R3	PA22	I/O	0	GPIO_A22
					1	SD1_DIO0
					2	MPI3_CLK
					4	PA_I2C_UART
					5	PA_TIM
					Others	Reserved
-	-	P2	PA23	I/O	0	GPIO_A23
					4	PA_I2C_UART
					5	PA_TIM
					6	LCDC1_DPI_R6
					Others	Reserved

续表下页...

表 5-1: 大核域 GPIO（PA）管脚列表（续）

Pin Number			Pin Name	Type	Sel #	Function
SF32LB560	SF32LB561 SF32LB563	SF32LB565 SF32LB566 SF32LB567				
QFN68L	QFN68L	BGA175				
-	-	N4	PA24	I/O	0	GPIO_A24
					2	ATIM1_CH1
					3	SPI1_CS
					4	PA_I2C_UART
					5	PA_TIM
					6	LCDC1_DPI_R3
					7	I2S1_SDI
					8	PDM1_CLK
					Others	Reserved
-	-	N3	PA25	I/O	0	GPIO_A25
					1	SD1_CLKIN
					2	ATIM1_CH1N
					3	SPI1_DI
					4	PA_I2C_UART
					5	PA_TIM
					6	LCDC1_DPI_R7
					7	I2S1_BCK
					8	PDM2_DATA
					Others	Reserved
-	-	N1	PA26	I/O	0	GPIO_A26
					1	SD1_CLK
					2	MPI3_DIO2
					3	SPI1_DO
					4	PA_I2C_UART
					5	PA_TIM
					7	I2S1_SDO
					8	PDM2_CLK
					Others	Reserved
-	-	N2	PA27	I/O	0	GPIO_A27
					1	SD1_CMD
					2	MPI3_DIO0
					4	PA_I2C_UART
					5	PA_TIM
					Others	Reserved
15	15	M3	PA28	I/O	0	GPIO_A28
					2	SPI2_CS
					3	SWDIO
					4	PA_I2C_UART
					5	PA_TIM
					6	LCDC1_DPI_G0
					7	LCDC1_JDI_B2
					8	LCDC1_8080_DIO2
					Others	Reserved

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表 5-1: 大核域 GPIO（PA）管脚列表（续）

Pin Number			Pin Name	Type	Sel #	Function
SF32LB560	SF32LB561 SF32LB563	SF32LB565 SF32LB566 SF32LB567				
QFN68L	QFN68L	BGA175				
-	-	L4	PA29	I/O	0	GPIO_A29
					2	SPI2_DI
					3	ATIM1_CH2
					4	PA_I2C_UART
					5	PA_TIM
					6	LCDC1_DPI_G5
					7	LCDC1_JDI_R1
					8	LCDC1_8080_DIO3
					Others	Reserved
-	-	M2	PA30	I/O	0	GPIO_A30
					2	SPI2_CLK
					3	ATIM1_CH2N
					4	PA_I2C_UART
					5	PA_TIM
					6	LCDC1_DPI_G1
					7	LCDC1_JDI_B1
					8	LCDC1_8080_DIO4
					Others	Reserved
14	14	K5	PA31	I/O	0	GPIO_A31
					3	SWCLK
					4	PA_I2C_UART
					5	PA_TIM
					6	LCDC1_DPI_G6
					7	LCDC1_JDI_R2
					8	LCDC1_8080_DIO5
					Others	Reserved
-	-	L3	PA32	I/O	0	GPIO_A32
					4	PA_I2C_UART
					5	PA_TIM
					6	LCDC1_DPI_G2
					7	LCDC1_JDI_G2
					8	LCDC1_8080_DIO6
					Others	Reserved
13	13	L1	PA33	I/O	0	GPIO_A33
					1	LCDC1_SPI_TE
					4	PA_I2C_UART
					5	PA_TIM
					6	LCDC1_DPI_G3
					8	LCDC1_8080_TE
					Others	Reserved

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表 5-1: 大核域 GPIO（PA）管脚列表（续）

Pin Number			Pin Name	Type	Sel #	Function
SF32LB560	SF32LB561 SF32LB563	SF32LB565 SF32LB566 SF32LB567				
QFN68L	QFN68L	BGA175				
-	-	L2	PA34	I/O	0	GPIO_A34
					2	SPI2_DO
					3	SPI2_DIO
					4	PA_I2C_UART
					5	PA_TIM
					6	LCDC1_DPI_G4
					7	LCDC1_JDI_G1
					8	LCDC1_8080_DIO7
					Others	Reserved
-	-	K1	PA35	I/O	0	GPIO_A35
					4	PA_I2C_UART
					5	PA_TIM
					6	LCDC1_DPI_G7
					Others	Reserved
12	12	K4	PA36	I/O	0	GPIO_A36
					1	LCDC1_SPI_CS
					4	PA_I2C_UART
					5	PA_TIM
					6	LCDC1_DPI_B0
					7	LCDC1_JDI_HCK
					8	LCDC1_8080_CS
					Others	Reserved
11	11	J5	PA37	I/O	0	GPIO_A37
					1	LCDC1_SPI_CLK
					2	I2S1_MCLK
					4	PA_I2C_UART
					5	PA_TIM
					6	LCDC1_DPI_B1
					8	LCDC1_8080_WR
					Others	Reserved
10	10	K2	PA38	I/O	0	GPIO_A38
					1	LCDC1_SPI_DIO0
					2	I2S1_SDI
					4	PA_I2C_UART
					5	PA_TIM
					6	LCDC1_DPI_B2
					7	LCDC1_JDI_HST
					8	LCDC1_8080_RD
					Others	Reserved

续表下页...

表 5-1: 大核域 GPIO（PA）管脚列表（续）

Pin Number			Pin Name	Type	Sel #	Function
SF32LB560	SF32LB561 SF32LB563	SF32LB565 SF32LB566 SF32LB567				
QFN68L	QFN68L	BGA175				
9	9	H5	PA39	I/O	0	GPIO_A39
					1	LCDC1_SPI_DIO1
					2	I2S1_SDO
					4	PA_I2C_UART
					5	PA_TIM
					6	LCDC1_DPI_B5
					7	LCDC1_JDI_XRST
					8	LCDC1_8080_DC
					Others	Reserved
8	8	H4	PA40	I/O	0	GPIO_A40
					1	LCDC1_SPI_DIO2
					2	I2S1_BCK
					4	PA_I2C_UART
					5	PA_TIM
					6	LCDC1_DPI_B6
					7	LCDC1_JDI_VST
					8	LCDC1_8080_DIO0
					Others	Reserved
7	7	J2	PA41	I/O	0	GPIO_A41
					1	LCDC1_SPI_DIO3
					2	I2S1_LRCK
					4	PA_I2C_UART
					5	PA_TIM
					6	LCDC1_DPI_B4
					7	LCDC1_JDI_VCK
					8	LCDC1_8080_DIO1
					Others	Reserved
-	-	G5	PA42	I/O	0	GPIO_A42
					4	PA_I2C_UART
					5	PA_TIM
					6	LCDC1_DPI_VSYNC
					Others	Reserved
-	-	H3	PA43	I/O	0	GPIO_A43
					1	LCDC1_SPI_RSTB
					4	PA_I2C_UART
					5	PA_TIM
					6	LCDC1_DPI_B3
					7	LCDC1_JDI_ENB
					8	LCDC1_8080_RSTB
					Others	Reserved

续表下页...

表 5-1: 大核域 GPIO（PA）管脚列表（续）

Pin Number			Pin Name	Type	Sel #	Function
SF32LB560	SF32LB561 SF32LB563	SF32LB565 SF32LB566 SF32LB567				
QFN68L	QFN68L	BGA175				
-	-	G3	PA44	I/O	0	GPIO_A44
					3	ATIM1_CH3
					4	PA_I2C_UART
					5	PA_TIM
					6	LCDC1_DPI_HSYNC
					Others	Reserved
-	-	G2	PA45	I/O	0	GPIO_A45
					3	ATIM1_CH3N
					4	PA_I2C_UART
					5	PA_TIM
					6	LCDC1_DPI_CLK
					Others	Reserved
-	-	G1	PA46	I/O	0	GPIO_A46
					4	PA_I2C_UART
					5	PA_TIM
					6	LCDC1_DPI_B7
					Others	Reserved
-	-	G4	PA47	I/O	0	GPIO_A47
					3	ATIM1_CH4
					4	PA_I2C_UART
					5	PA_TIM
					6	LCDC1_DPI_DE
					Others	Reserved
5	5	F3	PA48	I/O	0	GPIO_A48
					4	PA_I2C_UART
					5	PA_TIM
					Others	Reserved
4	4	F2	PA49	I/O	0	GPIO_A49
					4	PA_I2C_UART
					5	PA_TIM
					Others	Reserved
3	3	E2	PA50	I/O	0	GPIO_A50
					2	#WKUP_PIN5
					4	PA_I2C_UART
					5	PA_TIM
					6	LCDC1_DPI_SD
					Others	Reserved
2	2	E1	PA51	I/O	0	GPIO_A51
					2	#WKUP_PIN6
					4	PA_I2C_UART
					5	PA_TIM
					6	LCDC1_DPI_CM
					Others	Reserved

续表下页...

表 5-1: 大核域 GPIO（PA）管脚列表（续）

Pin Number			Pin Name	Type	Sel #	Function
SF32LB560	SF32LB561 SF32LB563	SF32LB565 SF32LB566 SF32LB567				
QFN68L	QFN68L	BGA175				
-	-	C3	PA52	I/O	0	GPIO_A52
					2	#WKUP_PIN7
					3	ATIM1_BKIN
					4	PA_I2C_UART
					5	PA_TIM
					Others	Reserved
-	-	D2	PA53	I/O	0	GPIO_A53
					2	#WKUP_PIN8
					3	ATIM1_BKIN2
					4	PA_I2C_UART
					5	PA_TIM
					Others	Reserved
-	-	D3	PA54	I/O	0	GPIO_A54
					2	#WKUP_PIN9
					3	ATIM1_ETR
					4	PA_I2C_UART
					5	PA_TIM
					Others	Reserved
61	61	A5	PA55	I/O	0	GPIO_A55
					1	#XTAL32K_XI
					4	PA_I2C_UART
					5	PA_TIM
					Others	Reserved
60	60	A6	PA56	I/O	0	GPIO_A56
					1	#XTAL32K_XO
					4	PA_I2C_UART
					5	PA_TIM
					Others	Reserved
-	-	D6	PA57	I/O	0	GPIO_A57
					1	SPI1_CLK
					4	PA_I2C_UART
					5	PA_TIM
					Others	Reserved
-	-	D4	PA58	I/O	0	GPIO_A58
					1	SPI1_CS
					4	PA_I2C_UART
					5	PA_TIM
					Others	Reserved
-	-	F4	PA59	I/O	0	GPIO_A59
					1	SPI1_DI
					4	PA_I2C_UART
					5	PA_TIM
					Others	Reserved

续表下页...

表 5-1: 大核域 GPIO（PA）管脚列表（续）

Pin Number			Pin Name	Type	Sel #	Function
SF32LB560	SF32LB561 SF32LB563	SF32LB565 SF32LB566 SF32LB567				
QFN68L	QFN68L	BGA175				
-	-	C6	PA60	I/O	0	GPIO_A60
					3	ATIM1_CH1
					4	PA_I2C_UART
					5	PA_TIM
					Others	Reserved
-	-	E6	PA61	I/O	0	GPIO_A61
					1	SPI1_DO
					2	SPI1_DIO
					4	PA_I2C_UART
					5	PA_TIM
					Others	Reserved
-	-	C7	PA62	I/O	0	GPIO_A62
					3	ATIM1_CH1N
					4	PA_I2C_UART
					5	PA_TIM
					Others	Reserved
-	-	D7	PA63	I/O	0	GPIO_A63
					4	PA_I2C_UART
					5	PA_TIM
					Others	Reserved
-	-	B7	PA64	I/O	0	GPIO_A64
					1	I2S1_SDO
					2	PDM1_DATA
					4	PA_I2C_UART
					5	PA_TIM
					6	SPI2_DO
					7	SPI2_DIO
					Others	Reserved
-	-	A7	PA65	I/O	0	GPIO_A65
					1	I2S1_MCLK
					4	PA_I2C_UART
					5	PA_TIM
					Others	Reserved
-	-	E7	PA66	I/O	0	GPIO_A66
					3	ATIM1_CH2
					4	PA_I2C_UART
					5	PA_TIM
					Others	Reserved
-	-	D8	PA67	I/O	0	GPIO_A67
					4	PA_I2C_UART
					5	PA_TIM
					Others	Reserved

续表下页...

表 5-1: 大核域 GPIO（PA）管脚列表（续）

Pin Number			Pin Name	Type	Sel #	Function
SF32LB560	SF32LB561 SF32LB563	SF32LB565 SF32LB566 SF32LB567				
QFN68L	QFN68L	BGA175				
-	-	E8	PA68	I/O	0	GPIO_A68
					3	ATIM1_CH2N
					4	PA_I2C_UART
					5	PA_TIM
					Others	Reserved
-	-	B8	PA69	I/O	0	GPIO_A69
					1	I2S1_SDI
					2	PDM1_CLK
					4	PA_I2C_UART
					5	PA_TIM
					6	SPI2_DI
					Others	Reserved
-	-	E9	PA70	I/O	0	GPIO_A70
					3	ATIM1_CH3
					4	PA_I2C_UART
					5	PA_TIM
					Others	Reserved
-	-	B9	PA71	I/O	0	GPIO_A71
					1	I2S1_LRCK
					2	PDM2_DATA
					3	ATIM1_CH3N
					4	PA_I2C_UART
					5	PA_TIM
					6	SPI2_CS
					Others	Reserved
-	-	E10	PA72	I/O	0	GPIO_A72
					4	PA_I2C_UART
					5	PA_TIM
					Others	Reserved
-	-	A9	PA73	I/O	0	GPIO_A73
					1	I2S1_BCK
					2	PDM2_CLK
					3	ATIM1_CH4
					4	PA_I2C_UART
					5	PA_TIM
					6	SPI2_CLK
					Others	Reserved
-	-	E11	PA74	I/O	0	GPIO_A74
					4	PA_I2C_UART
					5	PA_TIM
					Others	Reserved

续表下页...

表 5-1: 大核域 GPIO（PA）管脚列表（续）

Pin Number			Pin Name	Type	Sel #	Function
SF32LB560	SF32LB561 SF32LB563	SF32LB565 SF32LB566 SF32LB567				
QFN68L	QFN68L	BGA175				
-	-	C11	PA75	I/O	0	GPIO_A75
					3	ATIM1_BKIN
					4	PA_I2C_UART
					5	PA_TIM
					Others	Reserved
-	-	D10	PA76	I/O	0	GPIO_A76
					3	ATIM1_BKIN2
					4	PA_I2C_UART
					5	PA_TIM
					Others	Reserved
-	-	E12	PA77	I/O	0	GPIO_A77
					3	ATIM1_ETR
					4	PA_I2C_UART
					5	PA_TIM
					Others	Reserved
-	-	C10	PA78	I/O	0	GPIO_A78
					4	PA_I2C_UART
					5	PA_TIM
					Others	Reserved

5.9 小核域 GPIO（PB）列表

表 5-2: 小核域 GPIO（PB）管脚列表

Pin Number			Pin Name	Type	Sel #	Function
SF32LB560	SF32LB561 SF32LB563	SF32LB565 SF32LB566 SF32LB567				
QFN68L	QFN68L	BGA175				
-	-	L10	PB00	I/O	0	GPIO_B0
					2	PB_I2C_UART
					3	PB_TIM
					Others	Reserved
-	-	L11	PB01	I/O	0	GPIO_B1
					2	PB_I2C_UART
					3	PB_TIM
					Others	Reserved
-	-	P10	PB02	I/O	0	GPIO_B2
					2	PB_I2C_UART
					3	PB_TIM
					Others	Reserved
-	-	M11	PB03	I/O	0	GPIO_B3
					2	PB_I2C_UART
					3	PB_TIM
					4	BT_COLLISION
					Others	Reserved
26	-	H10	PB04	I/O	0	GPIO_B4
					1	TWI_CLK
					2	PB_I2C_UART
					3	PB_TIM
					Others	Reserved
27	-	G10	PB05	I/O	0	GPIO_B5
					1	TWI_DIO
					2	PB_I2C_UART
					3	PB_TIM
					Others	Reserved
-	-	P11	PB06	I/O	0	GPIO_B6
					2	PB_I2C_UART
					3	PB_TIM
					4	BT_ACTIVE
					7	LPCOMP1_OUT
					Others	Reserved
-	-	N11	PB07	I/O	0	GPIO_B7
					2	PB_I2C_UART
					3	PB_TIM
					4	WLAN_ACTIVE
					Others	Reserved

续表下页...

表 5-2: 小核域 GPIO（PB）管脚列表（续）

Pin Number			Pin Name	Type	Sel #	Function
SF32LB560	SF32LB561 SF32LB563	SF32LB565 SF32LB566 SF32LB567				
QFN68L	QFN68L	BGA175				
-	-	P13	PB08	I/O	0	GPIO_B8
					1	SPI4_CS
					2	PB_I2C_UART
					3	PB_TIM
					4	BT_PRIORITY
					Others	Reserved
-	-	J12	PB09	I/O	0	GPIO_B9
					1	SPI4_CLK
					2	PB_I2C_UART
					3	PB_TIM
					Others	Reserved
-	-	N13	PB10	I/O	0	GPIO_B10
					2	PB_I2C_UART
					3	PB_TIM
					Others	Reserved
-	-	K12	PB11	I/O	0	GPIO_B11
					1	SPI4_DI
					2	PB_I2C_UART
					3	PB_TIM
					Others	Reserved
-	-	R13	PB12	I/O	0	GPIO_B12
					1	SPI4_DO
					2	PB_I2C_UART
					3	PB_TIM
					4	SPI4_DIO
					Others	Reserved
28	28	R12	PB13	I/O	0	SWDIO
					1	GPIO_B13
					2	PB_I2C_UART
					3	PB_TIM
					Others	Reserved
-	-	N14	PB14	I/O	0	GPIO_B14
					2	PB_I2C_UART
					3	PB_TIM
					Others	Reserved
29	29	P12	PB15	I/O	0	SWCLK
					1	GPIO_B15
					2	PB_I2C_UART
					3	PB_TIM
					Others	Reserved

续表下页...

表 5-2: 小核域 GPIO（PB）管脚列表（续）

Pin Number			Pin Name	Type	Sel #	Function
SF32LB560	SF32LB561 SF32LB563	SF32LB565 SF32LB566 SF32LB567				
QFN68L	QFN68L	BGA175				
30	30	N12	PB16	I/O	0	GPIO_B16
					2	PB_I2C_UART
					3	PB_TIM
					7	#DCTEST0
					Others	Reserved
31	31	M12	PB17	I/O	0	GPIO_B17
					2	PB_I2C_UART
					3	PB_TIM
					7	#DCTEST1
					Others	Reserved
32	32	P14	PB18	I/O	0	GPIO_B18
					1	SPI3_CS
					2	PB_I2C_UART
					3	PB_TIM
					7	#LPCOMP1_P
					Others	Reserved
33	33	P15	PB19	I/O	0	GPIO_B19
					1	SPI3_CLK
					2	PB_I2C_UART
					3	PB_TIM
					7	#LPCOMP1_N
					Others	Reserved
34	34	P16	PB20	I/O	0	GPIO_B20
					1	SPI3_DI
					2	PB_I2C_UART
					3	PB_TIM
					7	#LPCOMP2_P
					Others	Reserved
35	35	R15	PB21	I/O	0	GPIO_B21
					1	SPI3_DO
					2	PB_I2C_UART
					3	PB_TIM
					4	SPI3_DIO
					7	#LPCOMP2_N
					Others	Reserved
36	36	K13	PB22	I/O	0	GPIO_B22
					2	PB_I2C_UART
					3	PB_TIM
					4	TWI_CLK
					7	#GPADC_CH0
					Others	Reserved

续表下页...

表 5-2: 小核域 GPIO（PB）管脚列表（续）

Pin Number			Pin Name	Type	Sel #	Function
SF32LB560	SF32LB561 SF32LB563	SF32LB565 SF32LB566 SF32LB567				
QFN68L	QFN68L	BGA175				
37	37	L13	PB23	I/O	0	GPIO_B23
					2	PB_I2C_UART
					3	PB_TIM
					4	TWI_DIO
					7	#GPADC_CH1
					Others	Reserved
38	38	L14	PB24	I/O	0	GPIO_B24
					2	PB_I2C_UART
					3	PB_TIM
					7	#GPADC_CH2
					Others	Reserved
39	39	N15	PB25	I/O	0	GPIO_B25
					2	PB_I2C_UART
					3	PB_TIM
					7	#GPADC_CH3
					Others	Reserved
40	40	M14	PB26	I/O	0	GPIO_B26
					2	PB_I2C_UART
					3	PB_TIM
					7	#GPADC_CH4
					Others	Reserved
41	41	N16	PB27	I/O	0	GPIO_B27
					2	PB_I2C_UART
					3	PB_TIM
					7	#GPADC_CH5
					Others	Reserved
-	-	M15	PB28	I/O	0	GPIO_B28
					2	PB_I2C_UART
					3	PB_TIM
					4	BT_COLLISION
					7	#GPADC_CH6
					Others	Reserved
-	-	C15	PB29	I/O	0	GPIO_B29
					2	PB_I2C_UART
					3	PB_TIM
					4	BT_PRIORITY
					7	LPCOMP2_OUT
					Others	Reserved
-	-	B16	PB30	I/O	0	GPIO_B30
					2	PB_I2C_UART
					3	PB_TIM
					4	BT_ACTIVE
					Others	Reserved

续表下页...

表 5-2: 小核域 GPIO（PB）管脚列表（续）

Pin Number			Pin Name	Type	Sel #	Function
SF32LB560	SF32LB561 SF32LB563	SF32LB565 SF32LB566 SF32LB567				
QFN68L	QFN68L	BGA175				
-	-	B15	PB31	I/O	0	GPIO_B31
					2	PB_I2C_UART
					3	PB_TIM
					4	WLAN_ACTIVE
					Others	Reserved
54	54	D13	PB32	I/O	0	GPIO_B32
					1	#WKUP_PIN0
					7	#GPADC_CH7
					Others	Reserved
55	55	D14	PB33	I/O	0	GPIO_B33
					1	#WKUP_PIN1
					7	#ACTEST0
					Others	Reserved
56	56	C14	PB34	I/O	0	GPIO_B34
					1	#WKUP_PIN2
					7	#ACTEST1
					Others	Reserved
-	-	A15	PB35	I/O	0	GPIO_B35
					1	#WKUP_PIN3
					Others	Reserved
-	-	B14	PB36	I/O	0	GPIO_B36
					1	#WKUP_PIN4
					Others	Reserved
59	59	A10	PBR00	I/O	0	PWR_REQ
					1	GPO
					2	LPTIM3_OUT
					3	LPTIM3_OUT_BAR
					Others	Reserved
58	58	B10	PBR01	I/O	0	GPO
					1	CLK_LP
					2	LPTIM3_OUT
					3	LPTIM3_OUT_BAR
					Others	Reserved
57	57	D12	PBR02	I/O	0	GPO
					1	CLK_LP
					2	LPTIM3_OUT
					3	LPTIM3_OUT_BAR
					Others	Reserved
-	-	B11	PBR03	I/O	0	GPO
					1	CLK_LP
					2	LPTIM3_OUT
					3	LPTIM3_OUT_BAR
					Others	Reserved

5.10 合封 IO

合封 IO 不计入可配置 IO 数目，专用于 MPI 访问合封 (SiP) 的 NOR flash 或 pSRAM。合封 IO 与通用 IO 的结构相同，可以单独配置每个 IO 的功能以及上下拉。合封 IO 包括 IO(SA)，IO(SB) 和 IO(SC)。其中 IO(SA) 与 IO(SB) 在 HPSYS_PINMUX 中配置，IO(SC) 在 LPSYS_PINMUX 中配置。

IO(SA) 包括 SA00~SA12，用于 MPI1 访问合封的 8 线 pSRAM。

IO(SB) 包括 SB00~SB12，用于 MPI2 访问合封的另一片 8 线 pSRAM。

IO(SC) 包括 SC00~SC05，用于 MPI5 访问合封的 4 线 NOR Flash。

5.11 低功耗 IO(PBR)

低功耗 IO(PBR) 是一类特殊的 IO，能够在芯片处于低功耗模式下保持输入与输出能力。IO(PBR) 的输入使能、输出使能、上下拉电阻等功能可以通过 RTC 的 PBRxR 寄存器配置。IO(PBR) 能够持续输出固定电平，低功耗时钟 clk_lp 或 LPTIM3 产生的低功耗 PWM，不受系统进出低功耗模式的影响 (hibernate 模式下 LPTIM3 停止工作，因此无法输出 PWM)。

5.12 IO 供电

IO 的电平标准取决于其供电电压。

合封 IO 的供电电源同时也是对应合封存储器的供电电源。3 组合封 IO 的电源相互独立。

IO(PA) 与 IO(PB) 的供电独立。

IO(PA) 的供电电源分为两组，其中 PA00~PA11 通过 VDDIOA2 单独供电，有利于更灵活的器件选型。

IO 类别	供电电源
SA	VDDIOSA
SB	VDDIOSB
SC	VDDIOSC
PA00~PA11	VDDIOA2
PA12~PA78	VDDIOA
PB	VDDIOB
PBR	VDDIOB

5.13 唤醒 PIN

芯片支持最多 14 个唤醒 PIN，包括通用 IO PB32~PB36，PA50~PA54，以及低功耗 IO PBR00~PBR03。唤醒 PIN 能够将芯片从 hibernate 模式、standby 模式或 deepsleep 模式中唤醒，唤醒触发方式包括高电平唤醒、低电平唤醒、上升沿唤醒、下降沿唤醒以及双边沿唤醒。唤醒 PIN 功能不依赖于 IO 的功能选择，即 FSEL 寄存器不影响唤醒 PIN 功能。

hibernate 模式支持从这 14 个唤醒 PIN 中选择最多两个映射为实际的 PIN 唤醒源，选择寄存器是 PMUC 的

CR_PIN0_SEL 与 CR_PIN1_SEL。

standby 模式支持最多 14 个唤醒 PIN 同时作为唤醒源。

deepsleep 模式除支持最多 14 个唤醒 PIN 同时作为唤醒源以外，还支持子系统内任意通用 IO 唤醒。例如，HPSYS 进入 deepsleep 模式以后，不仅能够被 14 个唤醒 PIN 中的任意一个唤醒 (唤醒状态位是 HPSYS_AON 的 WSR_PIN0~13)，也能够被任意 IO(PA) 唤醒 (唤醒状态位是 HPSYS_AON 的 WSR_GPIO1，具体唤醒的 IO 需要在 GPIO 寄存器内查询)。

支持唤醒 PIN 功能的通用 IO(PB32~PB36，PA50~PA54) 除原有的 IO 输入通路以外，另有一路永久使能的输入通路用于唤醒 PIN 功能，因此不论芯片是否处于低功耗模式，都需要保证这些 IO 在未翻转时不能处于中间态电平，否则会产生漏电。

当芯片处于 hibernate 模式，所有通用 IO 在 PINMUX 寄存器中的上下拉电阻配置不生效，因此如果芯片外部电路不能保证支持唤醒 PIN 功能的 IO(PB32~PB36，PA50~PA54) 处于确定的高电平或低电平，那么在进入 hibernate 模式之前还需要额外配置 RTC 中的 PAWKUP 与 PBWKUP 寄存器使能上拉或下拉电阻。应当注意 PINMUX 寄存器与 RTC 寄存器中的上下拉电阻配置会同时生效，配置时应当注意避免冗余与冲突，推荐仅通过 RTC 寄存器配置。

5.14 低功耗模式下的 IO 状态

HPSYS 在 active 模式与 sleep 模式下，IO(PA)，IO(SA) 与 IO(SB) 正常工作，输出可正常翻转，可产生 IO 中断。

HPSYS 进入 deepsleep 模式以后，IO(PA)，IO(SA) 与 IO(SB) 进入睡眠模式，输入使能、输出使能、上下拉电阻等配置保持不变，输出保持前值，停止翻转，无法产生 IO 中断，但可产生 IO(PA) 唤醒。支持唤醒 PIN 功能的 IO(PA) 还可产生 PIN 唤醒。IO(PB) 与 IO(PBR) 的工作不受影响。

HPSYS 进入 standby 模式以后，IO(PA)，IO(SA) 与 IO(SB) 进入 retention 模式，输入使能、输出使能、上下拉电阻等配置保持不变，输出保持前值，停止翻转，无法产生 IO 中断与 IO(PA) 唤醒。支持唤醒 PIN 功能的 IO(PA) 可产生 PIN 唤醒。IO(PB) 与 IO(PBR) 的工作不受影响。

LPSYS 在 active 模式与 sleep 模式下，IO(PB) 与 IO(SC) 正常工作，输出可正常翻转，可产生 IO 中断。

LPSYS 进入 deepsleep 模式以后，IO(PB) 与 IO(SC) 进入睡眠模式，输入使能、输出使能、上下拉电阻等配置保持不变，输出保持前值，停止翻转，无法产生 IO 中断，但可产生 IO(PB) 唤醒。支持唤醒 PIN 功能的 IO(PB) 还可产生 PIN 唤醒。IO(PA) 与 IO(PBR) 的工作不受影响。

LPSYS 进入 standby 模式以后，IO(PB) 与 IO(SC) 进入 retention 模式，输入使能、输出使能、上下拉电阻等配置保持不变，输出保持前值，停止翻转，无法产生 IO 中断与 IO(PB) 唤醒。支持唤醒 PIN 功能的 IO(PB) 可产生 PIN 唤醒。IO(PA) 与 IO(PBR) 的工作不受影响。

芯片进入 hibernate 模式以后，所有合封 IO 以及不支持唤醒 PIN 功能的 IO(PA) 与 IO(PB) 进入关断模式，输入使能与输出使能关闭，上下拉电阻关闭，IO 表现为高阻，无法产生 IO 中断与唤醒。支持唤醒 PIN 功能的 IO(PA) 与 IO(PB) 进入唤醒模式，可产生 PIN 唤醒，上下拉电阻由 RTC 寄存器配置决定。IO(PBR) 工作不受影响，可保持输出 (除 LPTIM3 的 PWM)，并可产生 PIN 唤醒。

表 5-3: IO 工作状态

IO	功能	active	sleep	deepsleep	standby	hibernate
PA00~PA49 PA55~PA78 PB00~PB31	输入使能	工作	工作	保持	保持	无效
	输出使能	工作	工作	保持	保持	无效
	输出电平	可翻转	可翻转	保持	保持	高阻
	上下拉电阻	有效	有效	保持	保持	无效
	GPIO 中断	有	有	无	无	无
	IO 唤醒	有	有	有	无	无
	PIN 唤醒	无	无	无	无	无
PA50~PA54 PB32~PB36	输入使能	工作	工作	保持	保持	无效
	输出使能	工作	工作	保持	保持	无效
	输出电平	可翻转	可翻转	保持	保持	无效
	上下拉电阻	有效	有效	有效	有效	有效
	GPIO 中断	有	有	无	无	无
	IO 唤醒	有	有	有	无	无
	PIN 唤醒	有	有	有	有	有
PBR00~PBR03	输入使能	工作	工作	工作	工作	工作
	输出使能	工作	工作	工作	工作	工作
	输出电平	可翻转	可翻转	可翻转	可翻转	可翻转
	上下拉电阻	有效	有效	有效	有效	有效
	GPIO 中断	无	无	无	无	无
	IO 唤醒	无	无	无	无	无
	PIN 唤醒	有	有	有	有	有
SA00~SA12 SB00~SB12 SC00~SC05	输入使能	工作	工作	保持	保持	无效
	输出使能	工作	工作	保持	保持	无效
	输出电平	可翻转	可翻转	保持	保持	高阻
	上下拉电阻	有效	有效	保持	保持	无效
	GPIO 中断	无	无	无	无	无
	IO 唤醒	无	无	无	无	无
	PIN 唤醒	无	无	无	无	无

5.15 避免 IO 漏电

IO 漏电是芯片低功耗调试中经常遇到的问题。常见的 IO 漏电有以下几类：

- 短路漏电。输出高电平的 IO，与另一个输出低电平的 IO(可能来自其它器件) 通过芯片外部电路短路，会产生较大电流，严重时可造成芯片损坏。
- 输出导通漏电。IO 输出高电平时，芯片内部或外部存在下拉电阻，产生导通电流。或 IO 输出低电平时，芯片内部或外部存在上拉电阻，产生导通电流。
- 上下拉电阻导通漏电。某个 IO 在芯片内部或外部同时存在上拉电阻和下拉电阻，产生导通电流。
- 输入中间态电平漏电。IO 输入通路导通时，输入端处于中间态电平，使得 IO 内部产生导通电流。这种漏电较为隐蔽，且可表现为浮动变化的漏电电流。

针对第 2 类漏电，对于配置成模块输出或 GPIO 推挽输出的 IO，可关闭上下拉电阻 (PE 设为 0)。

针对第 3 类漏电，应检查芯片外部电路，确保上拉与下拉电阻不存在冲突。对于支持唤醒 PIN 功能的通用 IO(PB32~PB36，PA50~PA54)，应通过 RTC 中的 PAWKUP 与 PBWKUP 寄存器配置上下拉电阻，并关闭 PIN-MUX 寄存器中的上下拉电阻配置，避免配置冲突。

针对第 4 类漏电，除能明确输入电平是高电平或低电平的 IO 以外，应采用下述配置方法：

- 不需要输入功能的通用 IO，关闭输入使能 (IE 设为 0)。
- 不作为唤醒 PIN 使用的 IO(PBR)，关闭输入使能 (IE 设为 0)。
- 作为唤醒 PIN 使用的 IO(PBR)，设置芯片内部的上拉或下拉电阻。
- 支持唤醒 PIN 功能的通用 IO (PB32~PB36，PA50~PA54)，通过设置 RTC 中的 PAWKUP 与 PBWKUP 寄存器配置上下拉电阻。

当怀疑存在 IO 漏电时，可对各 IO 进行如下检查

表 5-4: IO 工作状态

IO	如果配置为 GPIO 功能并且开启了输出使能，或配置为其它模块的输出信号	输入使能时	输入使能与输出使能都关闭时
PA00~PA49 PA55~PA78 PB00~PB31	检查输出值与 PINMUX 配置的上下拉是否匹配 检查输出值与外部电路的上下拉是否匹配 检查是否输出高电平，但 IO 连接的外部器件供电关闭	检查 IO 连接的外部器件是否能提供确定电平 检查 PINMUX 是否配置了合理的上下拉	检查 PINMUX 配置的上下拉与外部电路的电平是否冲突
PA50~PA54 PB32~PB36	检查输出值与 RTC 配置的上下拉是否匹配 检查 PINMUX 与 RTC 配置的上下拉是否冲突 检查输出值与外部电路的上下拉是否匹配 检查是否输出高电平，但 IO 连接的外部器件供电关闭	检查 IO 连接的外部器件是否能提供确定电平 检查 PINMUX 与 RTC 是否配置了合理的上下拉	检查 IO 连接的外部器件是否能提供确定电平 检查 PINMUX 与 RTC 是否配置了合理的上下拉
PBR00~PBR03	检查输出值与 RTC 配置的上下拉是否匹配 检查输出值与外部电路的上下拉是否匹配 检查是否输出高电平，但 IO 连接的外部器件供电关闭	检查 IO 连接的外部器件是否能提供确定电平 检查 RTC 是否配置了合理的上下拉	检查 RTC 配置的上下拉与外部电路的电平是否冲突

芯片提供的 IO 数目众多，当无法确定哪些 IO 发生漏电时，可以先将所有通用 IO (PB00~PB36，PA00~PA78) 在 PINMUX 中配置成非输入高阻状态 (IE=0,PE=0,OE=0)，将所有低功耗 IO(PBR00~PBR03) 在 RTC 中配置成无输入高阻状态 (IE=0,PE=0,OE=0)，并将支持唤醒 PIN 功能的通用 IO (PB32~PB36，PA50~PA54) 在 RTC 寄存器中设置合理的上下拉电阻。这种状态下芯片 IO 不会产生漏电。再分批恢复 IO 的配置，找到发生漏电的 IO 并消除漏电因素。

Hibernate 模式下，芯片 IO 的漏电只会发生在唤醒 PIN 上，只需排查唤醒 PIN 的 IO 配置。

5.16 避免合封 IO 漏电

合封 IO 的供电电源同时也提供给对应的合封存储器，因此合封存储器的漏电也会体现在合封 IO 的电源上。常见的合封 IO 漏电有以下两种：

1. 芯片进入低功耗模式，但合封存储器未进入低功耗状态。合封的 NOR flash 或 pSRAM 在未访问的待机状态下也会消耗电流 (与存储器型号有关，通常约 10~200uA 量级)，这部分漏电在芯片进入低功耗模式后更加凸显，因此推荐芯片在进入 deepsleep 或 standby 模式之前先让合封存储器进入低功耗状态 (漏电约 1~10uA 量级)，芯片醒来以后再让合封存储器退出低功耗状态。合封的 pSRAM 可通过指令进入 half sleep 模式，合封的 NOR flash 可通过指令进入 deep power down 模式，这些模式可以显著降低存储器的漏电。

2. 合封 IO 不可控造成合封存储器漏电。当芯片进入 hibernate 模式，合封 IO 表现为高阻浮动电平。如果此时合封 IO 的电源仍在供电，有可能使得合封存储器进入高漏电状态 (如 CS 管脚为浮动的低电平或中间电平，可能产生上百 uA 到若干 mA 的漏电)。因此在芯片进入 hibernate 模式之前，应关闭合封 IO 的供电电源，避免合封存储器的漏电。芯片预留了 PBR00 可用于控制合封电源。默认配置下，当芯片上电或从 hibernate 唤醒以后 PBR00 自动输出高，而进入 hibernate 模式以后 PBR00 自动输出低。可将 PBR00 用于使能外部电源开关，从而自动控制合封电源的开启与关闭，避免漏电。如果合封 IO 的供电只能保持常供电无法控制，应避免使用芯片的 hibernate 模式，可使用 standby 模式代替。

5.17 HPSYS_PINMUX 寄存器

表 5-5: HPSYS_PINMUX 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x0			**PAD_SA00**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x4			**PAD_SA01**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x8			**PAD_SA02**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0xC			**PAD_SA03**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x10			**PAD_SA04**	

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表 5-5: HPSYS_PINMUX 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x14			**PAD_SA05**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h1	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x18			**PAD_SA06**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h1	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x1C			**PAD_SA07**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x20			**PAD_SA08**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength

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表 5-5: HPSYS_PINMUX 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x24			**PAD_SA09**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x28			**PAD_SA10**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x2C			**PAD_SA11**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x30			**PAD_SA12**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h1	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down

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表 5-5: HPSYS_PINMUX 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x34			**PAD_SB00**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h1	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x38			**PAD_SB01**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x3C			**PAD_SB02**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x40			**PAD_SB03**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h1	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x44			**PAD_SB04**	
[31:12]			RSVD	

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表 5-5: HPSYS_PINMUX 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x48			**PAD_SB05**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h1	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x4C			**PAD_SB06**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h1	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x50			**PAD_SB07**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x54			**PAD_SB08**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate

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表 5-5: HPSYS_PINMUX 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x58			**PAD_SB09**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x5C			**PAD_SB10**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x60			**PAD_SB11**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x64			**PAD_SB12**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h1	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device

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表 5-5: HPSYS_PINMUX 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[3:0]	rw	4'h0	FSEL	Function Select
0x68			**PAD_PA00**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x6C			**PAD_PA01**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x70			**PAD_PA02**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x74			**PAD_PA03**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x78			**PAD_PA04**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW

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表 5-5: HPSYS_PINMUX 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x7C			**PAD_PA05**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x80			**PAD_PA06**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h1	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x84			**PAD_PA07**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x88			**PAD_PA08**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input

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表 5-5: HPSYS_PINMUX 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x8C			**PAD_PA09**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h1	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x90			**PAD_PA10**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h1	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x94			**PAD_PA11**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x98			**PAD_PA12**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h1	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select

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表 5-5: HPSYS_PINMUX 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
0x9C			**PAD_PA13**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0xA0			**PAD_PA14**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0xA4			**PAD_PA15**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0xA8			**PAD_PA16**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0xAC			**PAD_PA17**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS	Drive Select. Logic LOW selects 4mA drive,logic HIGH selects 20mA drive

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表 5-5: HPSYS_PINMUX 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[9]			RSVD	
[8]	rw	1'h0	MODE	Mode Select. Logic LOW enables GPIO mode,logic HIGH enables I2C mode
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h1	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0xB0			**PAD_PA18**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS	Drive Select. Logic LOW selects 4mA drive,logic HIGH selects 20mA drive
[9]			RSVD	
[8]	rw	1'h0	MODE	Mode Select. Logic LOW enables GPIO mode,logic HIGH enables I2C mode
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h1	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0xB4			**PAD_PA19**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0xB8			**PAD_PA20**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0xBC			**PAD_PA21**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer

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表 5-5: HPSYS_PINMUX 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0xC0			**PAD_PA22**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h1	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0xC4			**PAD_PA23**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0xC8			**PAD_PA24**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0xCC			**PAD_PA25**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0xD0			**PAD_PA26**	

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表 5-5: HPSYS_PINMUX 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0xD4			**PAD_PA27**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h1	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0xD8			**PAD_PA28**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h1	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0xDC			**PAD_PA29**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0xE0			**PAD_PA30**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength

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表 5-5: HPSYS_PINMUX 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0xE4			**PAD_PA31**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0xE8			**PAD_PA32**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0xEC			**PAD_PA33**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0xF0			**PAD_PA34**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h1	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down

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表 5-5: HPSYS_PINMUX 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0xF4			**PAD_PA35**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0xF8			**PAD_PA36**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h1	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0xFC			**PAD_PA37**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x100			**PAD_PA38**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x104			**PAD_PA39**	
[31:12]			RSVD	

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表 5-5: HPSYS_PINMUX 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x108			**PAD_PA40**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x10C			**PAD_PA41**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x110			**PAD_PA42**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x114			**PAD_PA43**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate

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表 5-5: HPSYS_PINMUX 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x118			**PAD_PA44**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x11C			**PAD_PA45**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x120			**PAD_PA46**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x124			**PAD_PA47**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device

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表 5-5: HPSYS_PINMUX 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[3:0]	rw	4'h0	FSEL	Function Select
0x128			**PAD_PA48**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS	Drive Select. Logic LOW selects 4mA drive,logic HIGH selects 20mA drive
[9]			RSVD	
[8]	rw	1'h0	MODE	Mode Select. Logic LOW enables GPIO mode,logic HIGH enables I2C mode
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h1	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x12C			**PAD_PA49**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS	Drive Select. Logic LOW selects 4mA drive,logic HIGH selects 20mA drive
[9]			RSVD	
[8]	rw	1'h0	MODE	Mode Select. Logic LOW enables GPIO mode,logic HIGH enables I2C mode
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h1	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x130			**PAD_PA50**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x134			**PAD_PA51**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x138			**PAD_PA52**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW

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表 5-5: HPSYS_PINMUX 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x13C			**PAD_PA53**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x140			**PAD_PA54**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x144			**PAD_PA55**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x148			**PAD_PA56**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input

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表 5-5: HPSYS_PINMUX 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x14C			**PAD_PA57**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x150			**PAD_PA58**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h1	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x154			**PAD_PA59**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x158			**PAD_PA60**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select

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表 5-5: HPSYS_PINMUX 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
0x15C			**PAD_PA61**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x160			**PAD_PA62**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h1	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x164			**PAD_PA63**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h1	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x168			**PAD_PA64**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x16C			**PAD_PA65**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength

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表 5-5: HPSYS_PINMUX 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x170			**PAD_PA66**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x174			**PAD_PA67**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x178			**PAD_PA68**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x17C			**PAD_PA69**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer

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表 5-5: HPSYS_PINMUX 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x180			**PAD_PA70**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x184			**PAD_PA71**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x188			**PAD_PA72**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x18C			**PAD_PA73**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x190			**PAD_PA74**	

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表 5-5: HPSYS_PINMUX 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x194			**PAD_PA75**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h1	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x198			**PAD_PA76**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h1	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x19C			**PAD_PA77**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select
0x1A0			**PAD_PA78**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength

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表 5-5: HPSYS_PINMUX 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3:0]	rw	4'h0	FSEL	Function Select

5.18 HPSYS_CFG 寄存器

表 5-6: HPSYS_CFG 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00			**BMR**	Boot Mode Register
[31:1]			RSVD	
[0]	r	1'h0	BOOT_MODE	0 - normal, 1 - download mode
0x04			**IDR**	ID Register
[31:24]	r	8'hC2	SID	Series ID
[23:16]	r	8'h03	CID	Chip ID
[15:8]	r	8'h0	PID	Package ID
[7:0]	r	8'h0	REVID	Revision ID
0x08			**SCR**	Security Control Register
[31:1]			RSVD	
[0]	rw	1'h1	FKEY_MODE	reserved for debug
0x0C			**USBCR**	USB Control register
[31:24]			RSVD1	
[23:16]			RSVD0	
[15:13]	rw	3'h0	DC_TR	reserved for debug
[12]	rw	1'h0	DC_TE	reserved for debug
[11]			RSVD	
[10:8]	rw	3'h0	TX_RTUNE	TX outp impedance tuning 0 = 50 Ohm, 1 = 46 Ohm, 2 = 43 Ohm, 3 = 40 Ohm, 4 = 37.5 Ohm, 5 = 35 Ohm, 6 = 33 Ohm, 7 = 31.5 Ohm
[7]			RSVD	
[6]	rw	1'h0	DP_EN	0:disable dp pull up or pull down 1:enable dp pull or pull down
[5]	rw	1'h0	DM_PD	enable DM 15k Ohm pull down resistor
[4]	rw	1'h0	LDO_LP_EN	2.5V LDO low power mode enable. 0 = 240 uA, 1 = 50 uA
[3:1]	rw	3'h0	LDO_VSEL	2.5V LDO output voltage setting 0 = 2.40 V, 1 = 2.47 V, 2 = 2.53 V, 3 = 2.60 V, 4 = 2.60 V, 5 = 2.67 V, 6 = 2.73 V, 7 = 2.8 V
[0]	rw	1'h0	USB_EN	USB PHY enable, turn on power swith, power up LDO and bias
0x10			**MCR**	Memory Control register
[31]	rw	1'b0	FORCE_ON	reserved for debug
[30:14]			RSVD	
[13]	rw	1'b0	PD_OTHER	reserved for debug
[12:7]			RSVD	
[6]	rw	1'b0	PD_RAM3	reserved for debug
[5]	rw	1'b0	PD_RAM2	reserved for debug

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表 5-6: HPSYS_CFG 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[4]	rw	1'b0	PD_RAM1	reserved for debug
[3]	rw	1'b0	PD_RAM0	reserved for debug
[2]	rw	1'b0	PD_CACHE	reserved for debug
[1]	rw	1'b0	PD_ITCM	reserved for debug
[0]	rw	1'b0	PD_ROM	reserved for debug
0x14			**ULPMCR**	ULP Memory Control register
[31]	rw	1'h0	FORCE_ON	reserved for debug
[30:13]			RSVD	
[12:10]	rw	3'b000	WPULSE	reserved for debug
[9:7]	rw	3'b100	WA	reserved for debug
[6:5]	rw	2'b00	RA	reserved for debug
[4]	rw	1'b1	RME	reserved for debug
[3:2]			RSVD	
[1:0]	rw	2'b11	RM	reserved for debug
0x18			**RTC_TR**	Mirrored RTC Time Register
[31]	r	1'h0	PM	AM/PM notation 0: AM 1: PM
[30:29]	r	2'h0	HT	Hour tens in BCD format
[28:25]	r	4'h0	HU	Hour units in BCD format
[24:22]	r	3'h0	MNT	Minute tens in BCD format
[21:18]	r	4'h0	MNU	Minute units in BCD format
[17:15]	r	3'h0	ST	Second tens in BCD format
[14:11]	r	4'h0	SU	Second units in BCD format
[10]			RSVD	
[9:0]	r	10'h0	SS	Sub-second counter
0x1C			**RTC_DR**	Mirrored RTC Date Register
[31]	r	1'h0	ERR	reserved for debug
[30:25]			RSVD	
[24]	r	1'h0	CB	Century flag
[23:20]	r	4'h0	YT	Year tens in BCD format
[19:16]	r	4'h0	YU	Year units in BCD format
[15:13]	r	3'h1	WD	Week day units 000: forbidden 001: Monday ... 111: Sunday
[12]	r	1'h0	MT	Month tens in BCD format
[11:8]	r	4'h1	MU	Month units in BCD format
[7:6]			RSVD	
[5:4]	r	2'h0	DT	Date tens in BCD format
[3:0]	r	4'h1	DU	Date units in BCD format
0x20			**DBGR**	Debug Select Register
[31]			RSVD	
[30]	r	1'h0	LP2HP_NMIF	LP2HP NMI interrupt flag
[29]	rw	1'h0	LP2HP_NMIE	LP2HP NMI interrupt enable
[28]	rw	1'h0	HP2LP_NMI	set 1 to send NMI interrupt to LCPU
[27]	rw	1'b0	CLK_EN	reserved for debug

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表 5-6: HPSYS_CFG 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[26:24]	rw	3'b0	CLK_SEL	reserved for debug
[23:16]	rw	8'h0	BITEN_H	reserved for debug
[15:8]	rw	8'h0	BITEN_L	reserved for debug
[7:4]	rw	4'h0	SEL_H	reserved for debug
[3:0]	rw	4'h0	SEL_L	reserved for debug
0x24			**CAU2_CR**	CAU2 Control Register
[31:13]			RSVD	
[12:10]	rw	3'h0	DC_MR	reserved for debug
[9:7]	rw	3'h0	DC_BR	reserved for debug
[6:4]	rw	3'h0	DC_TR	reserved for debug
[3:2]			RSVD	
[1]	rw	1'b0	HPBG_EN	reserved for debug
[0]	rw	1'b0	HPBG_VDDPSW_EN	reserved for debug
0x28			**CAU2_RSVD1**	CAU2 RSVD Register1
[31:24]			RSVD	
[23:16]	rw	8'h0	RESERVE2	reserved for debug
[15:8]	rw	8'h0	RESERVE1	reserved for debug
[7:0]	rw	8'h0	RESERVE0	reserved for debug
0x2C			**CAU2_RSVD2**	CAU2 RSVD Register2
[31:24]			RSVD	
[23:16]	r	8'h0	RESERVE5	reserved for debug
[15:8]	r	8'h0	RESERVE4	reserved for debug
[7:0]	r	8'h0	RESERVE3	reserved for debug
0x38			**SYS_RSVD**	HPSYS RSVD Register
[31:24]	r	8'h0	RESERVE3	reserved for debug
[23:16]	rw	8'hff	RESERVE2	reserved for debug
[15:8]	rw	8'h0	RESERVE1	reserved for debug
[7:0]	rw	8'h0	RESERVE0	reserved for debug
0x3C			**LPIRQ**	Interrupt Selection for LCPU
[31]	rw1c	1'h0	IF3	hp2lp3 interrupt status. Write 1 to clear.
[30]			RSVD	
[29:24]	rw	6'h0	SEL3	select hp2lp3 interrupt source
[23]	rw1c	1'h0	IF2	hp2lp2 interrupt status. Write 1 to clear.
[22]			RSVD	
[21:16]	rw	6'h0	SEL2	select hp2lp2 interrupt source
[15]	rw1c	1'h0	IF1	hp2lp1 interrupt status. Write 1 to clear.
[14]			RSVD	
[13:8]	rw	6'h0	SEL1	select hp2lp1 interrupt source
[7]	rw1c	1'h0	IF0	hp2lp0 interrupt status. Write 1 to clear.
[6]			RSVD	
[5:0]	rw	6'h0	SEL0	select hp2lp0 interrupt source
0x5C			**SYSCR**	System Configure Register
[31:5]			RSVD	
[4]	rw	1'h0	SDNAND	0: MPI3 AHB space is allocated to MPI3 1: MPI3 AHB space is allocated to SDMMC2
[3]	rw	1'h0	REMAP	reserved for debug
[2]	rw	1'h0	HEXOKAYS	reserved for debug
[1]	rw	1'h0	HEXOKAYC	reserved for debug

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表 5-6: HPSYS_CFG 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[0]	rw	1'h0	WDT1_REBOOT	If set to 1, WDT1 reset will reboot the whole chip
0x60			**I2C1_PINR**	I2C1 Pin Register
[31:15]			RSVD	
[14:8]	rw	7'h7f	SDA_PIN	Connect function pin to selected IO(PA). 0 to 78 for PA00 to PA78. Other values for floating.
[7]			RSVD	
[6:0]	rw	7'h7f	SCL_PIN	Connect function pin to selected IO(PA). 0 to 78 for PA00 to PA78. Other values for floating.
0x64			**I2C2_PINR**	I2C2 Pin Register
[31:15]			RSVD	
[14:8]	rw	7'h7f	SDA_PIN	Connect function pin to selected IO(PA). 0 to 78 for PA00 to PA78. Other values for floating.
[7]			RSVD	
[6:0]	rw	7'h7f	SCL_PIN	Connect function pin to selected IO(PA). 0 to 78 for PA00 to PA78. Other values for floating.
0x68			**I2C3_PINR**	I2C3 Pin Register
[31:15]			RSVD	
[14:8]	rw	7'h7f	SDA_PIN	Connect function pin to selected IO(PA). 0 to 78 for PA00 to PA78. Other values for floating.
[7]			RSVD	
[6:0]	rw	7'h7f	SCL_PIN	Connect function pin to selected IO(PA). 0 to 78 for PA00 to PA78. Other values for floating.
0x6C			**I2C4_PINR**	I2C4 Pin Register
[31:15]			RSVD	
[14:8]	rw	7'h7f	SDA_PIN	Connect function pin to selected IO(PA). 0 to 78 for PA00 to PA78. Other values for floating.
[7]			RSVD	
[6:0]	rw	7'h7f	SCL_PIN	Connect function pin to selected IO(PA). 0 to 78 for PA00 to PA78. Other values for floating.
0x70			**USART1_PINR**	USART1 Pin Register
[31]			RSVD	
[30:24]	rw	7'h7f	CTS_PIN	Connect function pin to selected IO(PA). 0 to 78 for PA00 to PA78. Other values for floating.
[23]			RSVD	
[22:16]	rw	7'h7f	RTS_PIN	Connect function pin to selected IO(PA). 0 to 78 for PA00 to PA78. Other values for floating.
[15]			RSVD	

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表 5-6: HPSYS_CFG 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[14:8]	rw	7'h7f	RXD_PIN	Connect function pin to selected IO(PA). 0 to 78 for PA00 to PA78. Other values for floating.
[7]			RSVD	
[6:0]	rw	7'h7f	TXD_PIN	Connect function pin to selected IO(PA). 0 to 78 for PA00 to PA78. Other values for floating.
0x74			**USART2_PINR**	USART2 Pin Register
[31]			RSVD	
[30:24]	rw	7'h7f	CTS_PIN	Connect function pin to selected IO(PA). 0 to 78 for PA00 to PA78. Other values for floating.
[23]			RSVD	
[22:16]	rw	7'h7f	RTS_PIN	Connect function pin to selected IO(PA). 0 to 78 for PA00 to PA78. Other values for floating.
[15]			RSVD	
[14:8]	rw	7'h7f	RXD_PIN	Connect function pin to selected IO(PA). 0 to 78 for PA00 to PA78. Other values for floating.
[7]			RSVD	
[6:0]	rw	7'h7f	TXD_PIN	Connect function pin to selected IO(PA). 0 to 78 for PA00 to PA78. Other values for floating.
0x78			**USART3_PINR**	USART3 Pin Register
[31]			RSVD	
[30:24]	rw	7'h7f	CTS_PIN	Connect function pin to selected IO(PA). 0 to 78 for PA00 to PA78. Other values for floating.
[23]			RSVD	
[22:16]	rw	7'h7f	RTS_PIN	Connect function pin to selected IO(PA). 0 to 78 for PA00 to PA78. Other values for floating.
[15]			RSVD	
[14:8]	rw	7'h7f	RXD_PIN	Connect function pin to selected IO(PA). 0 to 78 for PA00 to PA78. Other values for floating.
[7]			RSVD	
[6:0]	rw	7'h7f	TXD_PIN	Connect function pin to selected IO(PA). 0 to 78 for PA00 to PA78. Other values for floating.
0x7C			**GPTIM1_PINR**	GPTIM1 Pin Register
[31]			RSVD	
[30:24]	rw	7'h7f	CH4_PIN	Connect function pin to selected IO(PA). 0 to 78 for PA00 to PA78. Other values for floating.
[23]			RSVD	

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表 5-6: HPSYS_CFG 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[22:16]	rw	7'h7f	CH3_PIN	Connect function pin to selected IO(PA). 0 to 78 for PA00 to PA78. Other values for floating.
[15]			RSVD	
[14:8]	rw	7'h7f	CH2_PIN	Connect function pin to selected IO(PA). 0 to 78 for PA00 to PA78. Other values for floating.
[7]			RSVD	
[6:0]	rw	7'h7f	CH1_PIN	Connect function pin to selected IO(PA). 0 to 78 for PA00 to PA78. Other values for floating.
0x80			**GPTIM2_PINR**	GPTIM2 Pin Register
[31]			RSVD	
[30:24]	rw	7'h7f	CH4_PIN	Connect function pin to selected IO(PA). 0 to 78 for PA00 to PA78. Other values for floating.
[23]			RSVD	
[22:16]	rw	7'h7f	CH3_PIN	Connect function pin to selected IO(PA). 0 to 78 for PA00 to PA78. Other values for floating.
[15]			RSVD	
[14:8]	rw	7'h7f	CH2_PIN	Connect function pin to selected IO(PA). 0 to 78 for PA00 to PA78. Other values for floating.
[7]			RSVD	
[6:0]	rw	7'h7f	CH1_PIN	Connect function pin to selected IO(PA). 0 to 78 for PA00 to PA78. Other values for floating.
0x84			**ETR_PINR**	GPTIM ETR Pin Register
[31:15]			RSVD	
[14:8]	rw	7'h7f	ETR2_PIN	Connect GPTIM2_ETR to selected IO(PA). 0 to 44 for PA00 to PA44. Other values for floating.
[7]			RSVD	
[6:0]	rw	7'h7f	ETR1_PIN	Connect GPTIM1_ETR to selected IO(PA). 0 to 44 for PA00 to PA44. Other values for floating.
0x88			**LPTIM1_PINR**	LPTIM1 Pin Register
[31:23]			RSVD	
[22:16]	rw	7'h7f	ETR_PIN	Connect function pin to selected IO(PA). 0 to 78 for PA00 to PA78. Other values for floating.
[15]			RSVD	
[14:8]	rw	7'h7f	OUT_PIN	Connect function pin to selected IO(PA). 0 to 78 for PA00 to PA78. Other values for floating.
[7]			RSVD	

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表 5-6: HPSYS_CFG 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[6:0]	rw	7'h7f	IN_PIN	Connect function pin to selected IO(PA). 0 to 78 for PA00 to PA78. Other values for floating.

5.19 HPSYS_GPIO 寄存器

表 5-7: HPSYS_GPIO 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00			**DIR0**	Data Input Register
[31:0]	r	32'h0	IN	GPIO[31:0] input value
0x04			**DOR0**	Data Output Register
[31:0]	rw	32'h0	OUT	GPIO[31:0] output value if output enabled
0x08			**DOSR0**	Data Output Set Register
[31:0]	w	32'h0	DOS	set 1 to pull up output of corresponding GPIO[31:0]
0x0C			**DOCR0**	Data Output Clear Register
[31:0]	w	32'h0	DOC	set 1 to pull down output of corresponding GPIO[31:0]
0x10			**DOER0**	Data Output Enable Register
[31:0]	rw	32'h0	DOE	GPIO[31:0] output enable
0x14			**DOESR0**	Data Output Enable Set Register
[31:0]	w	32'h0	DOES	set 1 to enable output of corresponding GPIO[31:0]
0x18			**DOECR0**	Data Output Enable Clear Register
[31:0]	w	32'h0	DOEC	set 1 to disable output of corresponding GPIO[31:0]
0x1C			**IER0**	Interrupt Enable Register
[31:0]	rw	32'h0	IER	GPIO[31:0] interrupt enable
0x20			**IESR0**	Interrupt Enable Set Register
[31:0]	w	32'h0	IES	set 1 to enable interrupt of corresponding GPIO[31:0]
0x24			**IECR0**	Interrupt Enable Clear Register
[31:0]	w	32'h0	IEC	set 1 to disable interrupt of corresponding GPIO[31:0]
0x28			**ITR0**	Interrupt Type Register
[31:0]	rw	32'h0	ITR	GPIO[31:0] interrupt type
0x2C			**ITSR0**	Interrupt Type Set Register
[31:0]	w	32'h0	ITS	set 1 for edge-sensitive interrupt mode of corresponding GPIO[31:0]
0x30			**ITCR0**	Interrupt Type Clear Register
[31:0]	w	32'h0	ITC	set 1 for level-sensitive interrupt mode of corresponding GPIO[31:0]
0x34			**IPHR0**	Interrupt Polarity High Register
[31:0]	rw	32'h0	IPH	rising edge in edge mode, or high level in level mode of corresponding GPIO[31:0]
0x38			**IPHSR0**	Interrupt Polarity High Set Register
[31:0]	w	32'h0	IPHS	set 1 for rising edge in edge mode, or high level in level mode of corresponding GPIO[31:0]
0x3C			**IPHCR0**	Interrupt Polarity High Clear Register
[31:0]	w	32'h0	IPHC	set 1 for disable rising edge in edge mode, or high level in level mode of corresponding GPIO[31:0]
0x40			**IPLR0**	Interrupt Polarity Low Register
[31:0]	rw	32'h0	IPL	falling edge in edge mode, or low level in level mode of corresponding GPIO[31:0]
0x44			**IPLSR0**	Interrupt Polarity Low Set Register

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表 5-7: HPSYS_GPIO 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:0]	w	32'h0	IPLS	set 1 for falling edge in edge mode, or low level in level mode of corresponding GPIO[31:0]
0x48			**IPLCR0**	Interrupt Polarity Low Clear Register
[31:0]	w	32'h0	IPLC	set 1 for disable falling edge in edge mode, or low level in level mode of corresponding GPIO[31:0]
0x4C			**ISR0**	Interrupt Status Register
[31:0]	rw	32'h0	IS	Interrupt status. Write 1 will clear interrupt status of corresponding GPIO[31:0]
0x60			**OEMR0**	output mode Register
[31:0]	rw	32'h0	OEM	output mode of corresponding GPIO[31:0]
0x64			**OEMSR0**	output mode Set Register
[31:0]	w	32'h0	OEMS	output mode Set of corresponding GPIO[31:0]
0x68			**OEMCR0**	output mode Clear Register
[31:0]	w	32'h0	OEMC	output mode Clear of corresponding GPIO[31:0]
0x80			**DIR1**	Data Input Register
[31:0]	r	32'h0	IN	GPIO[63:32] input value
0x84			**DOR1**	Data Output Register
[31:0]	rw	32'h0	OUT	GPIO[63:32] output value if output enabled
0x88			**DOSR1**	Data Output Set Register
[31:0]	w	32'h0	DOS	set 1 to pull up output of corresponding GPIO[63:32]
0x8C			**DOCR1**	Data Output Clear Register
[31:0]	w	32'h0	DOC	set 1 to pull down output of corresponding GPIO[63:32]
0x90			**DOER1**	Data Output Enable Register
[31:0]	rw	32'h0	DOE	GPIO[63:32] output enable
0x94			**DOESR1**	Data Output Enable Set Register
[31:0]	w	32'h0	DOES	set 1 to enable output of corresponding GPIO[63:32]
0x98			**DOECR1**	Data Output Enable Clear Register
[31:0]	w	32'h0	DOEC	set 1 to disable output of corresponding GPIO[63:32]
0x9C			**IER1**	Interrupt Enable Register
[31:0]	rw	32'h0	IER	GPIO[63:32] interrupt enable
0xA0			**IESR1**	Interrupt Enable Set Register
[31:0]	w	32'h0	IES	set 1 to enable interrupt of corresponding GPIO[63:32]
0xA4			**IECR1**	Interrupt Enable Clear Register
[31:0]	w	32'h0	IEC	set 1 to disable interrupt of corresponding GPIO[63:32]
0xA8			**ITR1**	Interrupt Type Register
[31:0]	rw	32'h0	ITR	GPIO[63:32] interrupt type
0xAC			**ITSR1**	Interrupt Type Set Register
[31:0]	w	32'h0	ITS	set 1 for edge-sensitive interrupt mode of corresponding GPIO[63:32]
0xB0			**ITCR1**	Interrupt Type Clear Register
[31:0]	w	32'h0	ITC	set 1 for level-sensitive interrupt mode of corresponding GPIO[63:32]
0xB4			**IPHR1**	Interrupt Polarity High Register
[31:0]	rw	32'h0	IPH	rising edge in edge mode, or high level in level mode of corresponding GPIO[63:32]
0xB8			**IPHSR1**	Interrupt Polarity High Set Register
[31:0]	w	32'h0	IPHS	set 1 for rising edge in edge mode, or high level in level mode of corresponding GPIO[63:32]
0xBC			**IPHCR1**	Interrupt Polarity High Clear Register
[31:0]	w	32'h0	IPHC	set 1 for disable rising edge in edge mode, or high level in level mode of corresponding GPIO[63:32]

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表 5-7: HPSYS_GPIO 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
0xC0			**IPLR1**	Interrupt Polarity Low Register
[31:0]	rw	32'h0	IPL	falling edge in edge mode, or low level in level mode of corresponding GPIO[63:32]
0xC4			**IPLSR1**	Interrupt Polarity Low Set Register
[31:0]	w	32'h0	IPLS	set 1 for falling edge in edge mode, or low level in level mode of corresponding GPIO[63:32]
0xC8			**IPLCR1**	Interrupt Polarity Low Clear Register
[31:0]	w	32'h0	IPLC	set 1 for disable falling edge in edge mode, or low level in level mode of corresponding GPIO[63:32]
0xCC			**ISR1**	Interrupt Status Register
[31:0]	rw	32'h0	IS	Interrupt status. Write 1 will clear interrupt status of corresponding GPIO[63:32]
0xE0			**OEMR1**	output mode Register
[31:0]	rw	32'h0	OEM	output mode of corresponding GPIO[63:32]
0xE4			**OEMSR1**	output mode Set Register
[31:0]	w	32'h0	OEMS	output mode Set of corresponding GPIO[63:32]
0xE8			**OEMCR1**	output mode Clear Register
[31:0]	w	32'h0	OEMC	output mode Clear of corresponding GPIO[63:32]
0x100			**DIR2**	Data Input Register
[31:15]			RSVD	
[14:0]	r	15'h0	IN	GPIO[78:64] input value
0x104			**DOR2**	Data Output Register
[31:15]			RSVD	
[14:0]	rw	15'h0	OUT	GPIO[78:64] output value if output enabled
0x108			**DOSR2**	Data Output Set Register
[31:15]			RSVD	
[14:0]	w	15'h0	DOS	set 1 to pull up output of corresponding GPIO[78:64]
0x10C			**DOCR2**	Data Output Clear Register
[31:15]			RSVD	
[14:0]	w	15'h0	DOC	set 1 to pull down output of corresponding GPIO[78:64]
0x110			**DOER2**	Data Output Enable Register
[31:15]			RSVD	
[14:0]	rw	15'h0	DOE	GPIO[78:64] output enable
0x114			**DOESR2**	Data Output Enable Set Register
[31:15]			RSVD	
[14:0]	w	15'h0	DOES	set 1 to enable output of corresponding GPIO[78:64]
0x118			**DOECR2**	Data Output Enable Clear Register
[31:15]			RSVD	
[14:0]	w	15'h0	DOEC	set 1 to disable output of corresponding GPIO[78:64]
0x11C			**IER2**	Interrupt Enable Register
[31:15]			RSVD	
[14:0]	rw	15'h0	IER	GPIO[78:64] interrupt enable
0x120			**IESR2**	Interrupt Enable Set Register
[31:15]			RSVD	
[14:0]	w	15'h0	IES	set 1 to enable interrupt of corresponding GPIO[78:64]
0x124			**IECR2**	Interrupt Enable Clear Register
[31:15]			RSVD	
[14:0]	w	15'h0	IEC	set 1 to disable interrupt of corresponding GPIO[78:64]
0x128			**ITR2**	Interrupt Type Register

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表 5-7: HPSYS_GPIO 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:15]			RSVD	
[14:0]	rw	15'h0	ITR	GPIO[78:64] interrupt type
0x12C			**ITSR2**	Interrupt Type Set Register
[31:15]			RSVD	
[14:0]	w	15'h0	ITS	set 1 for edge-sensitive interrupt mode of corresponding GPIO[78:64]
0x130			**ITCR2**	Interrupt Type Clear Register
[31:15]			RSVD	
[14:0]	w	15'h0	ITC	set 1 for level-sensitive interrupt mode of corresponding GPIO[78:64]
0x134			**IPHR2**	Interrupt Polarity High Register
[31:15]			RSVD	
[14:0]	rw	15'h0	IPH	rising edge in edge mode, or high level in level mode of corresponding GPIO[78:64]
0x138			**IPHSR2**	Interrupt Polarity High Set Register
[31:15]			RSVD	
[14:0]	w	15'h0	IPHS	set 1 for rising edge in edge mode, or high level in level mode of corresponding GPIO[78:64]
0x13C			**IPHCR2**	Interrupt Polarity High Clear Register
[31:15]			RSVD	
[14:0]	w	15'h0	IPHC	set 1 for disable rising edge in edge mode, or high level in level mode of corresponding GPIO[78:64]
0x140			**IPLR2**	Interrupt Polarity Low Register
[31:15]			RSVD	
[14:0]	rw	15'h0	IPL	falling edge in edge mode, or low level in level mode of corresponding GPIO[78:64]
0x144			**IPLSR2**	Interrupt Polarity Low Set Register
[31:15]			RSVD	
[14:0]	w	15'h0	IPLS	set 1 for falling edge in edge mode, or low level in level mode of corresponding GPIO[78:64]
0x148			**IPLCR2**	Interrupt Polarity Low Clear Register
[31:15]			RSVD	
[14:0]	w	15'h0	IPLC	set 1 for disable falling edge in edge mode, or low level in level mode of corresponding GPIO[78:64]
0x14C			**ISR2**	Interrupt Status Register
[31:15]			RSVD	
[14:0]	rw	15'h0	IS	Interrupt status. Write 1 will clear interrupt status of corresponding GPIO[78:64]
0x160			**OEMR2**	output mode Register
[31:15]			RSVD	
[14:0]	rw	15'h0	OEM	output mode of corresponding GPIO[78:64]
0x164			**OEMSR2**	output mode Set Register
[31:15]			RSVD	
[14:0]	w	15'h0	OEMS	output mode Set of corresponding GPIO[78:64]
0x168			**OEMCR2**	output mode Clear Register
[31:15]			RSVD	
[14:0]	w	15'h0	OEMC	output mode Clear of corresponding GPIO[78:64]

5.20 LPSYS_PINMUX 寄存器

表 5-8: LPSYS_PINMUX 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x0			**PAD_SC00**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h1	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3]			RSVD	
[2:0]	rw	3'h0	FSEL	Function Select
0x4			**PAD_SC01**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3]			RSVD	
[2:0]	rw	3'h0	FSEL	Function Select
0x8			**PAD_SC02**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h0	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h0	PE	Pull Enable. Logic HIGH enables week pull device
[3]			RSVD	
[2:0]	rw	3'h0	FSEL	Function Select
0xC			**PAD_SC03**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h1	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3]			RSVD	
[2:0]	rw	3'h0	FSEL	Function Select

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表 5-8: LPSYS_PINMUX 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
0x10			**PAD_SC04**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h0	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h0	PE	Pull Enable. Logic HIGH enables week pull device
[3]			RSVD	
[2:0]	rw	3'h0	FSEL	Function Select
0x14			**PAD_SC05**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3]			RSVD	
[2:0]	rw	3'h0	FSEL	Function Select
0x18			**PAD_PB00**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS	Drive Select. Logic LOW selects 4mA drive,logic HIGH selects 20mA drive
[9]			RSVD	
[8]	rw	1'h0	MODE	Mode Select. Logic LOW enables GPIO mode,logic HIGH enables I2C mode
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h1	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3]			RSVD	
[2:0]	rw	3'h0	FSEL	Function Select
0x1C			**PAD_PB01**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS	Drive Select. Logic LOW selects 4mA drive,logic HIGH selects 20mA drive
[9]			RSVD	
[8]	rw	1'h0	MODE	Mode Select. Logic LOW enables GPIO mode,logic HIGH enables I2C mode
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h1	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3]			RSVD	
[2:0]	rw	3'h0	FSEL	Function Select

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表 5-8: LPSYS_PINMUX 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
0x20			**PAD_PB02**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3]			RSVD	
[2:0]	rw	3'h0	FSEL	Function Select
0x24			**PAD_PB03**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3]			RSVD	
[2:0]	rw	3'h0	FSEL	Function Select
0x28			**PAD_PB04**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3]			RSVD	
[2:0]	rw	3'h0	FSEL	Function Select
0x2C			**PAD_PB05**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3]			RSVD	
[2:0]	rw	3'h0	FSEL	Function Select

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表 5-8: LPSYS_PINMUX 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
0x30			**PAD_PB06**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3]			RSVD	
[2:0]	rw	3'h0	FSEL	Function Select
0x34			**PAD_PB07**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3]			RSVD	
[2:0]	rw	3'h0	FSEL	Function Select
0x38			**PAD_PB08**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h1	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3]			RSVD	
[2:0]	rw	3'h0	FSEL	Function Select
0x3C			**PAD_PB09**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3]			RSVD	
[2:0]	rw	3'h0	FSEL	Function Select

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表 5-8: LPSYS_PINMUX 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
0x40			**PAD_PB10**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3]			RSVD	
[2:0]	rw	3'h0	FSEL	Function Select
0x44			**PAD_PB11**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3]			RSVD	
[2:0]	rw	3'h0	FSEL	Function Select
0x48			**PAD_PB12**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3]			RSVD	
[2:0]	rw	3'h0	FSEL	Function Select
0x4C			**PAD_PB13**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3]			RSVD	
[2:0]	rw	3'h0	FSEL	Function Select

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表 5-8: LPSYS_PINMUX 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
0x50			**PAD_PB14**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h1	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3]			RSVD	
[2:0]	rw	3'h0	FSEL	Function Select
0x54			**PAD_PB15**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3]			RSVD	
[2:0]	rw	3'h0	FSEL	Function Select
0x58			**PAD_PB16**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3]			RSVD	
[2:0]	rw	3'h0	FSEL	Function Select
0x5C			**PAD_PB17**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h1	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3]			RSVD	
[2:0]	rw	3'h0	FSEL	Function Select

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表 5-8: LPSYS_PINMUX 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
0x60			**PAD_PB18**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h1	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3]			RSVD	
[2:0]	rw	3'h0	FSEL	Function Select
0x64			**PAD_PB19**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h1	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3]			RSVD	
[2:0]	rw	3'h0	FSEL	Function Select
0x68			**PAD_PB20**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3]			RSVD	
[2:0]	rw	3'h0	FSEL	Function Select
0x6C			**PAD_PB21**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3]			RSVD	
[2:0]	rw	3'h0	FSEL	Function Select

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表 5-8: LPSYS_PINMUX 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
0x70			**PAD_PB22**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3]			RSVD	
[2:0]	rw	3'h0	FSEL	Function Select
0x74			**PAD_PB23**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS	Drive Select. Logic LOW selects 4mA drive,logic HIGH selects 20mA drive
[9]			RSVD	
[8]	rw	1'h0	MODE	Mode Select. Logic LOW enables GPIO mode,logic HIGH enables I2C mode
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h1	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3]			RSVD	
[2:0]	rw	3'h0	FSEL	Function Select
0x78			**PAD_PB24**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS	Drive Select. Logic LOW selects 4mA drive,logic HIGH selects 20mA drive
[9]			RSVD	
[8]	rw	1'h0	MODE	Mode Select. Logic LOW enables GPIO mode,logic HIGH enables I2C mode
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h1	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3]			RSVD	
[2:0]	rw	3'h0	FSEL	Function Select
0x7C			**PAD_PB25**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3]			RSVD	
[2:0]	rw	3'h0	FSEL	Function Select

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表 5-8: LPSYS_PINMUX 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
0x80			**PAD_PB26**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3]			RSVD	
[2:0]	rw	3'h0	FSEL	Function Select
0x84			**PAD_PB27**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h0	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h0	PE	Pull Enable. Logic HIGH enables week pull device
[3]			RSVD	
[2:0]	rw	3'h0	FSEL	Function Select
0x88			**PAD_PB28**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3]			RSVD	
[2:0]	rw	3'h0	FSEL	Function Select
0x8C			**PAD_PB29**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3]			RSVD	
[2:0]	rw	3'h0	FSEL	Function Select

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表 5-8: LPSYS_PINMUX 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
0x90			**PAD_PB30**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3]			RSVD	
[2:0]	rw	3'h0	FSEL	Function Select
0x94			**PAD_PB31**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3]			RSVD	
[2:0]	rw	3'h0	FSEL	Function Select
0x98			**PAD_PB32**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3]			RSVD	
[2:0]	rw	3'h0	FSEL	Function Select
0x9C			**PAD_PB33**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3]			RSVD	
[2:0]	rw	3'h0	FSEL	Function Select

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表 5-8: LPSYS_PINMUX 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
0xA0			**PAD_PB34**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3]			RSVD	
[2:0]	rw	3'h0	FSEL	Function Select
0xA4			**PAD_PB35**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3]			RSVD	
[2:0]	rw	3'h0	FSEL	Function Select
0xA8			**PAD_PB36**	
[31:12]			RSVD	
[11]	rw	1'h0	POE	Reserved. Always set to logic LOW
[10]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[9]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[8]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[7]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[6]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[5]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[4]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[3]			RSVD	
[2:0]	rw	3'h0	FSEL	Function Select

5.21 LPSYS_CFG 寄存器

表 5-9: LPSYS_CFG 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00			**SWCR**	SW Control Register
[31:1]			RSVD	
[0]	rw	1'h0	SWSEL	0: SWD connected to HCPU 1: SWD connected to LCPU
0x04			**ULPMCR**	ULP Memory Control register

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表 5-9: LPSYS_CFG 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31]	rw	1'h0	FORCE_ON	reserved for debug
[30]	rw	1'h0	ROM_DIS	reserved for debug
[29:21]			RSVD	
[20]	rw	1'b1	ROM_RME	reserved for debug
[19:18]			RSVD	
[17:16]	rw	2'b10	ROM_RM	reserved for debug
[15:13]			RSVD	
[12:10]	rw	3'b000	RAM_WPULSE	reserved for debug
[9:7]	rw	3'b110	RAM_WA	reserved for debug
[6:5]	rw	2'b01	RAM_RA	reserved for debug
[4]	rw	1'b1	RAM_RME	reserved for debug
[3:2]			RSVD	
[1:0]	rw	2'b00	RAM_RM	reserved for debug
0x08			**RTC_TR**	Mirrored RTC Time Register
[31]	r	1'h0	PM	AM/PM notation 0: AM 1: PM
[30:29]	r	2'h0	HT	Hour tens in BCD format
[28:25]	r	4'h0	HU	Hour units in BCD format
[24:22]	r	3'h0	MNT	Minute tens in BCD format
[21:18]	r	4'h0	MNU	Minute units in BCD format
[17:15]	r	3'h0	ST	Second tens in BCD format
[14:11]	r	4'h0	SU	Second units in BCD format
[10]			RSVD	
[9:0]	r	10'h0	SS	Sub-second counter
0x0C			**RTC_DR**	Mirrored RTC Date Register
[31]	r	1'h0	ERR	reserved for debug
[30:25]			RSVD	
[24]	r	1'h0	CB	Century flag
[23:20]	r	4'h0	YT	Year tens in BCD format
[19:16]	r	4'h0	YU	Year units in BCD format
[15:13]	r	3'h1	WD	Week day units 000: forbidden 001: Monday ... 111: Sunday
[12]	r	1'h0	MT	Month tens in BCD format
[11:8]	r	4'h1	MU	Month units in BCD format
[7:6]			RSVD	
[5:4]	r	2'h0	DT	Date tens in BCD format
[3:0]	r	4'h1	DU	Date units in BCD format
0x10			**MDBGR**	Memory Debug Register
[31:9]			RSVD	
[8]	rw	1'b0	PD_CACHE	reserved for debug
[7]	rw	1'b0	DS_CACHE	reserved for debug
[6]	rw	1'b0	LS_ROM	reserved for debug
[5]	rw	1'b0	LS_CACHE	reserved for debug
[4]	rw	1'b0	LS_DTCM	reserved for debug

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表 5-9: LPSYS_CFG 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[3]	rw	1'b0	LS_ITCM	reserved for debug
[2]	rw	1'b0	LS_RAM2	reserved for debug
[1]	rw	1'b0	LS_RAM1	reserved for debug
[0]	rw	1'b0	LS_RAM0	reserved for debug
0x14			**DBGR**	Debug Register
[31]	rw	1'h0	READY	reserved for debug
[30]	r	1'h0	HP2LP_NMIF	HP2LP NMI interrupt flag
[29]	rw	1'h0	HP2LP_NMIE	HP2LP NMI interrupt enable
[28]	rw	1'h0	LP2HP_NMI	set 1 to send NMI interrupt to HCPU
[27]	rw	1'b0	CLK_EN	reserved for debug
[26:24]	rw	3'b0	CLK_SEL	reserved for debug
[23:16]	rw	8'h0	BITEN_H	reserved for debug
[15:8]	rw	8'h0	BITEN_L	reserved for debug
[7:4]	rw	4'h0	SEL_H	reserved for debug
[3:0]	rw	4'h0	SEL_L	reserved for debug
0x38			**SYSCR**	System Configure Register
[31:26]	r	6'h0	SCIO	reserved for debug
[25:2]			RSVD	
[1]	rw	1'h0	DBG_SWAP	reserved for debug
[0]	rw	1'h0	WDT2_REBOOT	If set to 1, WDT2 reset will reboot the whole chip
0x3C			**ANATR**	Analog Test Register
[31:8]			RSVD	
[7:5]	rw	3'h0	DC_UR_ATEST1	reserved for debug
[4]	rw	1'h0	DC_TE_ATEST1	reserved for debug
[3:1]	rw	3'h0	DC_UR_ATEST0	reserved for debug
[0]	rw	1'h0	DC_TE_ATEST0	reserved for debug
0x40			**I2C5_PINR**	I2C5 Pin Register
[31:14]			RSVD	
[13:8]	rw	6'h3f	SDA_PIN	Connect function pin to selected IO(PB). 0 to 31 for PB00 to PB31. Other values for floating.
[7:6]			RSVD	
[5:0]	rw	6'h3f	SCL_PIN	Connect function pin to selected IO(PB). 0 to 31 for PB00 to PB31. Other values for floating.
0x44			**I2C6_PINR**	I2C6 Pin Register
[31:14]			RSVD	
[13:8]	rw	6'h3f	SDA_PIN	Connect function pin to selected IO(PB). 0 to 31 for PB00 to PB31. Other values for floating.
[7:6]			RSVD	
[5:0]	rw	6'h3f	SCL_PIN	Connect function pin to selected IO(PB). 0 to 31 for PB00 to PB31. Other values for floating.
0x48			**I2C7_PINR**	I2C7 Pin Register
[31:14]			RSVD	

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表 5-9: LPSYS_CFG 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[13:8]	rw	6'h3f	SDA_PIN	Connect function pin to selected IO(PB). 0 to 31 for PB00 to PB31. Other values for floating.
[7:6]			RSVD	
[5:0]	rw	6'h3f	SCL_PIN	Connect function pin to selected IO(PB). 0 to 31 for PB00 to PB31. Other values for floating.
0x4C			**USART4_PINR**	USART4 Pin Register
[31:30]			RSVD	
[29:24]	rw	6'h3f	CTS_PIN	Connect function pin to selected IO(PB). 0 to 31 for PB00 to PB31. Other values for floating.
[23:22]			RSVD	
[21:16]	rw	6'h3f	RTS_PIN	Connect function pin to selected IO(PB). 0 to 31 for PB00 to PB31. Other values for floating.
[15:14]			RSVD	
[13:8]	rw	6'h3f	RXD_PIN	Connect function pin to selected IO(PB). 0 to 31 for PB00 to PB31. Other values for floating.
[7:6]			RSVD	
[5:0]	rw	6'h3f	TXD_PIN	Connect function pin to selected IO(PB). 0 to 31 for PB00 to PB31. Other values for floating.
0x50			**USART5_PINR**	USART5 Pin Register
[31:30]			RSVD	
[29:24]	rw	6'h3f	CTS_PIN	Connect function pin to selected IO(PB). 0 to 31 for PB00 to PB31. Other values for floating.
[23:22]			RSVD	
[21:16]	rw	6'h3f	RTS_PIN	Connect function pin to selected IO(PB). 0 to 31 for PB00 to PB31. Other values for floating.
[15:14]			RSVD	
[13:8]	rw	6'h3f	RXD_PIN	Connect function pin to selected IO(PB). 0 to 31 for PB00 to PB31. Other values for floating.
[7:6]			RSVD	
[5:0]	rw	6'h3f	TXD_PIN	Connect function pin to selected IO(PB). 0 to 31 for PB00 to PB31. Other values for floating.
0x54			**USART6_PINR**	USART6 Pin Register
[31:30]			RSVD	
[29:24]	rw	6'h3f	CTS_PIN	Connect function pin to selected IO(PB). 0 to 31 for PB00 to PB31. Other values for floating.
[23:22]			RSVD	

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表 5-9: LPSYS_CFG 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[21:16]	rw	6'h3f	RTS_PIN	Connect function pin to selected IO(PB). 0 to 31 for PB00 to PB31. Other values for floating.
[15:14]			RSVD	
[13:8]	rw	6'h3f	RXD_PIN	Connect function pin to selected IO(PB). 0 to 31 for PB00 to PB31. Other values for floating.
[7:6]			RSVD	
[5:0]	rw	6'h3f	TXD_PIN	Connect function pin to selected IO(PB). 0 to 31 for PB00 to PB31. Other values for floating.
0x58			**GPTIM3_PINR**	GPTIM3 Pin Register
[31:30]			RSVD	
[29:24]	rw	6'h3f	CH4_PIN	Connect function pin to selected IO(PB). 0 to 31 for PB00 to PB31. Other values for floating.
[23:22]			RSVD	
[21:16]	rw	6'h3f	CH3_PIN	Connect function pin to selected IO(PB). 0 to 31 for PB00 to PB31. Other values for floating.
[15:14]			RSVD	
[13:8]	rw	6'h3f	CH2_PIN	Connect function pin to selected IO(PB). 0 to 31 for PB00 to PB31. Other values for floating.
[7:6]			RSVD	
[5:0]	rw	6'h3f	CH1_PIN	Connect function pin to selected IO(PB). 0 to 31 for PB00 to PB31. Other values for floating.
0x5C			**GPTIM4_PINR**	GPTIM4 Pin Register
[31:30]			RSVD	
[29:24]	rw	6'h3f	CH4_PIN	Connect function pin to selected IO(PB). 0 to 31 for PB00 to PB31. Other values for floating.
[23:22]			RSVD	
[21:16]	rw	6'h3f	CH3_PIN	Connect function pin to selected IO(PB). 0 to 31 for PB00 to PB31. Other values for floating.
[15:14]			RSVD	
[13:8]	rw	6'h3f	CH2_PIN	Connect function pin to selected IO(PB). 0 to 31 for PB00 to PB31. Other values for floating.
[7:6]			RSVD	
[5:0]	rw	6'h3f	CH1_PIN	Connect function pin to selected IO(PB). 0 to 31 for PB00 to PB31. Other values for floating.
0x60			**GPTIM5_PINR**	GPTIM5 Pin Register
[31:30]			RSVD	

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表 5-9: LPSYS_CFG 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[29:24]	rw	6'h3f	CH4_PIN	Connect function pin to selected IO(PB). 0 to 31 for PB00 to PB31. Other values for floating.
[23:22]			RSVD	
[21:16]	rw	6'h3f	CH3_PIN	Connect function pin to selected IO(PB). 0 to 31 for PB00 to PB31. Other values for floating.
[15:14]			RSVD	
[13:8]	rw	6'h3f	CH2_PIN	Connect function pin to selected IO(PB). 0 to 31 for PB00 to PB31. Other values for floating.
[7:6]			RSVD	
[5:0]	rw	6'h3f	CH1_PIN	Connect function pin to selected IO(PB). 0 to 31 for PB00 to PB31. Other values for floating.
0x64			**ETR_PINR**	ETR Pin Register
[31:22]			RSVD	
[21:16]	rw	6'h3f	ETR5_PIN	Connect GPTIM5_ETR to selected IO(PB). 0 to 31 for PB00 to PB31. Other values for floating.
[15:14]			RSVD	
[13:8]	rw	6'h3f	ETR4_PIN	Connect GPTIM4_ETR to selected IO(PB). 0 to 31 for PB00 to PB31. Other values for floating.
[7:6]			RSVD	
[5:0]	rw	6'h3f	ETR3_PIN	Connect GPTIM3_ETR to selected IO(PB). 0 to 31 for PB00 to PB31. Other values for floating.
0x68			**LPTIM3_PINR**	LPTIM3 Pin Register
[31:22]			RSVD	
[21:16]	rw	6'h3f	ETR_PIN	Connect function pin to selected IO(PB). 0 to 31 for PB00 to PB31. Other values for floating.
[15:14]			RSVD	
[13:8]	rw	6'h3f	OUT_PIN	Connect function pin to selected IO(PB). 0 to 31 for PB00 to PB31. Other values for floating.
[7:6]			RSVD	
[5:0]	rw	6'h3f	IN_PIN	Connect function pin to selected IO(PB). 0 to 31 for PB00 to PB31. Other values for floating.

5.22 LPSYS_GPIO 寄存器

表 5-10: LPSYS_GPIO 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00			**DIR0**	Data Input Register
[31:0]	r	32'h0	IN	GPIO[31:0] input value
0x04			**DOR0**	Data Output Register
[31:0]	rw	32'h0	OUT	GPIO[31:0] output value if output enabled
0x08			**DOSR0**	Data Output Set Register
[31:0]	w	32'h0	DOS	set 1 to pull up output of corresponding GPIO[31:0]
0x0C			**DOCR0**	Data Output Clear Register
[31:0]	w	32'h0	DOC	set 1 to pull down output of corresponding GPIO[31:0]
0x10			**DOER0**	Data Output Enable Register
[31:0]	rw	32'h0	DOE	GPIO[31:0] output enable
0x14			**DOESR0**	Data Output Enable Set Register
[31:0]	w	32'h0	DOES	set 1 to enable output of corresponding GPIO[31:0]
0x18			**DOECR0**	Data Output Enable Clear Register
[31:0]	w	32'h0	DOEC	set 1 to disable output of corresponding GPIO[31:0]
0x1C			**IER0**	Interrupt Enable Register
[31:0]	rw	32'h0	IER	GPIO[31:0] interrupt enable
0x20			**IESR0**	Interrupt Enable Set Register
[31:0]	w	32'h0	IES	set 1 to enable interrupt of corresponding GPIO[31:0]
0x24			**IECR0**	Interrupt Enable Clear Register
[31:0]	w	32'h0	IEC	set 1 to disable interrupt of corresponding GPIO[31:0]
0x28			**ITR0**	Interrupt Type Register
[31:0]	rw	32'h0	ITR	GPIO[31:0] interrupt type
0x2C			**ITSR0**	Interrupt Type Set Register
[31:0]	w	32'h0	ITS	set 1 for edge-sensitive interrupt mode of corresponding GPIO[31:0]
0x30			**ITCR0**	Interrupt Type Clear Register
[31:0]	w	32'h0	ITC	set 1 for level-sensitive interrupt mode of corresponding GPIO[31:0]
0x34			**IPHR0**	Interrupt Polarity High Register
[31:0]	rw	32'h0	IPH	rising edge in edge mode, or high level in level mode of corresponding GPIO[31:0]
0x38			**IPHSR0**	Interrupt Polarity High Set Register
[31:0]	w	32'h0	IPHS	set 1 for rising edge in edge mode, or high level in level mode of corresponding GPIO[31:0]
0x3C			**IPHCR0**	Interrupt Polarity High Clear Register
[31:0]	w	32'h0	IPHC	set 1 for disable rising edge in edge mode, or high level in level mode of corresponding GPIO[31:0]
0x40			**IPLR0**	Interrupt Polarity Low Register
[31:0]	rw	32'h0	IPL	falling edge in edge mode, or low level in level mode of corresponding GPIO[31:0]
0x44			**IPLSR0**	Interrupt Polarity Low Set Register
[31:0]	w	32'h0	IPLS	set 1 for falling edge in edge mode, or low level in level mode of corresponding GPIO[31:0]
0x48			**IPLCR0**	Interrupt Polarity Low Clear Register
[31:0]	w	32'h0	IPLC	set 1 for disable falling edge in edge mode, or low level in level mode of corresponding GPIO[31:0]
0x4C			**ISR0**	Interrupt Status Register
[31:0]	rw	32'h0	IS	Interrupt status. Write 1 will clear interrupt status of corresponding GPIO[31:0]
0x50			**IER0_EXT**	Extra Interrupt Enable Register
[31:0]	rw	32'h0	IER	GPIO[31:0] extra interrupt enable
0x54			**IESR0_EXT**	Extra Interrupt Enable Set Register
[31:0]	w	32'h0	IES	set 1 to enable extra interrupt of corresponding GPIO[31:0]

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表 5-10: LPSYS_GPIO 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
0x58			**IECR0_EXT**	Extra Interrupt Enable Clear Register
[31:0]	w	32'h0	IEC	set 1 to disable extra interrupt of corresponding GPIO[31:0]
0x5C			**ISR0_EXT**	Extra Interrupt Status Register
[31:0]	rw	32'h0	IS	Interrupt status. Write 1 will clear extra interrupt status of corresponding GPIO[31:0]
0x60			**OEMR0**	output mode Register
[31:0]	rw	32'h0	OEM	output mode of corresponding GPIO[31:0]
0x64			**OEMSR0**	output mode Set Register
[31:0]	w	32'h0	OEMS	output mode Set of corresponding GPIO[31:0]
0x68			**OEMCR0**	output mode Clear Register
[31:0]	w	32'h0	OEMC	output mode Clear of corresponding GPIO[31:0]
0x80			**DIR1**	Data Input Register
[31:5]			RSVD	
[4:0]	r	5'h0	IN	GPIO[36:32] input value
0x84			**DOR1**	Data Output Register
[31:5]			RSVD	
[4:0]	rw	5'h0	OUT	GPIO[36:32] output value if output enabled
0x88			**DOSR1**	Data Output Set Register
[31:5]			RSVD	
[4:0]	w	5'h0	DOS	set 1 to pull up output of corresponding GPIO[36:32]
0x8C			**DOCR1**	Data Output Clear Register
[31:5]			RSVD	
[4:0]	w	5'h0	DOC	set 1 to pull down output of corresponding GPIO[36:32]
0x90			**DOER1**	Data Output Enable Register
[31:5]			RSVD	
[4:0]	rw	5'h0	DOE	GPIO[36:32] output enable
0x94			**DOESR1**	Data Output Enable Set Register
[31:5]			RSVD	
[4:0]	w	5'h0	DOES	set 1 to enable output of corresponding GPIO[36:32]
0x98			**DOECR1**	Data Output Enable Clear Register
[31:5]			RSVD	
[4:0]	w	5'h0	DOEC	set 1 to disable output of corresponding GPIO[36:32]
0x9C			**IER1**	Interrupt Enable Register
[31:5]			RSVD	
[4:0]	rw	5'h0	IER	GPIO[36:32] interrupt enable
0xA0			**IESR1**	Interrupt Enable Set Register
[31:5]			RSVD	
[4:0]	w	5'h0	IES	set 1 to enable interrupt of corresponding GPIO[36:32]
0xA4			**IECR1**	Interrupt Enable Clear Register
[31:5]			RSVD	
[4:0]	w	5'h0	IEC	set 1 to disable interrupt of corresponding GPIO[36:32]
0xA8			**ITR1**	Interrupt Type Register
[31:5]			RSVD	
[4:0]	rw	5'h0	ITR	GPIO[36:32] interrupt type
0xAC			**ITSR1**	Interrupt Type Set Register
[31:5]			RSVD	
[4:0]	w	5'h0	ITS	set 1 for edge-sensitive interrupt mode of corresponding GPIO[36:32]
0xB0			**ITCR1**	Interrupt Type Clear Register

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表 5-10: LPSYS_GPIO 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:5]			RSVD	
[4:0]	w	5'h0	ITC	set 1 for level-sensitive interrupt mode of corresponding GPIO[36:32]
0xB4			**IPHR1**	Interrupt Polarity High Register
[31:5]			RSVD	
[4:0]	rw	5'h0	IPH	rising edge in edge mode, or high level in level mode of corresponding GPIO[36:32]
0xB8			**IPHSR1**	Interrupt Polarity High Set Register
[31:5]			RSVD	
[4:0]	w	5'h0	IPHS	set 1 for rising edge in edge mode, or high level in level mode of corresponding GPIO[36:32]
0xBC			**IPHCR1**	Interrupt Polarity High Clear Register
[31:5]			RSVD	
[4:0]	w	5'h0	IPHC	set 1 for disable rising edge in edge mode, or high level in level mode of corresponding GPIO[36:32]
0xC0			**IPLR1**	Interrupt Polarity Low Register
[31:5]			RSVD	
[4:0]	rw	5'h0	IPL	falling edge in edge mode, or low level in level mode of corresponding GPIO[36:32]
0xC4			**IPLSR1**	Interrupt Polarity Low Set Register
[31:5]			RSVD	
[4:0]	w	5'h0	IPLS	set 1 for falling edge in edge mode, or low level in level mode of corresponding GPIO[36:32]
0xC8			**IPLCR1**	Interrupt Polarity Low Clear Register
[31:5]			RSVD	
[4:0]	w	5'h0	IPLC	set 1 for disable falling edge in edge mode, or low level in level mode of corresponding GPIO[36:32]
0xCC			**ISR1**	Interrupt Status Register
[31:5]			RSVD	
[4:0]	rw	5'h0	IS	Interrupt status. Write 1 will clear interrupt status of corresponding GPIO[36:32]
0xD0			**IER1_EXT**	Extra Interrupt Enable Register
[31:5]			RSVD	
[4:0]	rw	5'h0	IER	GPIO[36:32] extra interrupt enable
0xD4			**IESR1_EXT**	Extra Interrupt Enable Set Register
[31:5]			RSVD	
[4:0]	w	5'h0	IES	set 1 to enable extra interrupt of corresponding GPIO[36:32]
0xD8			**IECR1_EXT**	Extra Interrupt Enable Clear Register
[31:5]			RSVD	
[4:0]	w	5'h0	IEC	set 1 to disable extra interrupt of corresponding GPIO[36:32]
0xDC			**ISR1_EXT**	extra Interrupt Status Register
[31:5]			RSVD	
[4:0]	rw	5'h0	IS	Interrupt status. Write 1 will clear interrupt status of corresponding GPIO[36:32]
0xE0			**OEMR1**	output mode Register
[31:5]			RSVD	
[4:0]	rw	5'h0	OEM	output mode of corresponding GPIO[36:32]
0xE4			**OEMSR1**	output mode Set Register
[31:5]			RSVD	
[4:0]	w	5'h0	OEMS	output mode Set of corresponding GPIO[36:32]
0xE8			**OEMCR1**	output mode Clear Register

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表 5-10: LPSYS_GPIO 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:5]			RSVD	
[4:0]	w	5'h0	OEMC	output mode Clear of corresponding GPIO[36:32]

6 DMA

6.1 DMAC

芯片共有 2 个 DMAC，其中 DMAC1 位于 HPSYS，DMAC2 位于 LPSYS。

6.1.1 简介

DMAC(Direct Memory Access Controller) 用于实现总线上两个不同地址区间内数据的搬运工作。DMAC 共有 8 个独立通道，每个通道可配置源地址区间与目标地址区间，分别映射到各存储器或外设的地址范围内，从而实现存储器-存储器，存储器-外设，外设-存储器，外设-外设之间的高效率传输，有效缓解 CPU 的工作量。DMAC 支持外设响应模式和存储器搬运模式：在外设响应模式下，DMAC 基于外设的 DMA 请求进行搬运，从而适配外设的带宽；在存储器搬运模式下，DMAC 不等待外设的 DMA 请求，尽快完成数据搬运。当多个通道同时使能时，DMAC 依照优先级由高至低的次序依次搬运；并且在较低优先级的通道搬运过程中，较高优先级的通道能够进行抢占搬运。每个通道传输过半或完成时，能够产生中断或 PTC 触发。

6.1.2 主要特性

- 单 AHB 主控总线，可访问 SRAM，PSRAM，FLASH，AHB 和 APB 外设等
- 8 个独立的可配置通道
- 每个通道的 DMA 请求可在至多 64 个外设 DMA 请求中选择 1 个，或由软件请求
- 每个通道支持 4 档优先级配置，优先级相同时依照通道编号大小判决
- 支持外设到存储器、存储器到外设、存储器到存储器以及外设到外设的数据传输
- 源地址和目标地址均独立支持单字节、双字节、四字节访问。源和目标的地址必须根据传输数据单元的大小进行对齐，并支持地址自动递增
- 单次传输单元数可配置为 0 到 65535
- 支持循环缓冲模式，单次传输完成后自动重新启动
- 每个通道支持 3 种事件标志：传输完成、过半传输或传输错误，并能独立生成中断请求及 PTC 触发
- 每个通道支持可配置块尺寸的块传输模式

6.1.3 外设请求

每个通道通过配置 CSELR1/2_CxS 在 64 个外设请求源中选择任意一个作为该通道的绑定请求源，该外设的应答信号也相应绑定到该通道上。DMAC 的外设请求表如下。

表 6-1: DMAC 外设请求表

CSELR1/2_CxS	DMAC1	DMAC2
0	mpi1	usart4_tx
1	mpi2	usart4_rx
2	mpi3	usart5_tx
3	i2c4	usart5_rx

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表 6-1: DMAC 外设请求表（续）

CSELR1/2_CxS	DMAC1	DMAC2
4	usart1_tx	usart6_tx
5	usart1_rx	usart6_rx
6	usart2_tx	btim3
7	usart2_rx	btim4
8	gptim1_update	gptim3_update
9	gptim1_trigger	gptim3_trigger
10	gptim1_cc1	gptim3_cc1
11	gptim1_cc2	gptim3_cc2
12	gptim1_cc3	gptim3_cc3
13	gptim1_cc4	gptim3_cc4
14	btim1	gptim5_update
15	btim2	gptim5_trigger
16	atim1_update	spi3_tx
17	atim1_trigger	spi3_rx
18	atim1_cc1	spi4_tx
19	atim1_cc2	spi4_rx
20	atim1_cc3	mpi5
21	atim1_cc4	i2c5
22	i2c1	i2c6
23	i2c2	i2c7
24	i2c3	gptim4_update
25	atim1_com	gptim4_trigger
26	usart3_tx	gptim4_cc1
27	usart3_rx	gptim4_cc2
28	spi1_tx	audadc_ch0
29	spi1_rx	audadc_ch1
30	spi2_tx	gpadc
31	spi2_rx	/
32	i2s1_tx	/
33	i2s1_rx	/
34	sci_tx	/
35	sci_rx	/
36	pdm1_l	/
37	pdm1_r	/
38	pdm2_l	/
39	pdm2_r	/
40	/	/
41	dac0	/
42	dac1	/
43	gptim2_update	/
44	gptim2_trigger	/
45	gptim2_cc1	/
46	audprc_tx_out_ch1	/
47	audprc_tx_out_ch0	/
48	audprc_tx_ch3	/
49	audprc_tx_ch2	/
50	audprc_tx_ch1	/
51	audprc_tx_ch0	/

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表 6-1: DMAC 外设请求表（续）

CSELR1/2_CxS	DMAC1	DMAC2
52	audprc_rx_ch1	/
53	audprc_rx_ch0	/
54	gptim2_cc2	/
55	gptim2_cc3	/
56	gptim2_cc4	/
57	sdmmc2	/
58	/	/
59	/	/
60	/	/
61	/	/
62	/	/
63	/	/

6.1.4 DMAC 功能描述

6.1.4.1 DMAC 结构图

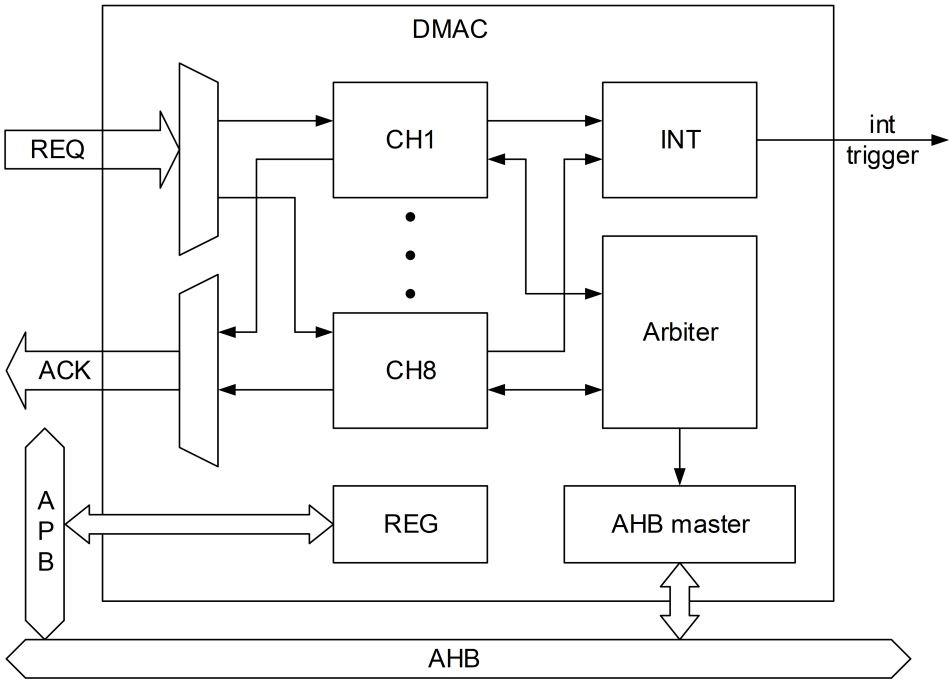

图 6-1: DMAC 结构图

6.1.4.2 传输效率

DMAC 和 CPU 及其它主控设备共享 AHB 总线。当 CPU 和 DMAC 同时访问相同的目标（存储器或外设）时，DMAC 请求可能会暂停 CPU 访问系统总线，由总线仲裁器执行循环调度，以保证 CPU 至少可以得到一半的总线带宽。同理，当其它主控设备与 DMAC 访问相同 AHB 目标时，DMAC 访问带宽也会下降。当总线没有其它访问时，DMAC 完成一笔单元传输最快需要 2 个 HCLK 周期，具体取决于访问目标的 AHB 等待周期。

6.1.4.3 传输模式

DMAC 的每个通道可独立配置为外设传输模式或存储器传输模式，由 CCRx_MEM2MEM 寄存器控制，主要区别在于是否启用外设请求/应答机制。外设传输模式通过请求/应答机制适配外设的数据带宽，仅在外设准备好了以后才发起传输，通常用于 UART 收发、I2S 音频输入输出、FLASH 烧写等场景。存储器传输模式不需等待请求信号，将以最大可能的数据带宽进行传输，通常用于 SRAM 搬运、CRC 校验等场景。

6.1.4.4 传输流程

外设传输模式下，DMAC 传输使用外设请求/应答机制，传输由外设请求发起，按照以下步骤进行传输：

1. 外设在需要传输数据时（如接收缓存满，或发送缓存空），向 DMAC 相关通道发送请求信号；
2. DMAC 按照相关通道的优先级来处理该请求，当该通道优先级为所有请求通道中最高时，启动该通道的单元传输或块传输；
3. 单元传输或块传输完成后，DMAC 向外设发送应答信号；
4. 外设获得 DMAC 的应答信号后，便会释放请求；
5. 检测到外设请求释放后，DMAC 就会释放应答信号；
6. 外设检测到应答信号释放后，如还有传输需求，可继续发送请求，再次启动 DMAC 单元传输或块传输。

存储器传输模式下，传输由软件发起，并当该通道优先级足够时，重复进行单元传输直至传输完成。

6.1.4.5 传输使能

DMAC 的 8 个通道独立使能。当 CCRx_EN 为 1 且 CNDTRx 不为 0 时，通道传输启动，在外设传输模式下开始响应外设请求，在存储器传输模式下立即开始传输。需要注意当通道使能时，即使上一笔传输已经完成，重新写入非 0 的 CNDTRx 也会立刻启动 DMAC 传输，在此之前应当确保其它参数已经配置完毕，或者在写入 CNDTRx 时保证 CCRx_EN 为 0。

6.1.4.6 传输单元

DMAC 传输的基本单位是一个传输单元，包括 3 个步骤：

1. 通过总线单次读取源地址数据，单字节/双字节/四字节可配置；
2. 将读取到的数据单次写入目标地址，单字节/双字节/四字节可配置；
3. 更新计数，根据计数结果停止传输，或计算下一次传输的地址。

6.1.4.7 传输数量

DMAC 每个通道传输的数量由 CNDTRx 控制，以传输单元计数，支持范围 0~65535。例如配置为四字节传输，则通道单次传输最大数据量为 65535×4=262140 字节。配置 CNDTRx 并启动单元传输 (CCRx_EN=1) 后，每完成一个传输单元，CNDTRx 寄存器值减 1。非循环模式下 (CCRx_CIRC=0)，CNDTRx 减到 0 就会停止传输。循环模式下 (CCRx_CIRC=1)，CNDTRx 减到 0 后会立即重新加载软件配置的初始值，并继续传输。

6.1.4.8 循环模式

循环模式下，传输不会自动停止。在循环模式下，最后一次数据传输完成后，CNDTRx 寄存器将自动重新加载初始编程值。当前的内部地址寄存器重新加载 CPARx 和 CM0ARx 寄存器中的基址值。循环模式下通过判断过半传输与传输完成标志，能够实现乒乓缓存的功能。

6.1.4.9 传输方向

DMAC 的传输方向由 CCRx_DIR 决定。

表 6-2: DMAC 传输方向

	源起始地址 (读)	目标起始地址 (写)
DIR=0	CPARx	CM0ARx
DIR=1	CM0ARx	CPARx

6.1.4.10 传输位宽

DMAC 传输时，对总线源地址和目标地址的访问可独立通过 CCRx_MSIZE 和 CCRx_PSIZE 配置为单字节/双字节/四字节类型。DMAC 不提供数据打包和拆分的功能，因此当源地址和目标地址访问数据位宽不一致时，数据会有截取或补偿，基于下表示例

表 6-3: DMAC 传输位宽

Source Size	Destination Size	Source Data	Destination Data
byte	byte	0xB0 @0x0 0xB1 @0x1 0xB2 @0x2 0xB3 @0x3	0xB0 @0x0 0xB1 @0x1 0xB2 @0x2 0xB3 @0x3
byte	half-word(16bit)	0xB0 @0x0 0xB1 @0x1 0xB2 @0x2 0xB3 @0x3	0x00B0 @0x0 0x00B1 @0x2 0x00B2 @0x4 0x00B3 @0x6
byte	word(32bit)	0xB0 @0x0 0xB1 @0x1 0xB2 @0x2 0xB3 @0x3	0x000000B0 @0x0 0x000000B1 @0x4 0x000000B2 @0x8 0x000000B3 @0xC
half-word	byte	0xB1B0 @0x0 0xB3B2 @0x2 0xB4B4 @0x4 0xB7B6 @0x6	0xB0 @0x0 0xB2 @0x1 0xB4 @0x2 0xB6 @0x3
half-word	half-word	0xB1B0 @0x0 0xB3B2 @0x2 0xB4B4 @0x4 0xB7B6 @0x6	0xB1B0 @0x0 0xB3B2 @0x2 0xB4B4 @0x4 0xB7B6 @0x6
half-word	word	0xB1B0 @0x0 0xB3B2 @0x2 0xB4B4 @0x4 0xB7B6 @0x6	0x0000B1B0 @0x0 0x0000B3B2 @0x4 0x0000B5B4 @0x8 0x0000B7B6 @0xC
word	byte	0xB3B2B1B0 @0x0 0xB7B6B5B4 @0x4 0xBBBAB9B8 @0x8 0xBFBEBDBC @0xC	0xB0 @0x0 0xB4 @0x1 0xB8 @0x2 0xBC @0x3
word	half-word	0xB3B2B1B0 @0x0 0xB7B6B5B4 @0x4 0xBBBAB9B8 @0x8 0xBFBEBDBC @0xC	0xB1B0 @0x0 0xB5B4 @0x2 0xB9B8 @0x4 0xBDBC @0x6

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表 6-3: DMAC 传输位宽（续）

Source Size	Destination Size	Source Data	Destination Data
word	word	0xB3B2B1B0 @0x0	0xB3B2B1B0 @0x0
		0xB7B6B5B4 @0x4	0xB7B6B5B4 @0x4
		0xBBBAB9B8 @0x8	0xBBBAB9B8 @0x8
		0xBFBEBDBC @0xC	0xBFBEBDBC @0xC

6.1.4.11 传输地址

传输的起始源地址和目标地址由 CPARx，CM0ARx 以及 CCRx_DIR 决定。如果使能了递增模式（CCRx_MINC 和 CCRx_PINC 独立配置），每完成一笔单元传输，则下次传输的地址是前一次传输的地址加上 1、2 或 4（与传输的位宽一致）。

地址配置时必须注意，DMAC 传输过程中地址自增不能越过 1M 字节的边界。例如当传输地址从 0x600FFFFC 增加到 0x60100000 时，传输会出现错误。因此如果要传输跨越 1M 字节边界的数据，应当分成前后两笔进行。

在传输过程中，这些寄存器将保持初始编程的值。软件无法获得当前正在传输的地址。通常外设 FIFO 的传输地址配置为不递增，而存储器的传输地址配置为递增。

6.1.4.12 通道仲裁

DMAC 仲裁器管理不同通道间的优先级。当仲裁器为某个有效通道授予优先权后（硬件请求或软件触发），会发起该通道的单元传输或块传输。随后仲裁器会再次对有效通道进行仲裁，并选择优先级最高的通道。

仲裁器基于如下准则判断优先级：

1. 外设传输模式的通道优先于存储器传输模式的通道
2. 同为外设传输模式或存储器传输模式的，通道 CCRx_PL 低的优先级高
3. 传输模式与 CCRx_PL 均相同的，通道编号小的优先级高 (如通道 1 优先于通道 2)

在某一通道传输过程中，如果有另一更高优先级的通道发出了传输请求，则在当前通道的单元传输或块传输完成后，仲裁器会把传输切换到更高优先级的通道上。

6.1.4.13 块传输

块传输仅在外设传输模式下生效。CBSRx 定义了对于每一笔外设请求，DMAC 要连续完成多少次单元传输。例如 CBSRx 设为 4 时，每当外设发起一笔请求，DMAC 将完成连续 4 次单元传输，之后再给出应答信号，期间 CNDTRx 也将连续减 4。如果剩余待传输的 CNDTRx 小于 CBSRx，则仅传输剩余的 CNDTRx 次单元传输。

6.1.4.14 通知机制

DMAC 每个通道可独立产生中断和 PTC 触发信号，并可单独配置每种中断的使能。通道传输完成至少一半时，产生 HTIFx 中断和触发。通道传输全部完成后，产生 TCIFx 中断和触发。通道传输发生总线访问错误时，产生 TEIFx 中断和触发。以上三种中断任一种发生时，产生 GIFx 中断。通道中断可单独清除，或通过 CGIFx 一并清除。

6.1.4.15 通道配置流程

配置 DMAC 通道时需按照以下步骤操作：

1. 在 CPARx 寄存器中设置外设寄存器地址。
   在外设请求发生后，或在存储器模式下使能通道后，会将数据从该地址移至存储器或从存储器移至该地址。
2. 设置 CM0ARx 寄存器中的存储器地址。
   在外设请求发生后，或在存储器模式下使能通道后，会将数据写入存储器或从存储器读取数据。
3. 确保 CCRx_EN 为 0 时，将待传输的单元数写入 CNDTRx 寄存器。
   每次数据传输后，该值都会递减。
4. 在 CCRx 寄存器中配置下列参数：
   - 通道优先级
   - 数据传输方向
   - 循环模式
   - 外设和存储器递增模式
   - 外设和存储器数据大小
   - 传输完成一半和/或全部完成以及/或者出现传输错误时的中断使能
5. 将 CCRx_EN 置 1 以激活通道。
   通道在使能后可处理来自此通道所连接外设的请求，或者启动存储器到存储器传输。

6.1.4.16 传输完成处理

在非循环模式下，DMAC 某通道传输完成后，CNDTRx 自动归零，软件需将该通道的 CCRx_EN 写 0 以避免下次配置时误触发。如果有中断标志出现，软件应当在进行相应处理后清除中断标志。

循环模式下 DMAC 不会自动停止传输，当软件想要停止传输时，应将该通道的 CCRx_EN 写 0，并清除中断标志。

6.1.5 DMAC 寄存器

表 6-4: DMAC 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00			**ISR**	
[31]	r	1'h0	TEIF8	channel transfer error flag
[30]	r	1'h0	HTIF8	channel half transfer flag
[29]	r	1'h0	TCIF8	channel transfer complete flag
[28]	r	1'h0	GIF8	channel global interrupt flag
[27]	r	1'h0	TEIF7	channel transfer error flag
[26]	r	1'h0	HTIF7	channel half transfer flag
[25]	r	1'h0	TCIF7	channel transfer complete flag
[24]	r	1'h0	GIF7	channel global interrupt flag
[23]	r	1'h0	TEIF6	channel transfer error flag
[22]	r	1'h0	HTIF6	channel half transfer flag
[21]	r	1'h0	TCIF6	channel transfer complete flag
[20]	r	1'h0	GIF6	channel global interrupt flag
[19]	r	1'h0	TEIF5	channel transfer error flag
[18]	r	1'h0	HTIF5	channel half transfer flag
[17]	r	1'h0	TCIF5	channel transfer complete flag
[16]	r	1'h0	GIF5	channel global interrupt flag
[15]	r	1'h0	TEIF4	channel transfer error flag

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表 6-4: DMAC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[14]	r	1'h0	HTIF4	channel half transfer flag
[13]	r	1'h0	TCIF4	channel transfer complete flag
[12]	r	1'h0	GIF4	channel global interrupt flag
[11]	r	1'h0	TEIF3	channel transfer error flag
[10]	r	1'h0	HTIF3	channel half transfer flag
[9]	r	1'h0	TCIF3	channel transfer complete flag
[8]	r	1'h0	GIF3	channel global interrupt flag
[7]	r	1'h0	TEIF2	channel transfer error flag
[6]	r	1'h0	HTIF2	channel half transfer flag
[5]	r	1'h0	TCIF2	channel transfer complete flag
[4]	r	1'h0	GIF2	channel global interrupt flag
[3]	r	1'h0	TEIF1	channel transfer error flag. Set when bus error detected. Cleared when write 1 to CTEIF or CGIF.
[2]	r	1'h0	HTIF1	channel half transfer flag. Set when half NDT are transferred. Cleared when write 1 to CHTIF or CGIF.
[1]	r	1'h0	TCIF1	channel transfer complete flag. Set when all NDT are transferred. Cleared when write 1 to CTCIF or CGIF.
[0]	r	1'h0	GIF1	channel global interrupt flag. Set when any of TEIF/HTIF/TCIF asserted. Cleared when TEIF/HTIF/TCIF all cleared.
0x04			**IFCR**	
[31]	w	1'h0	CTEIF8	CTEIF, transfer error flag clear
[30]	w	1'h0	CHTIF8	CHTIF, half transfer flag clear
[29]	w	1'h0	CTCIF8	CTCIF, transfer complete flag clear
[28]	w	1'h0	CGIF8	CGIF, global interrupt flag clear
[27]	w	1'h0	CTEIF7	CTEIF, transfer error flag clear
[26]	w	1'h0	CHTIF7	CHTIF, half transfer flag clear
[25]	w	1'h0	CTCIF7	CTCIF, transfer complete flag clear
[24]	w	1'h0	CGIF7	CGIF, global interrupt flag clear
[23]	w	1'h0	CTEIF6	CTEIF, transfer error flag clear
[22]	w	1'h0	CHTIF6	CHTIF, half transfer flag clear
[21]	w	1'h0	CTCIF6	CTCIF, transfer complete flag clear
[20]	w	1'h0	CGIF6	CGIF, global interrupt flag clear
[19]	w	1'h0	CTEIF5	CTEIF, transfer error flag clear
[18]	w	1'h0	CHTIF5	CHTIF, half transfer flag clear
[17]	w	1'h0	CTCIF5	CTCIF, transfer complete flag clear
[16]	w	1'h0	CGIF5	CGIF, global interrupt flag clear
[15]	w	1'h0	CTEIF4	CTEIF, transfer error flag clear
[14]	w	1'h0	CHTIF4	CHTIF, half transfer flag clear
[13]	w	1'h0	CTCIF4	CTCIF, transfer complete flag clear
[12]	w	1'h0	CGIF4	CGIF, global interrupt flag clear
[11]	w	1'h0	CTEIF3	CTEIF, transfer error flag clear
[10]	w	1'h0	CHTIF3	CHTIF, half transfer flag clear
[9]	w	1'h0	CTCIF3	CTCIF, transfer complete flag clear
[8]	w	1'h0	CGIF3	CGIF, global interrupt flag clear
[7]	w	1'h0	CTEIF2	CTEIF, transfer error flag clear
[6]	w	1'h0	CHTIF2	CHTIF, half transfer flag clear
[5]	w	1'h0	CTCIF2	CTCIF, transfer complete flag clear
[4]	w	1'h0	CGIF2	CGIF, global interrupt flag clear

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表 6-4: DMAC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[3]	w	1'h0	CTEIF1	CTEIF, transfer error flag clear. Write 1 to clear TEIF.
[2]	w	1'h0	CHTIF1	CHTIF, half transfer flag clear. Write 1 to clear HTIF.
[1]	w	1'h0	CTCIF1	CTCIF, transfer complete flag clear. Write 1 to clear TCIF.
[0]	w	1'h0	CGIF1	CGIF, global interrupt flag clear. Write 1 to clear all TEIF/HTIF/TCIF.
0x08			**CCR1**	
[31:15]			RSVD	
[14]	rw	1'h0	MEM2MEM	memory-to-memory mode 0: disabled 1: enabled
[13:12]	rw	2'h0	PL	priority level 00: low 01: medium 10: high 11: very high
[11:10]	rw	2'h0	MSIZE	memory size Defines the data size of each DMA transfer to the identified memory. In memory-to-memory mode, this field identifies the memory source if DIR = 1 and the memory destination if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral source if DIR = 1 and the peripheral destination if DIR = 0. 00: 8 bits 01: 16 bits 10: 32 bits 11: reserved
[9:8]	rw	2'h0	PSIZE	peripheral size Defines the data size of each DMA transfer to the identified peripheral. In memory-to-memory mode, this field identifies the memory destination if DIR = 1 and the memory source if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral destination if DIR = 1 and the peripheral source if DIR = 0. 00: 8 bits 01: 16 bits 10: 32 bits 11: reserved
[7]	rw	1'h0	MINC	memory increment mode Defines the increment mode for each DMA transfer to the identified memory. In memory-to-memory mode, this field identifies the memory source if DIR = 1 and the memory destination if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral source if DIR = 1 and the peripheral destination if DIR = 0. 0: disabled 1: enabled

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表 6-4: DMAC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[6]	rw	1'h0	PINC	peripheral increment mode Defines the increment mode for each DMA transfer to the identified peripheral. n memory-to-memory mode, this field identifies the memory destination if DIR = 1 and the memory source if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral destination if DIR = 1 and the peripheral source if DIR = 0. 0: disabled 1: enabled
[5]	rw	1'h0	CIRC	circular mode 0: disabled 1: enabled
[4]	rw	1'h0	DIR	data transfer direction This bit must be set only in memory-to-peripheral and peripheral-to-memory modes. 0: read from peripheral Source attributes are defined by PSIZE and PINC, plus the CPARx register. This is still valid in a memory-to-memory mode. Destination attributes are defined by MSIZE and MINC, plus the CM0ARx register. This is still valid in a peripheral-to-peripheral mode. 1: read from memory Destination attributes are defined by PSIZE and PINC, plus the CPARx register. This is still valid in a memory-to-memory mode. Source attributes are defined by MSIZE and MINC, plus the CM0ARx register. This is still valid in a peripheral-to-peripheral mode.
[3]	rw	1'h0	TEIE	transfer error interrupt enable 0: disabled 1: enabled
[2]	rw	1'h0	HTIE	half transfer interrupt enable 0: disabled 1: enabled
[1]	rw	1'h0	TCIE	transfer complete interrupt enable 0: disabled 1: enabled
[0]	rw	1'h0	EN	channel enable When a channel transfer error occurs, this bit is cleared by hardware. It can not be set again by software (channel x re-activated) until the TEIFx bit of the ISR register is cleared (by setting the CTEIFx bit of the IFCR register). 0: disabled 1: enabled
0x0C			**CNDTR1**	
[31:16]			RSVD	

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表 6-4: DMAC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[15:0]	rw	16'h0	NDT	number of data to transfer (0 to 2^{16} - 1) This field is updated by hardware when the channel is enabled: It is decremented after each single DMA 'read followed by write' transfer, indicating the remaining amount of data items to transfer. It is kept at zero when the programmed amount of data to transfer is reached, if the channel is not in circular mode (CIRC = 0 in the CCRx register). It is reloaded automatically by the previously programmed value, when the transfer is complete, if the channel is in circular mode (CIRC = 1). If this field is zero, no transfer can be served whatever the channel status (enabled or not).
0x10			**CPAR1**	
[31:0]	rw	32'h0	PA	peripheral address It contains the base address of the peripheral data register from/to which the data will be read/written. In memory-to-memory mode, this register identifies the memory destination address if DIR = 1 and the memory source address if DIR = 0. In peripheral-to-peripheral mode, this register identifies the peripheral destination address DIR = 1 and the peripheral source address if DIR = 0.
0x14			**CM0AR1**	
[31:0]	rw	32'h0	MA	memory address It contains the base address of the memory from/to which the data will be read/written. In memory-to-memory mode, this register identifies the memory source address if DIR = 1 and the memory destination address if DIR = 0. In peripheral-to-peripheral mode, this register identifies the peripheral source address DIR = 1 and the peripheral destination address if DIR = 0.
0x18			**CBSR1**	
[31:8]			RSVD	
[7:0]	rw	8'h0	BS	burst size in non-m2m mode When BS>1, DMA will transfer for BS times for each request if left NDT is larger than BS, or else transfer for left NDT times. When BS=0 or 1, DMA will always do single transfer for each request. In memory-to-memory mode, BS is ignored.
0x1C			**CCR2**	
[31:15]			RSVD	
[14]	rw	1'h0	MEM2MEM	memory-to-memory mode 0: disabled 1: enabled
[13:12]	rw	2'h0	PL	priority level 00: low 01: medium 10: high 11: very high

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表 6-4: DMAC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[11:10]	rw	2'h0	MSIZE	memory size Defines the data size of each DMA transfer to the identified memory. In memory-to-memory mode, this field identifies the memory source if DIR = 1 and the memory destination if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral source if DIR = 1 and the peripheral destination if DIR = 0. 00: 8 bits 01: 16 bits 10: 32 bits 11: reserved
[9:8]	rw	2'h0	PSIZE	peripheral size Defines the data size of each DMA transfer to the identified peripheral. In memory-to-memory mode, this field identifies the memory destination if DIR = 1 and the memory source if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral destination if DIR = 1 and the peripheral source if DIR = 0. 00: 8 bits 01: 16 bits 10: 32 bits 11: reserved
[7]	rw	1'h0	MINC	memory increment mode Defines the increment mode for each DMA transfer to the identified memory. In memory-to-memory mode, this field identifies the memory source if DIR = 1 and the memory destination if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral source if DIR = 1 and the peripheral destination if DIR = 0. 0: disabled 1: enabled
[6]	rw	1'h0	PINC	peripheral increment mode Defines the increment mode for each DMA transfer to the identified peripheral. n memory-to-memory mode, this field identifies the memory destination if DIR = 1 and the memory source if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral destination if DIR = 1 and the peripheral source if DIR = 0. 0: disabled 1: enabled
[5]	rw	1'h0	CIRC	circular mode 0: disabled 1: enabled

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表 6-4: DMAC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[4]	rw	1'h0	DIR	data transfer direction This bit must be set only in memory-to-peripheral and peripheral-to-memory modes. 0: read from peripheral Source attributes are defined by PSIZE and PINC, plus the CPARx register. This is still valid in a memory-to-memory mode. Destination attributes are defined by MSIZE and MINC, plus the CM0ARx register. This is still valid in a peripheral-to-peripheral mode. 1: read from memory Destination attributes are defined by PSIZE and PINC, plus the CPARx register. This is still valid in a memory-to-memory mode. Source attributes are defined by MSIZE and MINC, plus the CM0ARx register. This is still valid in a peripheral-to-peripheral mode.
[3]	rw	1'h0	TEIE	transfer error interrupt enable 0: disabled 1: enabled
[2]	rw	1'h0	HTIE	half transfer interrupt enable 0: disabled 1: enabled
[1]	rw	1'h0	TCIE	transfer complete interrupt enable 0: disabled 1: enabled
[0]	rw	1'h0	EN	channel enable When a channel transfer error occurs, this bit is cleared by hardware. It can not be set again by software (channel x re-activated) until the TEIFx bit of the ISR register is cleared (by setting the CTEIFx bit of the IFCR register). 0: disabled 1: enabled
0x20			**CNDTR2**	
[31:16]			RSVD	
[15:0]	rw	16'h0	NDT	number of data to transfer (0 to 2^{16} - 1) This field is updated by hardware when the channel is enabled: It is decremented after each single DMA 'read followed by write' transfer, indicating the remaining amount of data items to transfer. It is kept at zero when the programmed amount of data to transfer is reached, if the channel is not in circular mode (CIRC = 0 in the CCRx register). It is reloaded automatically by the previously programmed value, when the transfer is complete, if the channel is in circular mode (CIRC = 1). If this field is zero, no transfer can be served whatever the channel status (enabled or not).
0x24			**CPAR2**	
[31:0]	rw	32'h0	PA	peripheral address It contains the base address of the peripheral data register from/to which the data will be read/written. In memory-to-memory mode, this register identifies the memory destination address if DIR = 1 and the memory source address if DIR = 0. In peripheral-to-peripheral mode, this register identifies the peripheral destination address DIR = 1 and the peripheral source address if DIR = 0.
0x28			**CM0AR2**	

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表 6-4: DMAC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:0]	rw	32'h0	MA	peripheral address It contains the base address of the memory from/to which the data will be read/written. In memory-to-memory mode, this register identifies the memory source address if DIR = 1 and the memory destination address if DIR = 0. In peripheral-to-peripheral mode, this register identifies the peripheral source address DIR = 1 and the peripheral destination address if DIR = 0.
0x2C			**CBSR2**	
[31:8]			RSVD	
[7:0]	rw	8'h0	BS	burst size in non-m2m mode When BS>1, DMA will transfer for BS times for each request if left NDT is larger than BS, or else transfer for left NDT times. When BS=0 or 1, DMA will always do single transfer for each request. In memory-to-memory mode, BS is ignored.
0x30			**CCR3**	
[31:15]			RSVD	
[14]	rw	1'h0	MEM2MEM	memory-to-memory mode 0: disabled 1: enabled
[13:12]	rw	2'h0	PL	priority level 00: low 01: medium 10: high 11: very high
[11:10]	rw	2'h0	MSIZE	memory size Defines the data size of each DMA transfer to the identified memory. In memory-to-memory mode, this field identifies the memory source if DIR = 1 and the memory destination if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral source if DIR = 1 and the peripheral destination if DIR = 0. 00: 8 bits 01: 16 bits 10: 32 bits 11: reserved
[9:8]	rw	2'h0	PSIZE	peripheral size Defines the data size of each DMA transfer to the identified peripheral. In memory-to-memory mode, this field identifies the memory destination if DIR = 1 and the memory source if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral destination if DIR = 1 and the peripheral source if DIR = 0. 00: 8 bits 01: 16 bits 10: 32 bits 11: reserved

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表 6-4: DMAC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[7]	rw	1'h0	MINC	memory increment mode Defines the increment mode for each DMA transfer to the identified memory. In memory-to-memory mode, this field identifies the memory source if DIR = 1 and the memory destination if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral source if DIR = 1 and the peripheral destination if DIR = 0. 0: disabled 1: enabled
[6]	rw	1'h0	PINC	peripheral increment mode Defines the increment mode for each DMA transfer to the identified peripheral. n memory-to-memory mode, this field identifies the memory destination if DIR = 1 and the memory source if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral destination if DIR = 1 and the peripheral source if DIR = 0. 0: disabled 1: enabled
[5]	rw	1'h0	CIRC	circular mode 0: disabled 1: enabled
[4]	rw	1'h0	DIR	data transfer direction This bit must be set only in memory-to-peripheral and peripheral-to-memory modes. 0: read from peripheral Source attributes are defined by PSIZE and PINC, plus the CPARx register. This is still valid in a memory-to-memory mode. Destination attributes are defined by MSIZE and MINC, plus the CM0ARx register. This is still valid in a peripheral-to-peripheral mode. 1: read from memory Destination attributes are defined by PSIZE and PINC, plus the CPARx register. This is still valid in a memory-to-memory mode. Source attributes are defined by MSIZE and MINC, plus the CM0ARx register. This is still valid in a peripheral-to-peripheral mode.
[3]	rw	1'h0	TEIE	transfer error interrupt enable 0: disabled 1: enabled
[2]	rw	1'h0	HTIE	half transfer interrupt enable 0: disabled 1: enabled
[1]	rw	1'h0	TCIE	transfer complete interrupt enable 0: disabled 1: enabled
[0]	rw	1'h0	EN	channel enable When a channel transfer error occurs, this bit is cleared by hardware. It can not be set again by software (channel x re-activated) until the TEIFx bit of the ISR register is cleared (by setting the CTEIFx bit of the IFCR register). 0: disabled 1: enabled

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表 6-4: DMAC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
0x34			**CNDTR3**	
[31:16]			RSVD	
[15:0]	rw	16'h0	NDT	number of data to transfer (0 to 2^{16} - 1) This field is updated by hardware when the channel is enabled: It is decremented after each single DMA 'read followed by write' transfer, indicating the remaining amount of data items to transfer. It is kept at zero when the programmed amount of data to transfer is reached, if the channel is not in circular mode (CIRC = 0 in the CCRx register). It is reloaded automatically by the previously programmed value, when the transfer is complete, if the channel is in circular mode (CIRC = 1). If this field is zero, no transfer can be served whatever the channel status (enabled or not).
0x38			**CPAR3**	
[31:0]	rw	32'h0	PA	peripheral address It contains the base address of the peripheral data register from/to which the data will be read/written. In memory-to-memory mode, this register identifies the memory destination address if DIR = 1 and the memory source address if DIR = 0. In peripheral-to-peripheral mode, this register identifies the peripheral destination address DIR = 1 and the peripheral source address if DIR = 0.
0x3C			**CM0AR3**	
[31:0]	rw	32'h0	MA	peripheral address It contains the base address of the memory from/to which the data will be read/written. In memory-to-memory mode, this register identifies the memory source address if DIR = 1 and the memory destination address if DIR = 0. In peripheral-to-peripheral mode, this register identifies the peripheral source address DIR = 1 and the peripheral destination address if DIR = 0.
0x40			**CBSR3**	
[31:8]			RSVD	
[7:0]	rw	8'h0	BS	burst size in non-m2m mode When BS>1, DMA will transfer for BS times for each request if left NDT is larger than BS, or else transfer for left NDT times. When BS=0 or 1, DMA will always do single transfer for each request. In memory-to-memory mode, BS is ignored.
0x44			**CCR4**	
[31:15]			RSVD	
[14]	rw	1'h0	MEM2MEM	memory-to-memory mode 0: disabled 1: enabled
[13:12]	rw	2'h0	PL	priority level 00: low 01: medium 10: high 11: very high

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表 6-4: DMAC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[11:10]	rw	2'h0	MSIZE	memory size Defines the data size of each DMA transfer to the identified memory. In memory-to-memory mode, this field identifies the memory source if DIR = 1 and the memory destination if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral source if DIR = 1 and the peripheral destination if DIR = 0. 00: 8 bits 01: 16 bits 10: 32 bits 11: reserved
[9:8]	rw	2'h0	PSIZE	peripheral size Defines the data size of each DMA transfer to the identified peripheral. In memory-to-memory mode, this field identifies the memory destination if DIR = 1 and the memory source if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral destination if DIR = 1 and the peripheral source if DIR = 0. 00: 8 bits 01: 16 bits 10: 32 bits 11: reserved
[7]	rw	1'h0	MINC	memory increment mode Defines the increment mode for each DMA transfer to the identified memory. In memory-to-memory mode, this field identifies the memory source if DIR = 1 and the memory destination if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral source if DIR = 1 and the peripheral destination if DIR = 0. 0: disabled 1: enabled
[6]	rw	1'h0	PINC	peripheral increment mode Defines the increment mode for each DMA transfer to the identified peripheral. n memory-to-memory mode, this field identifies the memory destination if DIR = 1 and the memory source if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral destination if DIR = 1 and the peripheral source if DIR = 0. 0: disabled 1: enabled
[5]	rw	1'h0	CIRC	circular mode 0: disabled 1: enabled

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表 6-4: DMAC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[4]	rw	1'h0	DIR	data transfer direction This bit must be set only in memory-to-peripheral and peripheral-to-memory modes. 0: read from peripheral Source attributes are defined by PSIZE and PINC, plus the CPARx register. This is still valid in a memory-to-memory mode. Destination attributes are defined by MSIZE and MINC, plus the CM0ARx register. This is still valid in a peripheral-to-peripheral mode. 1: read from memory Destination attributes are defined by PSIZE and PINC, plus the CPARx register. This is still valid in a memory-to-memory mode. Source attributes are defined by MSIZE and MINC, plus the CM0ARx register. This is still valid in a peripheral-to-peripheral mode.
[3]	rw	1'h0	TEIE	transfer error interrupt enable 0: disabled 1: enabled
[2]	rw	1'h0	HTIE	half transfer interrupt enable 0: disabled 1: enabled
[1]	rw	1'h0	TCIE	transfer complete interrupt enable 0: disabled 1: enabled
[0]	rw	1'h0	EN	channel enable When a channel transfer error occurs, this bit is cleared by hardware. It can not be set again by software (channel x re-activated) until the TEIFx bit of the ISR register is cleared (by setting the CTEIFx bit of the IFCR register). 0: disabled 1: enabled
0x48			**CNDTR4**	
[31:16]			RSVD	
[15:0]	rw	16'h0	NDT	number of data to transfer (0 to 2^{16} - 1) This field is updated by hardware when the channel is enabled: It is decremented after each single DMA 'read followed by write' transfer, indicating the remaining amount of data items to transfer. It is kept at zero when the programmed amount of data to transfer is reached, if the channel is not in circular mode (CIRC = 0 in the CCRx register). It is reloaded automatically by the previously programmed value, when the transfer is complete, if the channel is in circular mode (CIRC = 1). If this field is zero, no transfer can be served whatever the channel status (enabled or not).
0x4C			**CPAR4**	
[31:0]	rw	32'h0	PA	peripheral address It contains the base address of the peripheral data register from/to which the data will be read/written. In memory-to-memory mode, this register identifies the memory destination address if DIR = 1 and the memory source address if DIR = 0. In peripheral-to-peripheral mode, this register identifies the peripheral destination address DIR = 1 and the peripheral source address if DIR = 0.
0x50			**CM0AR4**	

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表 6-4: DMAC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:0]	rw	32'h0	MA	peripheral address It contains the base address of the memory from/to which the data will be read/written. In memory-to-memory mode, this register identifies the memory source address if DIR = 1 and the memory destination address if DIR = 0. In peripheral-to-peripheral mode, this register identifies the peripheral source address DIR = 1 and the peripheral destination address if DIR = 0.
0x54			**CBSR4**	
[31:8]			RSVD	
[7:0]	rw	8'h0	BS	burst size in non-m2m mode When BS>1, DMA will transfer for BS times for each request if left NDT is larger than BS, or else transfer for left NDT times. When BS=0 or 1, DMA will always do single transfer for each request. In memory-to-memory mode, BS is ignored.
0x58			**CCR5**	
[31:15]			RSVD	
[14]	rw	1'h0	MEM2MEM	memory-to-memory mode 0: disabled 1: enabled
[13:12]	rw	2'h0	PL	priority level 00: low 01: medium 10: high 11: very high
[11:10]	rw	2'h0	MSIZE	memory size Defines the data size of each DMA transfer to the identified memory. In memory-to-memory mode, this field identifies the memory source if DIR = 1 and the memory destination if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral source if DIR = 1 and the peripheral destination if DIR = 0. 00: 8 bits 01: 16 bits 10: 32 bits 11: reserved
[9:8]	rw	2'h0	PSIZE	peripheral size Defines the data size of each DMA transfer to the identified peripheral. In memory-to-memory mode, this field identifies the memory destination if DIR = 1 and the memory source if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral destination if DIR = 1 and the peripheral source if DIR = 0. 00: 8 bits 01: 16 bits 10: 32 bits 11: reserved

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表 6-4: DMAC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[7]	rw	1'h0	MINC	memory increment mode Defines the increment mode for each DMA transfer to the identified memory. In memory-to-memory mode, this field identifies the memory source if DIR = 1 and the memory destination if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral source if DIR = 1 and the peripheral destination if DIR = 0. 0: disabled 1: enabled
[6]	rw	1'h0	PINC	peripheral increment mode Defines the increment mode for each DMA transfer to the identified peripheral. n memory-to-memory mode, this field identifies the memory destination if DIR = 1 and the memory source if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral destination if DIR = 1 and the peripheral source if DIR = 0. 0: disabled 1: enabled
[5]	rw	1'h0	CIRC	circular mode 0: disabled 1: enabled
[4]	rw	1'h0	DIR	data transfer direction This bit must be set only in memory-to-peripheral and peripheral-to-memory modes. 0: read from peripheral Source attributes are defined by PSIZE and PINC, plus the CPARx register. This is still valid in a memory-to-memory mode. Destination attributes are defined by MSIZE and MINC, plus the CM0ARx register. This is still valid in a peripheral-to-peripheral mode. 1: read from memory Destination attributes are defined by PSIZE and PINC, plus the CPARx register. This is still valid in a memory-to-memory mode. Source attributes are defined by MSIZE and MINC, plus the CM0ARx register. This is still valid in a peripheral-to-peripheral mode.
[3]	rw	1'h0	TEIE	transfer error interrupt enable 0: disabled 1: enabled
[2]	rw	1'h0	HTIE	half transfer interrupt enable 0: disabled 1: enabled
[1]	rw	1'h0	TCIE	transfer complete interrupt enable 0: disabled 1: enabled
[0]	rw	1'h0	EN	channel enable When a channel transfer error occurs, this bit is cleared by hardware. It can not be set again by software (channel x re-activated) until the TEIFx bit of the ISR register is cleared (by setting the CTEIFx bit of the IFCR register). 0: disabled 1: enabled

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表 6-4: DMAC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
0x5C			**CNDTR5**	
[31:16]			RSVD	
[15:0]	rw	16'h0	NDT	number of data to transfer (0 to 2^{16} - 1) This field is updated by hardware when the channel is enabled: It is decremented after each single DMA 'read followed by write' transfer, indicating the remaining amount of data items to transfer. It is kept at zero when the programmed amount of data to transfer is reached, if the channel is not in circular mode (CIRC = 0 in the CCRx register). It is reloaded automatically by the previously programmed value, when the transfer is complete, if the channel is in circular mode (CIRC = 1). If this field is zero, no transfer can be served whatever the channel status (enabled or not).
0x60			**CPAR5**	
[31:0]	rw	32'h0	PA	peripheral address It contains the base address of the peripheral data register from/to which the data will be read/written. In memory-to-memory mode, this register identifies the memory destination address if DIR = 1 and the memory source address if DIR = 0. In peripheral-to-peripheral mode, this register identifies the peripheral destination address DIR = 1 and the peripheral source address if DIR = 0.
0x64			**CM0AR5**	
[31:0]	rw	32'h0	MA	peripheral address It contains the base address of the memory from/to which the data will be read/written. In memory-to-memory mode, this register identifies the memory source address if DIR = 1 and the memory destination address if DIR = 0. In peripheral-to-peripheral mode, this register identifies the peripheral source address DIR = 1 and the peripheral destination address if DIR = 0.
0x68			**CBSR5**	
[31:8]			RSVD	
[7:0]	rw	8'h0	BS	burst size in non-m2m mode When BS>1, DMA will transfer for BS times for each request if left NDT is larger than BS, or else transfer for left NDT times. When BS=0 or 1, DMA will always do single transfer for each request. In memory-to-memory mode, BS is ignored.
0x6C			**CCR6**	
[31:15]			RSVD	
[14]	rw	1'h0	MEM2MEM	memory-to-memory mode 0: disabled 1: enabled
[13:12]	rw	2'h0	PL	priority level 00: low 01: medium 10: high 11: very high

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表 6-4: DMAC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[11:10]	rw	2'h0	MSIZE	memory size Defines the data size of each DMA transfer to the identified memory. In memory-to-memory mode, this field identifies the memory source if DIR = 1 and the memory destination if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral source if DIR = 1 and the peripheral destination if DIR = 0. 00: 8 bits 01: 16 bits 10: 32 bits 11: reserved
[9:8]	rw	2'h0	PSIZE	peripheral size Defines the data size of each DMA transfer to the identified peripheral. In memory-to-memory mode, this field identifies the memory destination if DIR = 1 and the memory source if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral destination if DIR = 1 and the peripheral source if DIR = 0. 00: 8 bits 01: 16 bits 10: 32 bits 11: reserved
[7]	rw	1'h0	MINC	memory increment mode Defines the increment mode for each DMA transfer to the identified memory. In memory-to-memory mode, this field identifies the memory source if DIR = 1 and the memory destination if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral source if DIR = 1 and the peripheral destination if DIR = 0. 0: disabled 1: enabled
[6]	rw	1'h0	PINC	peripheral increment mode Defines the increment mode for each DMA transfer to the identified peripheral. n memory-to-memory mode, this field identifies the memory destination if DIR = 1 and the memory source if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral destination if DIR = 1 and the peripheral source if DIR = 0. 0: disabled 1: enabled
[5]	rw	1'h0	CIRC	circular mode 0: disabled 1: enabled

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表 6-4: DMAC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[4]	rw	1'h0	DIR	data transfer direction This bit must be set only in memory-to-peripheral and peripheral-to-memory modes. 0: read from peripheral Source attributes are defined by PSIZE and PINC, plus the CPARx register. This is still valid in a memory-to-memory mode. Destination attributes are defined by MSIZE and MINC, plus the CM0ARx register. This is still valid in a peripheral-to-peripheral mode. 1: read from memory Destination attributes are defined by PSIZE and PINC, plus the CPARx register. This is still valid in a memory-to-memory mode. Source attributes are defined by MSIZE and MINC, plus the CM0ARx register. This is still valid in a peripheral-to-peripheral mode.
[3]	rw	1'h0	TEIE	transfer error interrupt enable 0: disabled 1: enabled
[2]	rw	1'h0	HTIE	half transfer interrupt enable 0: disabled 1: enabled
[1]	rw	1'h0	TCIE	transfer complete interrupt enable 0: disabled 1: enabled
[0]	rw	1'h0	EN	channel enable When a channel transfer error occurs, this bit is cleared by hardware. It can not be set again by software (channel x re-activated) until the TEIFx bit of the ISR register is cleared (by setting the CTEIFx bit of the IFCR register). 0: disabled 1: enabled
0x70			**CNDTR6**	
[31:16]			RSVD	
[15:0]	rw	16'h0	NDT	number of data to transfer (0 to 2^{16} - 1) This field is updated by hardware when the channel is enabled: It is decremented after each single DMA 'read followed by write' transfer, indicating the remaining amount of data items to transfer. It is kept at zero when the programmed amount of data to transfer is reached, if the channel is not in circular mode (CIRC = 0 in the CCRx register). It is reloaded automatically by the previously programmed value, when the transfer is complete, if the channel is in circular mode (CIRC = 1). If this field is zero, no transfer can be served whatever the channel status (enabled or not).
0x74			**CPAR6**	
[31:0]	rw	32'h0	PA	peripheral address It contains the base address of the peripheral data register from/to which the data will be read/written. In memory-to-memory mode, this register identifies the memory destination address if DIR = 1 and the memory source address if DIR = 0. In peripheral-to-peripheral mode, this register identifies the peripheral destination address DIR = 1 and the peripheral source address if DIR = 0.
0x78			**CM0AR6**	

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表 6-4: DMAC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:0]	rw	32'h0	MA	peripheral address It contains the base address of the memory from/to which the data will be read/written. In memory-to-memory mode, this register identifies the memory source address if DIR = 1 and the memory destination address if DIR = 0. In peripheral-to-peripheral mode, this register identifies the peripheral source address DIR = 1 and the peripheral destination address if DIR = 0.
0x7C			**CBSR6**	
[31:8]			RSVD	
[7:0]	rw	8'h0	BS	burst size in non-m2m mode When BS>1, DMA will transfer for BS times for each request if left NDT is larger than BS, or else transfer for left NDT times. When BS=0 or 1, DMA will always do single transfer for each request. In memory-to-memory mode, BS is ignored.
0x80			**CCR7**	
[31:15]			RSVD	
[14]	rw	1'h0	MEM2MEM	memory-to-memory mode 0: disabled 1: enabled
[13:12]	rw	2'h0	PL	priority level 00: low 01: medium 10: high 11: very high
[11:10]	rw	2'h0	MSIZE	memory size Defines the data size of each DMA transfer to the identified memory. In memory-to-memory mode, this field identifies the memory source if DIR = 1 and the memory destination if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral source if DIR = 1 and the peripheral destination if DIR = 0. 00: 8 bits 01: 16 bits 10: 32 bits 11: reserved
[9:8]	rw	2'h0	PSIZE	peripheral size Defines the data size of each DMA transfer to the identified peripheral. In memory-to-memory mode, this field identifies the memory destination if DIR = 1 and the memory source if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral destination if DIR = 1 and the peripheral source if DIR = 0. 00: 8 bits 01: 16 bits 10: 32 bits 11: reserved

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表 6-4: DMAC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[7]	rw	1'h0	MINC	memory increment mode Defines the increment mode for each DMA transfer to the identified memory. In memory-to-memory mode, this field identifies the memory source if DIR = 1 and the memory destination if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral source if DIR = 1 and the peripheral destination if DIR = 0. 0: disabled 1: enabled
[6]	rw	1'h0	PINC	peripheral increment mode Defines the increment mode for each DMA transfer to the identified peripheral. n memory-to-memory mode, this field identifies the memory destination if DIR = 1 and the memory source if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral destination if DIR = 1 and the peripheral source if DIR = 0. 0: disabled 1: enabled
[5]	rw	1'h0	CIRC	circular mode 0: disabled 1: enabled
[4]	rw	1'h0	DIR	data transfer direction This bit must be set only in memory-to-peripheral and peripheral-to-memory modes. 0: read from peripheral Source attributes are defined by PSIZE and PINC, plus the CPARx register. This is still valid in a memory-to-memory mode. Destination attributes are defined by MSIZE and MINC, plus the CM0ARx register. This is still valid in a peripheral-to-peripheral mode. 1: read from memory Destination attributes are defined by PSIZE and PINC, plus the CPARx register. This is still valid in a memory-to-memory mode. Source attributes are defined by MSIZE and MINC, plus the CM0ARx register. This is still valid in a peripheral-to-peripheral mode.
[3]	rw	1'h0	TEIE	transfer error interrupt enable 0: disabled 1: enabled
[2]	rw	1'h0	HTIE	half transfer interrupt enable 0: disabled 1: enabled
[1]	rw	1'h0	TCIE	transfer complete interrupt enable 0: disabled 1: enabled
[0]	rw	1'h0	EN	channel enable When a channel transfer error occurs, this bit is cleared by hardware. It can not be set again by software (channel x re-activated) until the TEIFx bit of the ISR register is cleared (by setting the CTEIFx bit of the IFCR register). 0: disabled 1: enabled

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表 6-4: DMAC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
0x84			**CNDTR7**	
[31:16]			RSVD	
[15:0]	rw	16'h0	NDT	number of data to transfer (0 to 2^{16} - 1) This field is updated by hardware when the channel is enabled: It is decremented after each single DMA 'read followed by write' transfer, indicating the remaining amount of data items to transfer. It is kept at zero when the programmed amount of data to transfer is reached, if the channel is not in circular mode (CIRC = 0 in the CCRx register). It is reloaded automatically by the previously programmed value, when the transfer is complete, if the channel is in circular mode (CIRC = 1). If this field is zero, no transfer can be served whatever the channel status (enabled or not).
0x88			**CPAR7**	
[31:0]	rw	32'h0	PA	peripheral address It contains the base address of the peripheral data register from/to which the data will be read/written. In memory-to-memory mode, this register identifies the memory destination address if DIR = 1 and the memory source address if DIR = 0. In peripheral-to-peripheral mode, this register identifies the peripheral destination address DIR = 1 and the peripheral source address if DIR = 0.
0x8C			**CM0AR7**	
[31:0]	rw	32'h0	MA	peripheral address It contains the base address of the memory from/to which the data will be read/written. In memory-to-memory mode, this register identifies the memory source address if DIR = 1 and the memory destination address if DIR = 0. In peripheral-to-peripheral mode, this register identifies the peripheral source address DIR = 1 and the peripheral destination address if DIR = 0.
0x90			**CBSR7**	
[31:8]			RSVD	
[7:0]	rw	8'h0	BS	burst size in non memory-to-memory mode When BS>1, DMA will transfer for BS times for each request if left NDT is larger than BS, or else transfer for left NDT times. When BS=0 or 1, DMA will always do single transfer for each request. In memory-to-memory mode, BS is ignored.
0x94			**CCR8**	
[31:15]			RSVD	
[14]	rw	1'h0	MEM2MEM	memory-to-memory mode 0: disabled 1: enabled
[13:12]	rw	2'h0	PL	priority level 00: low 01: medium 10: high 11: very high

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表 6-4: DMAC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[11:10]	rw	2'h0	MSIZE	memory size Defines the data size of each DMA transfer to the identified memory. In memory-to-memory mode, this field identifies the memory source if DIR = 1 and the memory destination if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral source if DIR = 1 and the peripheral destination if DIR = 0. 00: 8 bits 01: 16 bits 10: 32 bits 11: reserved
[9:8]	rw	2'h0	PSIZE	peripheral size Defines the data size of each DMA transfer to the identified peripheral. In memory-to-memory mode, this field identifies the memory destination if DIR = 1 and the memory source if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral destination if DIR = 1 and the peripheral source if DIR = 0. 00: 8 bits 01: 16 bits 10: 32 bits 11: reserved
[7]	rw	1'h0	MINC	memory increment mode Defines the increment mode for each DMA transfer to the identified memory. In memory-to-memory mode, this field identifies the memory source if DIR = 1 and the memory destination if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral source if DIR = 1 and the peripheral destination if DIR = 0. 0: disabled 1: enabled
[6]	rw	1'h0	PINC	peripheral increment mode Defines the increment mode for each DMA transfer to the identified peripheral. n memory-to-memory mode, this field identifies the memory destination if DIR = 1 and the memory source if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral destination if DIR = 1 and the peripheral source if DIR = 0. 0: disabled 1: enabled
[5]	rw	1'h0	CIRC	circular mode 0: disabled 1: enabled

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表 6-4: DMAC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[4]	rw	1'h0	DIR	data transfer direction This bit must be set only in memory-to-peripheral and peripheral-to-memory modes. 0: read from peripheral Source attributes are defined by PSIZE and PINC, plus the CPARx register. This is still valid in a memory-to-memory mode. Destination attributes are defined by MSIZE and MINC, plus the CM0ARx register. This is still valid in a peripheral-to-peripheral mode. 1: read from memory Destination attributes are defined by PSIZE and PINC, plus the CPARx register. This is still valid in a memory-to-memory mode. Source attributes are defined by MSIZE and MINC, plus the CM0ARx register. This is still valid in a peripheral-to-peripheral mode.
[3]	rw	1'h0	TEIE	transfer error interrupt enable 0: disabled 1: enabled
[2]	rw	1'h0	HTIE	half transfer interrupt enable 0: disabled 1: enabled
[1]	rw	1'h0	TCIE	transfer complete interrupt enable 0: disabled 1: enabled
[0]	rw	1'h0	EN	channel enable When a channel transfer error occurs, this bit is cleared by hardware. It can not be set again by software (channel x re-activated) until the TEIFx bit of the ISR register is cleared (by setting the CTEIFx bit of the IFCR register). 0: disabled 1: enabled
0x98			**CNDTR8**	
[31:16]			RSVD	
[15:0]	rw	16'h0	NDT	number of data to transfer (0 to 2^{16} - 1) This field is updated by hardware when the channel is enabled: It is decremented after each single DMA 'read followed by write' transfer, indicating the remaining amount of data items to transfer. It is kept at zero when the programmed amount of data to transfer is reached, if the channel is not in circular mode (CIRC = 0 in the CCRx register). It is reloaded automatically by the previously programmed value, when the transfer is complete, if the channel is in circular mode (CIRC = 1). If this field is zero, no transfer can be served whatever the channel status (enabled or not).
0x9C			**CPAR8**	
[31:0]	rw	32'h0	PA	peripheral address It contains the base address of the peripheral data register from/to which the data will be read/written. In memory-to-memory mode, this register identifies the memory destination address if DIR = 1 and the memory source address if DIR = 0. In peripheral-to-peripheral mode, this register identifies the peripheral destination address DIR = 1 and the peripheral source address if DIR = 0.
0xA0			**CM0AR8**	

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表 6-4: DMAC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:0]	rw	32'h0	MA	peripheral address It contains the base address of the memory from/to which the data will be read/written. In memory-to-memory mode, this register identifies the memory source address if DIR = 1 and the memory destination address if DIR = 0. In peripheral-to-peripheral mode, this register identifies the peripheral source address DIR = 1 and the peripheral destination address if DIR = 0.
0xA4			**CBSR8**	
[31:8]			RSVD	
[7:0]	rw	8'h0	BS	burst size in non-m2m mode When BS>1, DMA will transfer for BS times for each request if left NDT is larger than BS, or else transfer for left NDT times. When BS=0 or 1, DMA will always do single transfer for each request. In memory-to-memory mode, BS is ignored.
0xA8			**CSELR1**	
[31:30]			RSVD	
[29:24]	rw	6'h0	C4S	DMA channel 4 selection
[23:22]			RSVD	
[21:16]	rw	6'h0	C3S	DMA channel 3 selection
[15:14]			RSVD	
[13:8]	rw	6'h0	C2S	DMA channel 2 selection
[7:6]			RSVD	
[5:0]	rw	6'h0	C1S	DMA channel 1 selection
0xAC			**CSELR2**	
[31:30]			RSVD	
[29:24]	rw	6'h0	C8S	DMA channel 8 selection
[23:22]			RSVD	
[21:16]	rw	6'h0	C7S	DMA channel 7 selection
[15:14]			RSVD	
[13:8]	rw	6'h0	C6S	DMA channel 6 selection
[7:6]			RSVD	
[5:0]	rw	6'h0	C5S	DMA channel 5 selection

6.2 ExtDMA

ExtDMA 位于 HPSYS。

6.2.1 简介

ExtDMA (Extended Direct Memory Access) 能够对总线上两个不同地址区间的数据进行高效率搬运工作，并集成 TurboPixel 图像帧压缩引擎，可在搬运的同时完成图像压缩。与 DMAC 相比，ExtDMA 在访问外部存储器 (如 FLASH、PSRAM) 时效率更高，但仅有一个通道，仅支持 4 字节对齐搬运，且不响应外设请求。

6.2.2 主要特性

- 单 AHB 主控，可访问 SRAM，PSRAM，FLASH 等，支持 BURST 传输
- 单个传输通道，内置深度为 16 ，位宽 32 比特的 FIFO

- 源地址和目标地址均为 4 字节访问，并支持地址自动递增
- 单次配置最大传输单元数为 2^{20}-1，每单元固定 4 字节传输，即单次最大传输 4M 字节
- 通道支持传输完成、过半传输、传输出错事件标志，并能产生中断请求及 PTC 触发
- 集成 TurboPixel 图像帧压缩引擎，支持 RGB565/RGB888/ARGB8888 格式输入，单行最大支持 512 像素

6.2.3 功能描述

6.2.3.1 传输效率

ExtDMA 和 CPU 及其它主控设备共享 AHB 总线。当 CPU 和 ExtDMA 同时访问相同的存储器时，ExtDMA 请求可能会暂停 CPU 访问系统总线，由总线仲裁器执行循环调度，以保证 CPU 至少可以得到部分总线带宽。同理，当其它主控设备与 ExtDMA 访问相同 AHB 目标时，ExtDMA 访问带宽也会下降。ExtDMA 优先采用 AHB Burst 传输模式，因此在访问 Burst 传输友好的存储器时，传输效率会优于 DMAC。

6.2.3.2 工作模式

ExtDMA 不能响应外设请求，工作模式包括搬运模式与压缩模式两种。

CMPRCR_CMPREN 为 0 时，ExtDMA 处于搬运模式，能够将指定容量的存储器数据从源地址搬运至目标地址。

CMPRCR_CMPREN 为 1 时，ExtDMA 处于压缩模式，能够启动 TurboPixel 压缩引擎对保存在源地址的指定容量的图像数据进行压缩，并将压缩结果保存到目标地址。

6.2.3.3 数据地址与位宽

ExtDMA 的源地址 SRCAR 与目标地址 DSTAR 都必须为四字节对齐，并且源数据位宽 CCR_SRCSIZE 与目标数据位宽 CCR_DSTSIZE 也必须设置为四字节。

如果使能了地址递增（源地址和目标地址由 CCR_SRCINC 和 CCR_DSTINC 分别配置），ExtDMA 每完成一次源数据读取或目标数据写入操作，则下次读取或写入操作的地址是前一次的地址加上 4，否则会保持同样地址。地址非递增的模式主要用于访问固定入口地址的 FIFO，如 CRC 的数据入口。

6.2.3.4 传输使能

CCR_EN 是通道使能寄存器。当 CCR_EN 为 1 且 CNDTR 不为 0 时，数据传输就会启动。需要注意当通道使能时，即使上一笔传输已经完成，重新写入非 0 的 CNDTR 也会立刻启动 ExtDMA 传输，所以在此之前应当确保其它参数已经配置完毕，否则应首先关闭通道使能。

6.2.3.5 传输数量

搬运模式下，数据搬运的数量通过 CNDTR 配置，以四字节为一个单元计数，支持范围 0 到 2^{20}-1。例如 CNDTR 配置为 1000 时，则传输数据量为 4000 字节。启动数据搬运后，每完成一次四字节读取，CNDTR 减 1。CMPRNDTR 表示待写入数据量，在搬运模式下不需要软件配置。启动数据搬运后，CMPRNDTR 自动复制初始 CNDTR，之后每完成一次四字节写入，CMPRNDTR 减 1。CNDTR 与 CMPRNDTR 都减到 0 时，数据读取与写入全部完成，ExtDMA 停止传输。

压缩模式下，待压缩图像的数据量通过 CNDTR 配置，以四字节为一个单元计数，支持范围 0 到 2^{20}-1。例如 CNDTR 配置为 1000 时，则待压缩图像为 4000 字节。启动数据搬运后，每完成一次四字节读取，CNDTR 减

1。CMPRNDTR 表示图像压缩后的数据量，在压缩模式下需要软件根据公式计算并写入。CMPRNDTR 的计算公式为 TGTSIZE*6* 待压缩图像总行数/4，其中 TGTSIZE 与待压缩图像总行数中必须至少有一个是偶数。如果 CMPRNDTR 软件配置有误，ExtDMA 可能无法正常完成传输。启动数据搬运后，CMPRNDTR 每完成一次四字节写入，CMPRNDTR 减 1。CNDTR 与 CMPRNDTR 都减到 0 时，数据读取与写入全部完成，ExtDMA 停止传输。

6.2.3.6 TurboPixel 压缩

ExtDMA 内嵌 TurboPixel 图像帧压缩引擎，能够将原始图像压缩并输出至目标地址，压缩过程不需要占用额外内存空间。

原始图像支持 RGB565/RGB888/ARGB8888 格式，由 CMPRCR_SRCFMT 寄存器配置。原始图像储存的起始地址对齐方式由 CMPRCR_SRCPOS 寄存器配置。其中 ARGB8888 图像储存的起始地址必须为四字节对齐。RGB565 图像储存的起始地址必须为双字节对齐。RGB888 图像储存的起始地址没有对齐要求。需要注意虽然图像起始地址支持非四字节对齐，但 ExtDMA 的搬运源地址 SRCAR 必须配置为图像起始地址所在的四字节对齐地址。

原始图像每行像素点由 CMPRSR_LINESIZE 配置，最大可支持到 512。

图像的压缩率通过相关联的两个寄存器 CMPRSR_TGTSIZE 与 CMPRNDTR 配置。压缩前后数据量的比值近似 (因为原始图像可能非对齐) 等于 CNDTR 与 CMPRNDTR 的比值。图像压缩参数通过 CMPRCFG0 和 CMPRCFG1 寄存器配置，需根据压缩率和图像格式调整。

图像压缩的品质可以通过 CMPRQR 和 CMPRDR 寄存器评价。需要注意在较高压缩率 (压缩后数据量较小) 配置下，可能存在个别特殊样式的图像压缩品质出现异常，此时会上报溢出错误中断 OFIF。当出现这种异常时，可避免使用类似样式的图像，或降低压缩率 (增大压缩后的数据量)。

6.2.3.7 通知机制

ExtDMA 可产生中断和 PTC 触发信号，并可单独配置每种中断的使能。传输完成至少一半时，产生 HTIF 中断和触发。传输全部完成后，产生 TCIF 中断和触发。传输发生总线访问错误时，产生 TEIF 中断和触发。压缩模式下发生溢出错误时，产生 OFIF 中断和触发。

中断通过 CCR 寄存器中 TCIE/HTIE/TEIE/OFIE 等控制位使能。中断状态可通过 ISR 寄存器访问，并通过 IFCR 寄存器清除。

6.2.3.8 异常处理

如果因为配置错误造成 ExtDMA 传输无法结束，可将 CCR_RESET 置 1 复位 ExtDMA 逻辑。复位后 CCR_RESET 会自动清 0。其它配置寄存器不会被该操作复位。

6.2.3.9 搬运模式推荐配置流程

1. 设置搬运模式，CMPRCR_CMPREN 为 0。
2. 设置四字节对齐的源地址 SRCAR 与目标地址 DSTAR。
3. 确保 CCR_EN 为 0 时，以四字节为单位，将待传输的数据量写入 CNDTR 寄存器。
4. 在 CCR 寄存器中配置下列参数：
    - 地址递增模式 CR_SRCINC 和 CCR_DSTINC
    - 源数据位宽 CCR_SRCSIZE 与目标数据位宽 CCR_DSTSIZE 为四字节
    - 中断使能

5. 将 CCR_EN 置 1，启动数据搬运。
6. 等待中断到来并处理，将 CCR_EN 置 0。

6.2.3.10 压缩模式推荐配置流程

1. 设置压缩模式，CMPRCR_CMPREN 为 1。
2. CMPRCR 中设置源图像格式与起始地址对齐方式。
3. 设置四字节对齐的源地址 SRCAR 与目标地址 DSTAR。
4. 确保 CCR_EN 为 0 时，以四字节为单位，将源图像数据量写入 CNDTR 寄存器。
5. 配置压缩参数 CMPRSR，CMPRCFG0 和 CMPRCFG1。
6. 计算压缩后数据量，并配置 CMPRNDTR。
7. 在 CCR 寄存器中配置下列参数：
   - 地址递增模式 CR_SRCINC 和 CCR_DSTINC
   - 源数据位宽 CCR_SRCSIZE 与目标数据位宽 CCR_DSTSIZE 为四字节
   - 中断使能
8. 将 CCR_EN 置 1，启动图像压缩。
9. 等待中断到来并处理，将 CCR_EN 置 0。

6.2.4 ExtDMA 寄存器

表 6-5: ExtDMA 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00			**ISR**	interrupt status register
[31:5]			RSVD	
[4]	r	1'h0	OFIF	OFIF, overflow flag
[3]	r	1'h0	TEIF	TEIF, transfer error flag
[2]	r	1'h0	HTIF	HTIF, half transfer flag
[1]	r	1'h0	TCIF	TCIF, transfer complete flag
[0]	r	1'h0	GIF	GIF, global interrupt flag
0x04			**IFCR**	interrupt clear register
[31:5]			RSVD	
[4]	w1s	1'h0	COFIF	COFIF, overflow flag clear
[3]	w1s	1'h0	CTEIF	CTEIF, transfer error flag clear
[2]	w1s	1'h0	CHTIF	CHTIF, half transfer flag clear
[1]	w1s	1'h0	CTCIF	CTCIF, transfer complete flag clear
[0]	w1s	1'h0	CGIF	CGIF, global interrupt flag clear
0x08			**CCR**	channel control register
[31]	w1s	1'h0	RESET	Software reset, will clear extdma status. Active high. Will be cleared by HW automatically
[30:20]			RSVD	
[19:18]	rw	2'h3	SRCBURST	source burst transfer configuration 00: single transfer 01: INCR4 (incremental burst of 4 beats) 10: INCR8 (incremental burst of 8 beats) 11: INCR16 (incremental burst of 16 beats)

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表 6-5: ExtDMA 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[17:16]	rw	2'h3	DSTBURST	destination burst transfer configuration 00: single transfer 01: INCR4 (incremental burst of 4 beats) 10: INCR8 (incremental burst of 8 beats) 11: INCR16 (incremental burst of 16 beats)
[15:12]			RSVD	
[11:10]	rw	2'h2	SRCSIZE	source size Defines the data size of each DMA transfer to the source memory. Should be fixed to 10 (32 bits), word access allowed only.
[9:8]	rw	2'h2	DSTSIZE	destination size Defines the data size of each DMA transfer to the destination memory. Should be fixed to 10 (32 bits), word access allowed only.
[7]	rw	1'h1	SRCINC	source increment mode Defines the increment mode for each DMA transfer to the source memory. 0: disabled 1: enabled
[6]	rw	1'h1	DSTINC	destination increment mode Defines the increment mode for each DMA transfer to the destination memory. 0: disabled 1: enabled
[5]			RSVD	
[4]	rw	1'h0	OFIE	overflow interrupt enable 0: disabled 1: enabled
[3]	rw	1'h0	TEIE	transfer error interrupt enable 0: disabled 1: enabled
[2]	rw	1'h0	HTIE	half transfer interrupt enable 0: disabled 1: enabled
[1]	rw	1'h0	TCIE	transfer complete interrupt enable 0: disabled 1: enabled
[0]	rw	1'h0	EN	extdma enable. Will be cleared if ccr_reset is written
0x0C			**CNDTR**	number of data register
[31:20]			RSVD	
[19:0]	rw	20'h0	NDT	number of data to transfer (0 to 2^{20} - 1) This field is updated by hardware when the channel is enabled: It is decremented after each transfer, indicating the remaining amount of data items to transfer. It is kept at zero when the programmed amount of data to transfer is reached. If this field is zero, no transfer can be served whatever the channel enabled or not
0x10			**SRCAR**	source address register
[31:0]	rw	32'h0	SRCADDR	source address It contains the base address of the source data to be read. Should be word aligned
0x14			**DSTAR**	destination 0 address register
[31:0]	rw	32'h0	DSTADDR	destination address It contains the base address of the destination data to be written. Should be word aligned

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表 6-5: ExtDMA 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
0x20			**CMPRCR**	Image Compression control register
[31:8]			RSVD	
[7:6]	rw	2'h0	SRCPOS	Starting byte position in the first word of the source frame Valid starting positon includes: RGB565: 0x0,0x2 RGB888: 0x0, 0x1, 0x2, 0x3 ARGB8888: 0x0
[5:4]	rw	2'h0	SRCFMT	Source frame format 00: 16-bit RGB 5:6:5 01: 24-bit RGB 8:8:8 10: 32-bit ARGB 8:8:8:8 11: Reserved
[3:1]			RSVD	
[0]	rw	1'h0	CMPREN	Compression enable
0x24			**CMPRSR**	Compression size register
[31:28]			RSVD	
[27:16]	rw	12'h0	TGTSIZE	output target size of each line after compression. output data size of each line is tgtsize*3*2 bytes
[15:12]			RSVD	
[11:0]	rw	12'h0	LINESIZE	column number (pixel number) of each line. Input data size of each line is linesize*(size per pixel)
0x28			**CMPRNDTR**	number of compression output data register
[31:20]			RSVD	
[19:0]	rw	20'h0	CMPRNDT	If compression enabled, cmprndt is the number of data to transfer after compression (0 to 2^{20} - 1) and have to be written by software before compression. The value should be TGTSIZE*6*line_number/4 in compression mode. If compression disabled, it reads the number of data that extdma has written into destination address. Software do not need to write this field. This field is updated by hardware when extdma enabled
0x2C			**CMPRCFG0**	Compression configuration 0
[31:0]	rw	32'h80023307	CFG	Compression configuration
0x30			**CMPRCFG1**	Compression configuration 1
[31:0]	rw	32'h01055982	CFG	Compression configuration
0x34			**CMPRQR**	Compression quality register
[31:29]			RSVD	
[28:16]	r	13'h0	DUMMY	line least dummy word in one frame, update every frame.
[15:8]	r	8'h0	LQB	low quality block number. the bigger of this number, the worse compressed image quality
[7:0]	r	8'h0	LQR	quality sum to low qulity block number ratio. the bigger of this number, the worse compressed image quality.
0x38			**CMPRDR**	Compression debug register
[31:7]			RSVD	
[6:0]	r	7'h0	MAXBUF	record of max used buffer during compression output

7 连接外设

7.1 I2C

芯片共有 7 个 I2C，其中 I2C1，I2C2，I2C3 和 I2C4 位于 HPSYS，输入输出连接至 IO(PA)，可向 DMAC1 发送请求；I2C5，I2C6 和 I2C7 位于 LPSYS，输入输出连接至 IO(PB)，可向 DMAC2 发送请求。

7.1.1 简介

I2C(Inter-Integrated Circuit) 接口同时支持主设备与从设备角色，可作为主设备与 I2C 外设通信，也可作为从设备响应外部的 I2C 主设备。I2C 内置 8 字节 FIFO，可以进行单笔读写，也可通过 DMA 进行批量数据读写。I2C 支持标准模式 (standard-mode)、快速模式 (fast-mode)、增强快速模式 (fast-mode plus) 以及高速模式 (high-speed-mode)，最高速率可达 3.4Mbps。

7.1.2 主要特性

可同时作为主设备与从设备

- 支持总线多主设备
- 支持标准模式 (最高 100kbps)
- 支持快速模式 (最高 400kbps)
- 支持增强快速模式 (最高 1Mbps)
- 支持高速模式 (最高 3.4Mbps)
- 作为主设备支持访问 7 比特或 10 比特寻址
- 作为从设备支持 7 比特寻址
- 可配置的总线时序
- 支持时钟延展 (clock stretching)
- 8 字节 FIFO，支持 DMA
- 可配置的数字防抖动电路
- 独立的功能时钟，支持系统时钟动态调节

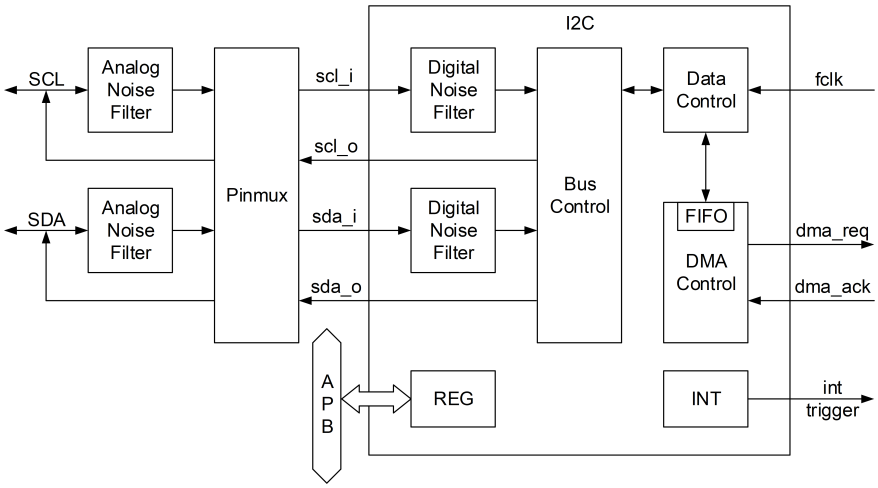

图 7-1: I2C 结构图

7.1.3 I2C 功能描述

7.1.3.1 两线传输

I2C 总线利用 SCL 与 SDA 两根线进行传输，其中 SCL 通常称为时钟线，SDA 通常称为数据线。两根线均为双向传输，且输出均为开漏模式，因此需要在芯片外部增加上拉电阻，阻值应根据最大传输速率决定。I2C 总线空闲时，SCL 与 SDA 均为上拉高电平。可通过 BMR_SCL 和 BMR_SDA 查询当前 I2C 总线信号电平。

7.1.3.2 输入滤波器

SCL 与 SDA 输入信号可经由模拟滤波器和数字滤波器滤除毛刺。模拟滤波器可滤除小于 50ns 的毛刺，在 PINMUX 模块中配置。数字滤波器可通过配置 CR_DNF 选择滤除毛刺的宽度上限，最大可配置为 7 个 fclk 周期 (约 146ns)。

7.1.3.3 传输速率

I2C 的传输速率主要由主设备决定，但当从设备支持时钟延展 (clock stretching) 时，也会受从设备影响。

I2C 接口时序基于 fclk 产生。该时钟来自芯片的外设时钟，独立于系统时钟，因此系统时钟频率的变化不会影响 I2C 的传输速率。

根据 I2C 协议，标准模式 (standard-mode) 比特率最高为 100kbps，快速模式 (fast-mode) 比特率最高为 400kbps，增强快速模式 (fast-mode plus) 比特率最高为 1Mbps，高速模式 (high-speed mode) 比特率最高为 3.4Mbps。

标准模式的基础比特率可由下列近似公式计算：

$$bit\_rate = Ffclk/(LCR\_SLV + max(LCR\_SLV, (WCR\_CNT \times 2 + 6)) + 7 + CR\_DNF)$$

其中，Ffclk 为 fclk 的频率 (48MHz)。WCR_CNT 用于调整 SDA 与 SCL 边沿之间的偏移，以保证信号的建立与保持时间满足 I2C 协议，配置合理时不会影响比特率。

快速模式/增强快速模式的基础比特率可由下列近似公式计算：

$$bitrate = Ffclk/(LCR\_FLV + max(LCR\_FLV, (WCR\_CNT \times 2 + 6)) + 7 + CR\_DNF)$$

7.1.3.4 传输序列

一次完整的 I2C 传输应基于下列传输序列进行：

1. 起始位。主设备发出，启动传输。
2. 7 比特从地址。主设备发出，用于选择从设备。
3. R/nW 比特。主设备发出，标志接收或发送方向。
4. ACK 比特。从设备发出，响应主设备请求。ACK=0 表示响应成功。ACK=1 则传输失败。
5. 8 比特数据。接收时由从设备发出，发送时由主设备发出。根据不同从设备的访问方式，可能代表寄存器地址或数据。
6. ACK 比特。接收时由主设备发出，发送时由从设备发出，是对之前 8 比特数据的响应。
7. 重复步骤 5-6 直至数据完成或出现 ACK=1。
8. 重复起始位 (回到步骤 1) 或停止位。主设备发出，重新启动传输或停止传输。

7.1.3.5 工作模式与状态

I2C 默认处于主模式，可以发起主动传输，但不监控总线上的地址传输。软件启动传输时，I2C 进入主发送或主接收状态。

若将 CR_SLVEN 置 1，则 I2C 进入主从模式，可以发起主动传输，同时监控总线上的地址传输。软件启动传输时，I2C 进入主发送或主接收状态。当监控到起始位之后的 7 位地址与 SAR_ADDR 相符时，I2C 根据 R/nW 比特进入从发送或从接收状态。

7.1.3.6 I2C 初始化流程

1. 配置 I2C 速率模式 CR_MODE，并根据速率配置相关时序寄存器 LCR、WCR 等
2. 配置 IER 使能所需中断
3. 使能 I2C，CR_SCLE=1，CR_IUE=1

7.1.3.7 主发送流程

1. 将从设备地址左移 1 位，拼上最低位 0，写入 DBR。
2. TCR=TCR_START;TCR|=TCR_TB。
3. 轮询 SR_TE 直到为 1，或等待发送完成 TE 中断。
4. SR_TE 写 1 清除标志。检查 SR_NACK，如果为 1 则发送停止位并中止传输。
5. 将待发送数据写入 DBR。
6. TCR=TCR_TB。
7. 轮询 SR_TE 直到为 1，或等待 TE 中断。
8. SR_TE 写 1 清除标志。检查 SR_NACK，如果为 1 则发送停止位并中止传输。
9. 重复步骤 5-8，如果是最后一笔数据则 TCR=TCR_TB|TCR_STOP，停止位会在发送完成后自动产生。

7.1.3.8 主接收流程

1. 将从设备地址左移 1 位，拼上最低位 1，写入 DBR。

2. TCR=TCR_START;TCR|=TCR_TB。
3. 轮询 SR_TE 直到为 1，或等待 TE 中断。
4. SR_TE 写 1 清除标志。检查 SR_NACK，如果为 1 则发送停止位并中止传输。
5. TCR=TCR_TB。
6. 轮询 SR_RF 直到为 1，或等待接收完成 RF 中断。
7. SR_RF 写 1 清除标志。从 DBR 中获取接收的数据。
8. 重复步骤 5-7，如果是最后一笔数据则 TCR=TCR_TB|TCR_NACK。
9. TCR=TCR_MA，发送停止位。
10. 轮询 SR_UB 直到为 0，停止位发送完毕，TCR=0。

7.1.3.9 从发送流程

1. 当地址检测中断 SAD 触发后，自动回复 ACK。
2. SR_SAD 写 1 清除标志。读取 SR_RWM，1 表示从发送，0 表示从接收。假设当前 SR_RWM 为 1，进入从发送状态。
3. 将待发送数据写入 DBR。
4. TCR=TCR_TB。
5. 轮询 SR_TE 直到为 1，或等待 TE 中断。
6. SR_TE 写 1 清除标志。检查 SR_NACK，如果为 1 则中止传输。
7. 重复步骤 3-6，直到检测到停止位中断 SSD。
8. SR_SSD 写 1 清除标志。

7.1.3.10 从接收流程

1. 当地址检测中断 SAD 触发后，自动回复 ACK。
2. SR_SAD 写 1 清除标志。读取 SR_RWM，1 表示从发送，0 表示从接收。假设当前 SR_RWM 为 0，进入从接收状态。
3. TCR=TCR_TB。
4. 轮询 SR_RF 直到为 1，或等待接收完成 RF 中断。
5. SR_RF 写 1 清除标志。从 DBR 中获取接收的数据。
6. 重复步骤 3-5，如果缓存将满则 TCR=TCR_TB|TCR_NACK，直到检测到停止位中断 SSD。
7. SR_SSD 写 1 清除标志。

7.1.3.11 DMA 传输

I2C 处于主发送或主接收状态时，可以开启 DMA 传输。DMA 仅作用于数据段，不能用于传输从设备地址和 R/nW 比特。I2C 支持单次 DMA 最大 511byte 数据连续传输。如果有更多的数据传输需求，可以再次启动 DMA。

DMA 启动以后，传输过程不需要 CPU 参与，由 I2C 与 DMAC 模块直接交互完成传输，并产生中断 DMADONE。I2C 模块内置 8 字节 FIFO，用于在 DMA 传输过程中缓存数据。如果出现 FIFO 溢出，会产生上溢中断 OF 或下溢中断 UF。如果主发送过程中收到从设备产生的 ACK=1，数据传输会中止，并产生中断 DMADONE。

DMA 传输的字节数通过写 DNR_NDT 配置。剩余待传输字节数可以通过读 DNR_NDT 获取。在中断 DMADONE 发生时，通过读取 DNR_NDT 以及 SR_NACK 可以获知 DMA 传输是否正常完成。

将 CR_LASTSTOP 置 1 可以在本次 DMA 传输完成后自动发送停止位。将 CR_LASTNACK 置 1 可以在本次 DMA

接收完成后自动回复 ACK=1。

使用 DMA 进行主发送或主接收的流程如下：

1. 将从设备地址左移 1 位，拼上最低位 R/nW，写入 DBR。
2. TCR=TCR_START;TCR=TCR_TB。
3. 轮询 SR_TE 直到为 1，或等待发送完成 TE 中断。
4. SR_TE 写 1 清除标志。检查 SR_NACK，如果为 1 则发送停止位并中止传输。
5. 配置 DMAC 模块。通道外设选择为当前 I2C，数据宽度为单字节，外设地址为当前 I2C 的 FIFO 寄存器，并启动 DMAC 通道。
6. 配置 I2C 的 DMA。DNR_NDT 设为待传输字节数。如果 DMA 传输完成后需自动发送停止位，则将 CR_LASTSTOP 置 1。如果 DMA 传输完成后需自动回复 ACK=1，则将 CR_LASTNACK 置 1。CR_DMAEN 置 1 使能 DMA。
7. 等待 DMADONE 中断。
8. SR_DMADONE 写 1 清除标志。
9. 如果还需再次启动 DMA，重复步骤 5-8。
10. 轮询 SR_UB 直到为 0，停止位发送完毕。

7.1.3.12 总线异常恢复

由于电气干扰或设备异常，I2C 总线有时会出现卡死，表现为 I2C 发送或接收持续失败。当怀疑总线卡死时，可通过下述方法尝试恢复。

1. 复位 I2C 模块。CR_UR 置 1，等待 100us 后置 0。
2. 如果 BMR_SCL 和 BMR_SDA 均为 1，可将 CR_RSTREQ 置 1，并查询 CR_RSTREQ 直到变为 0。在此期间，I2C 会连续发送 RCCR_RSTCYC 个周期的时钟信号，从设备检测到这类总线信号后或可从异常中恢复。
3. 如果 BMR_SCL 或 BMR_SDA 持续为 0，怀疑上拉电阻失效或从设备挂死，需检查硬件电路或复位从设备。

7.1.4 I2C 寄存器

表 7-1: I2C 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00			**CR**	Control register
[31]	rw	1'h0	UR	Unit Reset. Software need first assert to reset then deassert to release. 0 = No reset. 1 = Reset I2C module.
[30]	rw	1'h0	RSTREQ	I2C will do bus reset upon this bit set. Will be cleared by HW automatically after RSTCYC cycles of SCL generated. 1 = request for i2c bus reset 0 = bus reset finished
[29]	rw	1'h0	BRGRST	Reset bus related state machine and signals. Will be cleared by HW automatically 1 = request for reset 0 = reset finished
[28:15]			RSVD	

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表 7-1: I2C 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[14:12]	rw	3'h0	DNF	Digital noise filter These bits are used to configure the digital noise filter on SDA and SCL input. The digital filter will filter spikes with a length of up to DNF*Tfclk. 0: Digital filter disabled 1: Digital filter enabled and filtering capability up to 1 Tfclk ... 7: digital filter enabled and filtering capability up to 7 Tfclk Digital filter is added to analog filter. Digital filter will introduce delay on SCL and SDA processing, which is essential in hs-mode.
[11]	rw	1'h0	SLVEN	Slave mode Enable for SCL. 0 = Disable slave mode. Will not monitor slave address on I2C bus. 1 = Enable slave mode. Will monitor slave address on I2C bus.
[10]			RSVD	
[9]	rw	1'h0	SCLPP	Push-pull mode Enable for SCL. 0 = open drain output for SCL. 1 = Push-pull output for SCL
[8]	rw	1'h0	MSDE	Master Stop Detected Enable: 0 = Master Stop Detect (MSD) status is not enabled. 1 = Master Stop Detect (MSD) status is enabled.
[7]			RSVD	
[6]	rw	1'h0	LASTSTOP	Generate STOP for last DMA transfer
[5]	rw	1'h0	LASTNACK	Generate NACK for last DMA Read transfer
[4]	rw	1'h0	DMAEN	DMA Enable for both TX and RX 0 = DMA mode is NOT enabled 1 = DMA mode enabled
[3]	rw	1'h0	SCLE	SCL Enable: 0 = Disables the I2C from driving the SCL line. 1 = Enables the I2C clock output for master-mode operation.
[2]	rw	1'h0	IUE	I2C Unit Enable: 0 = Disables the unit and does not master any transactions or respond to any slave transactions. 1 = Enables the I2C (defaults to slave-receive mode). Software must guarantee the I2C bus is idle before setting this bit.
[1:0]	rw	2'h0	MODE	Bus Mode (Master operation): 2'b00: standard-mode 2'b01: fast-mode and fast-mode plus 2'b10: HS-mode (standard mode when not doing a high speed transfer) 2'b11: HS-mode (fast mode when not doing a high speed transfer) Bus Mode (Slave operation): 2'b0x: HS-mode is disabled. I2C unit uses Standard/Fast mode timing on the SDA pin. 2'b1x: HS-mode is enabled. I2C unit uses HS-mode timing on the SDA pin when a master code is received.
0x04			**TCR**	Transfer Control register
[31:8]			RSVD	
[7]	w1s	1'h0	ABORTDMA	Abort DMA operation. Will be cleared by HW automatically
[6]	w1s	1'h0	RXREQ	Request DMA RX. Will be cleared by HW automatically
[5]	w1s	1'h0	TXREQ	Request DMA TX. Will be cleared by HW automatically

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表 7-1: I2C 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[4]	rw	1'h0	MA	Master Abort: Used by the I2C in master mode to generate a Stop without transmitting another data byte: 0 = The I2C transmits Stop on if TCR[STOP] is set. 1 = The I2C sends Stop without data transmission. When in master-transmit mode, after transmitting a data byte, the TCR[TB] bit is cleared. When no more data bytes need to be sent, setting master abort bit sends the Stop. The TCR[TB] bit must remain clear. In master-receive mode, when a NAK is sent without a Stop (TCR[STOP] bit was not set) and CPU does not send a repeated Start, setting this bit sends the Stop. Once again, the TCR[TB] bit must remain clear. Master Abort can be done immediately after the address phase (Master Transmit mode only).
[3]	rw	1'h0	NACK	The positive/negative acknowledge control bit, defines the type of acknowledge pulse sent by the I2C when in master receive mode: 0 = Send a positive acknowledge (ACK) pulse after receiving a data byte. 1 = Send a negative acknowledge (NACK) pulse after receiving a data byte. The I2C automatically sends an ACK pulse when responding to its slave address or when responding in slave-receive mode, regardless of the NACK control-bit setting.
[2]	rw	1'h0	STOP	Stop: Used to initiate a Stop condition after transferring the next data byte on the I2C bus when in master mode. In master-receive mode, the NACK control bit must be set in conjunction with the STOP bit. 0 = Do not send a Stop. 1 = Send a Stop.
[1]	rw	1'h0	START	Start: Used to initiate a Start condition to the I2C unit when in master mode. 0 = Do not send a Start pulse. 1 = Send a Start pulse.
[0]	rw	1'h0	TB	Transfer Byte: Used to send or receive a byte on the I2C bus: 0 = Cleared by I2C when the byte is sent/received. 1 = Send/receive a byte. CPU can monitor this bit to determine when the byte transfer has completed. In master or slave mode, after each byte transfer including acknowledge pulse, the I2C holds the SCL line low (inserting wait states) until TB is set.
0x08			**IER**	Interrupt Enable register
[31:16]			RSVD	
[15]	rw	1'h0	UFIE	FIFO Underflow Interrupt Enable 0 = FIFO Underflow interrupt is not enabled 1 = FIFO Underflow interrupt is enabled
[14]	rw	1'h0	OFIE	FIFO Overflow Interrupt Enable 0 = FIFO Overflow interrupt is not enabled 1 = FIFO Overflow interrupt is enabled
[13]	rw	1'h0	DMADONEIE	DMA Transaction Done Interrupt Enable 0 = DMA Transaction done interrupt is not enabled. 1 = DMA Transaction done interrupt is enabled.

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表 7-1: I2C 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[12]	rw	1'h0	MSDIE	Master Stop Detected Interrupt Enable: 0 = Disable interrupt. 1 = Enables the I2C unit to interrupt upon detecting a Master Stop sent by the I2C unit.
[11]			RSVD	
[10]	rw	1'h0	BEDIE	Bus Error Detected Interrupt Enable: 0 = Disable interrupt. 1 = Enables the I2C to interrupt for the following I2C bus errors: As a master transmitter, no ACK was detected after a byte was sent. As a slave receiver, the I2C generated a NACK pulse. Software is responsible for guaranteeing that misplaced Start and Stop conditions do not occur.
[9]	rw	1'h0	SADIE	Slave Address Detected Interrupt Enable: 0 = Disable interrupt. 1 = Enables the I2C to interrupt upon detecting a slave address match or a general call address.
[8]			RSVD	
[7]	rw	1'h0	RFIE	DBR Receive Full Interrupt Enable: 0 = Disable interrupt. 1 = Enables the I2C to interrupt when the DBR has received a data byte from the I2C bus.
[6]	rw	1'h0	TEIE	DBR Transmit Empty Interrupt Enable: 0 = Disable interrupt. 1 = Enables the I2C to interrupt after transmitting a byte onto the I2C bus.
[5]	rw	1'h0	ALDIE	Arbitration Loss Detected Interrupt Enable: 0 = Disable interrupt. 1 = Enables the I2C to interrupt upon losing arbitration while in master mode.
[4]	rw	1'h0	SSDIE	Slave Stop Detected Interrupt Enable: 0 = Disable interrupt. 1 = Enables the I2C to interrupt when it detects a Stop condition while in slave mode.
[3:0]			RSVD	
0x0C			**SR**	Status register
[31:16]			RSVD	
[15]	rw1c	1'h0	UF	FIFO Underflow Flag. Asserted when FIFO is empty and a POP request generated without a PUSH. Cleared if write 1
[14]	rw1c	1'h0	OF	FIFO Overflow Flag. Asserted when FIFO is full and a PUSH request generated without a POP. Cleared if write 1
[13]	rw1c	1'h0	DMADONE	DMA Transaction Done. Asserted when both APB and I2C bus have finished transfer. Cleared if write 1
[12]	rw1c	1'h0	MSD	Master Stop Detected: 0 = No Master Stop Detected. 1 = This bit is set by the I2C unit when all of the following are true: This bit is enabled (CR[MSDE] = 1); I2C unit is configured as a master; I2C transmits a STOP signal

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表 7-1: I2C 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[11]	r	1'h0	EBB	Early Bus Busy 0 = I2C bus is idle or the I2C is using the bus (that is, unit busy). 1 = Set when the unit detects that the SCL or SDA line is low without a START condition. Bit will remain set until the I2C unit detects the bus is idle by detecting a STOP condition. Bit will also be set whenever the IBB bit is set.
[10]	rw1c	1'h0	BED	Bus Error Detected: 0 = No error detected. 1 = The I2C sets this bit when it detects one of the following error conditions: As a master transmitter, no ACK was detected on the interface after a byte was sent. As a slave receiver, the I2C generates a NACK pulse. When an error occurs, I2C bus transactions continue. Software must guarantee that misplaced Start and Stop conditions do not occur. Cleared if write 1
[9]	rw1c	1'h0	SAD	Slave Address Detected: 0 = No slave address was detected. 1 = The I2C detected a seven-bit address that matches the general call address or SAR. An interrupt is signalled when enabled in the CR. Cleared if write 1
[8]			RSVD	
[7]	rw1c	1'h0	RF	DBR Receive Full: 0 = The DBR has not received a new data byte or the I2C is idle. 1 = The DBR register received a new data byte from the I2C bus. An interrupt is signalled when enabled in the CR. Cleared if write 1
[6]	rw1c	1'h0	TE	DBR Transmit Empty: 0 = The data byte is still being transmitted. 1 = The I2C has finished transmitting a data byte on the I2C bus. An interrupt is signalled when enabled in the CR. Cleared if write 1
[5]	rw1c	1'h0	ALD	Arbitration Loss Detected: Used during multi-master operation: 0 = Cleared when arbitration is won or never took place. 1 = Set when the I2C loses arbitration. Cleared if write 1
[4]	rw1c	1'h0	SSD	Slave Stop Detected: 0 = No Stop detected. 1 = Set when the I2C detects a Stop while in slave-receive or slave-transmit mode. Cleared if write 1
[3]	r	1'h0	IBB	I2C Bus Busy: 0 = I2C bus is idle or the I2C is using the bus (that is, unit busy). 1 = Set when the I2C bus is busy but local I2C is not involved in the transaction.
[2]	r	1'h0	UB	Unit Busy: 0 = I2C not busy. 1 = Set when local I2C is busy. This is defined as the time between the first Start and Stop.

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表 7-1: I2C 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[1]	r	1'h0	NACK	ACK/NACK Status: 0 = The I2C received or sent an ACK on the bus. 1 = The I2C received or sent a NACK.on the bus. This bit is used in slave-transmit mode to determine when the byte transferred is the last one. This bit is updated after each byte and ACK/NACK information is received.
[0]	r	1'h0	RWM	Read/write Mode: 0 = The I2C is in master-transmit or slave-receive mode. 1 = The I2C is in master-receive or slave-transmit mode. This is the R/nW bit of the slave address. It is cleared automatically by hardware after a Stop state.
0x10			**DBR**	Data Buffer register
[31:8]			RSVD	
[7:0]	rw	8'h0	DATA	use the I2C Data Buffer register to transmit and receive data from the I2C bus. The DBR is accessed by software on one Side and by the I2C Shift register on the other. The DBR receives data coming into the I2C unit after a full byte is received and acknowledged. CPU writes data going out of the I2C to the DBR and sends it to the serial bus. When the I2C is in transmit mode (master or slave), CPU writes data to the DBR over the internal bus. CPU write data to the DBR when a master transaction is initiated or when the DBR transmit-empty interrupt is signalled. Data moves from the DBR to the Shift register when the transfer byte bit is set. The DBR transmit-empty interrupt is signalled (if enabled) when a byte is transferred on the I2C bus and the acknowledge cycle is complete. If the DBR is not written, and a Stop condition is not in place before the I2C bus is ready to transfer the next byte packet, the I2C unit inserts wait states until CPU writes the DBR and sets the transfer byte bit. When the I2C is in receive mode (master or slave), CPU reads DBR data over the internal bus. CPU reads data from the DBR when the DBR receive-full interrupt is signalled. The data moves from the Shift register to the DBR when the acknowledge cycle is complete. The I2C inserts wait states until the DBR is read. After the software reads the DBR, CR[NACK] are written by the software, allowing the next byte transfer to proceed to the I2C bus. In DMA mode, DBR is automatically filled from FIFO in master transmit mode, or fetched and stored in FIFO in master receive mode until DMA done or aborted.
0x14			**SAR**	Slave Address Register
[31:7]			RSVD	
[6:0]	rw	7'h47	ADDR	The seven-bit address to which the I2C responds when in slave-receive mode
0x18			**LCR**	Load Count Register
[31:27]	rw	5'h1	HLVH	Decrementer Load value for High Speed Mode SCL (master mode) for high phase. Thigh=Tfclk*(HLVH+4+DNF)
[26:18]	rw	9'h7	HLVL	Decrementer Load value for High Speed Mode SCL (master mode) for low phase. Tlow=Tfclk*(HLVL+3+DNF). Data rate is generated as 1/(Thigh+Tlow), or Ffclk/(HLVH+HLVL+7+2*DNF). 3.2Mbps data rate is generated by default if fclk is 48MHz. HLVL also controls setup time and hold time for START and STOP condition in High Speed Mode(master mode). Thdsta=Tsusta=Tsusto=Tfclk*(HLVL+1)

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表 7-1: I2C 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[17:9]	rw	9'h39	FLV	Decrementer Load value for Fast Mode (or Fast Mode Plus) SCL (master mode) for both high and low phase. Data rate is generated as Ffclk/(FLV+max(FLV,CNT*2+6)+7+DNF) approximately. 400kbps data rate is generated by default if fclk is 48MHz. FLV also controls setup time and hold time for START and STOP condition in Fast Mode(master mode). Thdsta=Tsusta=Tsusto=Tfclk*FLV
[8:0]	rw	9'hED	SLV	Decrementer Load value for Standard Mode SCL (master mode) for both high & low phase. Data rate is generated as Ffclk/(SLV+max(SLV,CNT*2+6)+7+DNF) approximately. 100kbps data rate is generated by default if fclk is 48MHz. SLV also controls setup time and hold time for START and STOP condition in Standard Mode(master mode). Thdsta=Tsusta=Tsusto=Tfclk*SLV
0x1C			**WCR**	Wait Count Register
[31:8]			RSVD	
[7:0]	rw	8'hA	CNT	Controls the counter values defining the setup and hold times in standard and fast mode Tvddat=Thddat=Tfclk*(CNT+2) Tsudat=max(Tlow-Thddat,Thddat) Lower counter values may violate setup and hold times.
0x20			**RCCR**	Bus Reset Cycle Counter Register
[31:4]			RSVD	
[3:0]	rw	4'h9	RSTCYC	The cycles of SCL during bus reset
0x24			**BMR**	Bus Monitor Register
[31:2]			RSVD	
[1]	r	1'h1	SCL	value of the SCL pin. Software can check bus level when the I2C bus is hung and the I2C unit must be reset.
[0]	r	1'h1	SDA	value of the SDA pin.
0x28			**DNR**	DMA number register
[31:9]			RSVD	
[8:0]	rw	9'h0	NDT	Write as number of data to transfer in byte. Read as left data number to transfer
0x30			**FIFO**	FIFO Register
[31:8]			RSVD	
[7:0]	rw	8'h0	DATA	Write to push send data into FIFO. Read to pop received data from FIFO

7.2 SPI

芯片共有 4 个 SPI，其中 SPI1 和 SPI2 位于 HPSYS，输入输出连接至 IO(PA)，可向 DMAC1 发送请求；SPI3 和 SPI4 位于 LPSYS，输入输出连接至 IO(PB)，可向 DMAC2 发送请求。

7.2.1 简介

SPI 支持 3 种通信格式：SSP/SPI/Microwire。SSP/SPI 为全双工通信协议，控制器可以配置为 Master 或 Slave 模式。Microwire 为半双工通信协议，控制器仅可配置为 Master 模式。SPI 控制器内置发送/接收 FIFO。发送 FIFO

和接收 FIFO 共享同一个地址，读该地址时访问接受 FIFO，写该地址时访问发送 FIFO。FIFO 支持软件访问模式和 DMA 访问模式。

7.2.2 主要特性

- 支持 3 种通信格式：SSP/SPI/Microwire
- 支持 4 到 32Bit 的数据宽度
- SPI 格式下时钟极性和相位可通过寄存器 SPO 和 SPH 设置
- 片选信号极性可配
- FIFO 深度为 32Bits×16Entry
- 接收发送都支持 DMA 模式
- HPSYS 中的 SPI 最高时钟频率为 48MHz；LPSYS 中的 SPI 最高时钟频率为 24MHz。

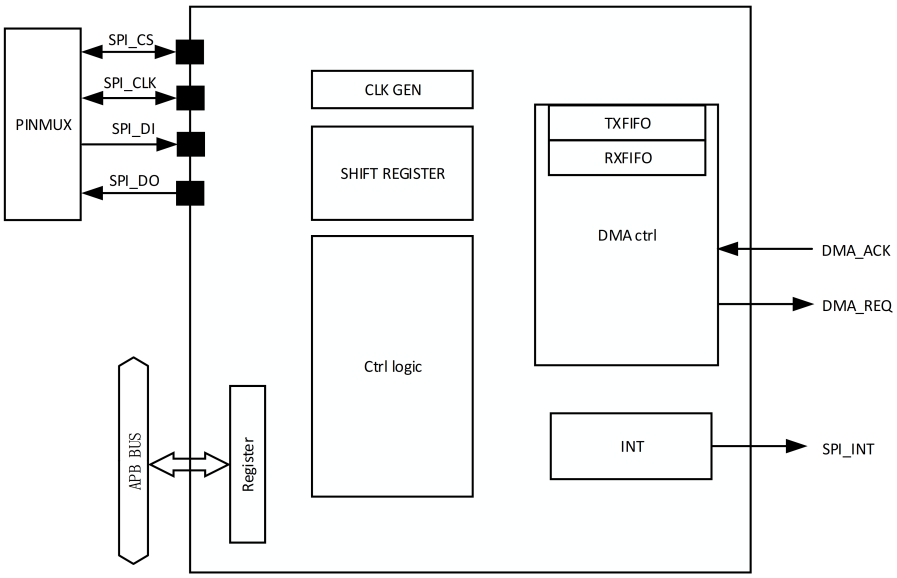

图 7-2: SPI 结构图

7.2.3 SPI 功能描述

7.2.4 接口信号

SPI_CS 用作片选信号或者数据帧开始信号。

当设置在 SPI 协议下通信时，SPI_CS 用作片选信号，在 SPI_CS 从 1 变 0 表示一次数据传输的开始，从 0 变 1 表示一次数据传输的结束。在作为 Master 进行通信时，SPI_CS 是输出信号，由内部驱动。在作为 Slave 进行通信时，SPI_CS 是输入信号，由外部驱动。

当设置在 SSP 协议下通信时，SPI_CS 用于指示一帧数据传输的开始，一个高脉冲指示一帧数据传输的开始，脉冲宽度为传输一个比特数据的时长。每帧数据的传输开始前。在作为 Master 进行通信时，SPI_CS 是输出信号，由内部驱动。在作为 Slave 进行通信时，SPI_CS 是输入信号，由外部驱动。

当设置在 Microwire 协议下通信时，SPI_CS 用作片选信号，在 SPI_CS 从 1 变 0 表示一次数据传输的开始，从 0 变 1 表示一次数据传输的结束。Microwire 协议下 SPI 只能作为 Master 进行通信，此时 SPI_CS 是输出信号，由内部驱动。

SPI_CLK 是串口通信的时钟信号，在作为 Master 进行通信时是输出信号，在作为 Slave 进行通信时是输入信号。

SPI_DO 是向外传输的数据信号，TX_FIFO 中的数据通过 SPI_DO 以 MSB first 的顺序发送出去。不管作为 Master 还是 Slave，始终是输出信号。

SPI_DI 是外部传输来的数据信号，从 SPI_DI 上接收到的数据，存到 RX_FIFO 里由 CPU 或 DMA 读取。不管作为 Master 还是 Slave，始终是输入信号。

7.2.5 FIFO

SPI 控制器中有 TXFIFO 和 RXFIFO，位宽都是 32 比特，深度都是 16。两 FIFO 都可以通过 CPU 或 DMA 访问。从地址映射的角度看，两 FIFO 共享同一地址，向该地址写数据会将数据写到 TXFIFO 中，从该地址读数据会将读出 RX_FIFO 中最早的数据。

FIFO 的一次访问只可以写入或读出一笔数据（无论数据位宽），并且对 FIFO 访问的数据位宽必须是 32 位，如果设置位宽不是 32 位，发送时 SPI 控制器会忽略 TXFIFO 的 32 比特中高于设置位宽的部分，接收时 SPI 控制器会将高于设置位宽部分补 0 后写入 RXFIFO。

FIFO 可以通过中断和 CPU 软件交互，也可以由 CPU 轮询 FIFO 状态寄存器来实现交互。CPU 根据交互结果向 TXFIFO 写数或从 RXFIFO 读数。

FIFO 通过 DMA_REQ 和 DMA 控制器交互，通知 DMA 向 TXFIFO 写数或从 RXFIFO 读数。

当 FIFO 通过中断和 CPU 交互时，产生中断的条件如下：

- 当 RXFIFO 中的数据个数大于寄存器 FIFO_CTRL 中 RFT 的值时，SPI 控制器会产生中断通知 CPU 来读取 RXFIFO 中的数据。
- 当 TXFIFO 中的数据个数小于寄存器 FIFO_CTRL 中 TFT 的值加 1 时，SPI 控制器会产生中断通知 CPU 向 TXFIFO 中写数据。

当 FIFO 通过 DMA_REQ 和 DMA 交互时，产生 DMA_REQ 的条件如下：

- 当 RXFIFO 中的数据个数大于寄存器 FIFO_CTRL 中 RFT 的值时，SPI 控制器会产生 DMA_REQ 通知 DMA 来读取 RXFIFO 中的数据。
- 当 TXFIFO 中的数据个数小于寄存器 FIFO_CTRL 中 TFT 的值加 1 时，SPI 控制器会产生 DMA_REQ 通知 DMA 向 TXFIFO 中写数据。

两种情况下都需要需要注意合理的设置，避免出现 RXFIFO overflow 或者 TXFIFO underrun 的情况出现。

7.2.6 数据格式

- SPI 格式 SPI 是全双工同步串口通信协议，根据 TOP_CTRL 寄存器中 SPO 和 SPH 的设置分为四种子模式。SPO 设置 SPI 控制器没有使能或是能后处于 IDLE 状态时候的 SPI_CLK 的极性，当 SPO 为 0 时，SPI_CLK 极性是低电压，第一个边沿是上升沿；当 SPO 为 1 时，SPI_CLK 极性是高电压，第一个边沿是下降沿。SPH 设置驱动数据的时钟沿以及采样数据时钟沿的时序，当 SPH 为 0 时 SPI 控制器从 SPI_CLK 的第一个边沿开始采样 SPI_DI 上的数据，从 SPI_CLK 的第二个边沿开始驱动 SPI_DO（SPI_DO 上默认是待发送数据的 MSB）；当 SPH 为 1 时 SPI 控制器从 SPI_CLK 的第一个边沿开始驱动 SPI_DO，从 SPI_CLK 的第二个边沿开始采样 SPI_DI 上的数据。具体通信时序见图7-3和图7-4。

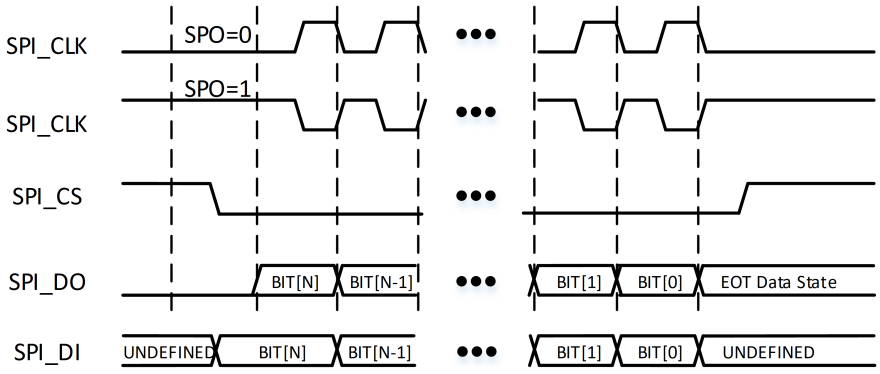

图 7-3: SPH 为 0 时的 SPI 通信

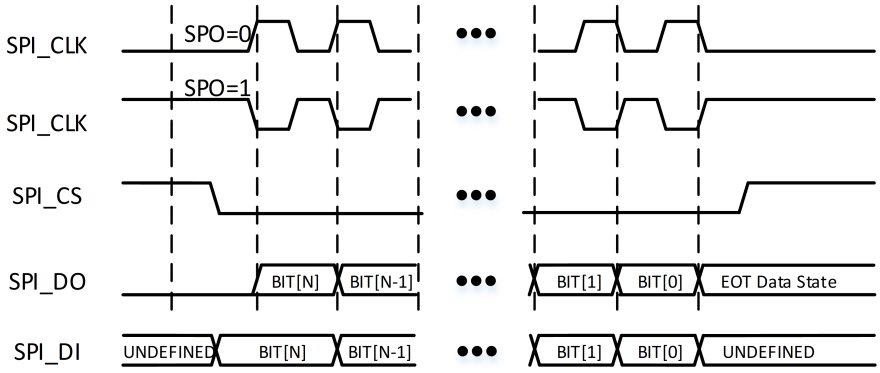

图 7-4: SPH 为 1 时的 SPI 通信

下面结合图7-3以 SPH=0 和 SPO=0 的情况描述 SPI 协议通信过程。当 SPI 控制器没有使能或使能后处于 IDLE 状态时，SPI_DO 处于低电平，SPI_CS 处于高电平，SPI_CLK 处于低电平。SPI_CS 信号拉低开始一次数据传输，并在该帧数据传输完成以前 SPI_CS 一直维持低电平。半个 SPI_CLK 周期后，将该次传输数据的 MSB 驱动到 SPI_DO 上，再过半个 SPI_CLK 周期，SPI_CLK 拉高开始第一个上升沿并采样 SPI_DI。在该次传输所有数据传完之前，SPI_CLK 按设定的频率持续翻转。完成最后一次采样后 SPI_CLK 回归低电平，再过半个 SPI_CLK 周期，SPI_CS 拉高结束本次传输。

在作为 MASTER 通信时，如果 TXFIFO 里有多笔数据待传输，SPI 控制器会通过连续传输将数据传输出去。过程中 SPI_CS 信号维持低电平。传输时序如图7-5。

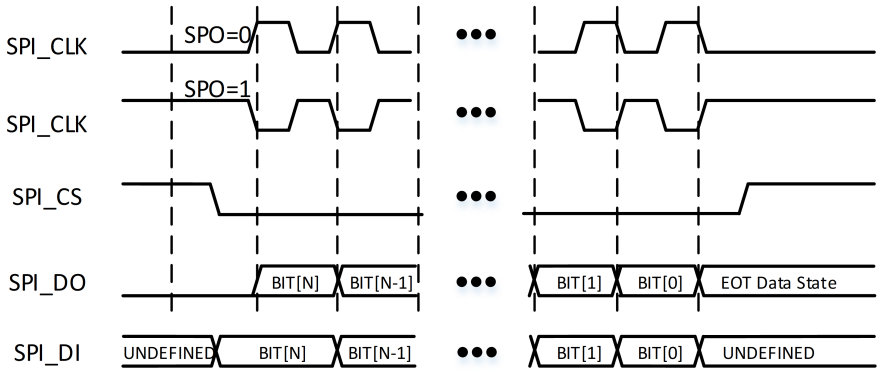

图 7-5: SPI 协议连续传输时序

实际使用中存在需要 SPI_CS 一次拉低传输多笔数据的场景，这种场景下如果 TXFIFO 数据填充不及时，

可能导致传输过程中 SPI_CS 拉高，从而导致通信失败。这种场景下需要通过一些特殊的软件控制来实现 SPI_CS 的稳定拉低，设置细节见后续章节。

- TI-SSP 格式

  TI-SSP 是全双工同步串口通信协议。数据传输时，SPI_CS 发出宽度为一个时钟周期的高脉冲表示开始传输，随后按每个周期一个比特的速率，以 MSB first 的顺序将待发送数据驱动到 SPI_DO 上。数据在 SPI_CLK 的上升沿被驱动到数据线上，在 SPI_CLK 的下降沿被 SPI 控制器采样。单次通信时序如图7-6。

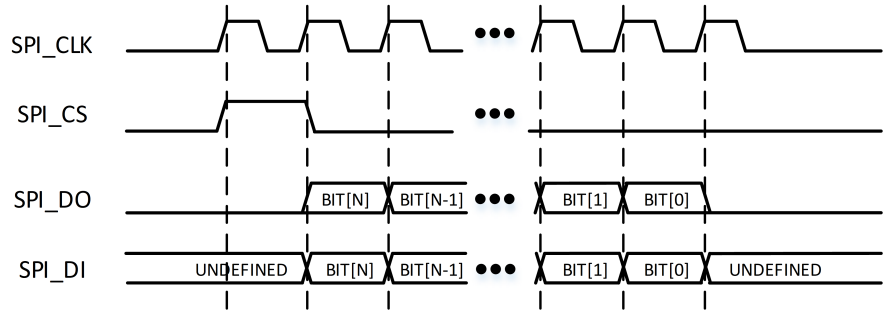

图 7-6: TI-SSP 协议通信时序

在作为 MASTER 通信时，如果 TXFIFO 里有多笔数据待传输，SPI 控制器会通过连续传输将数据传输出去，传输时序如图7-7。

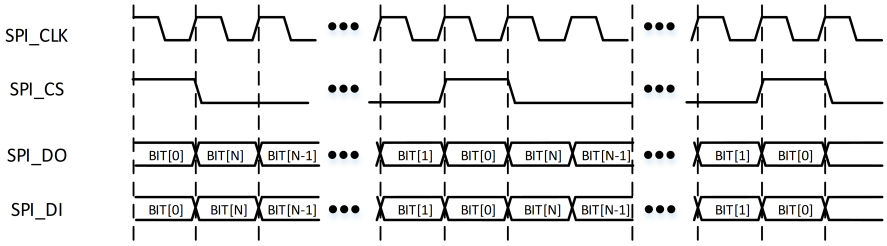

图 7-7: TI-SSP 协议连续通信时序

如果连续传输多笔数据，如果数据 B 紧跟在数据 A 之后，在传输数据 A 的最后一个比特时，SPI_CS 拉高一个周期，并在下一个 SPI_CLK 上升沿开始传输数据 B 的 MSB。

- Microwire 协议

  Microwire 协议是半双工协议。SPI 控制器只支持作为 Master 进行通信。通信中 Master 先在 SPI_DO 上发出 8 或 16bit 的命令字，等一个 SPI_CLK 周期后，Slave 在 SPI_DI 上返回数据。单笔传输的时序如图7-8

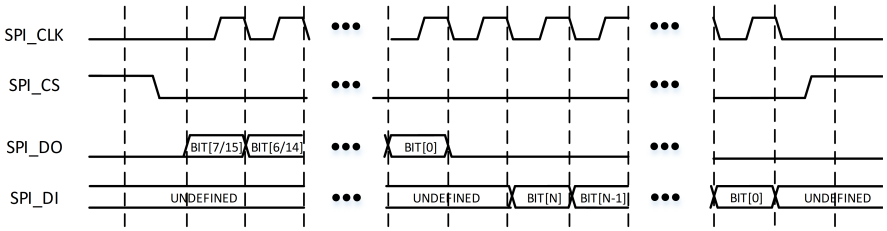

图 7-8: Microwire 协议单次通信时序

当连续多笔传输时，下一笔的命令字在 Slave 返回的最后一个比特结束后立刻被输出到 SPI_DO 上且在所有传输完成前 SPI_CS 一直维持低电平。连续传输的时序如图7-9.

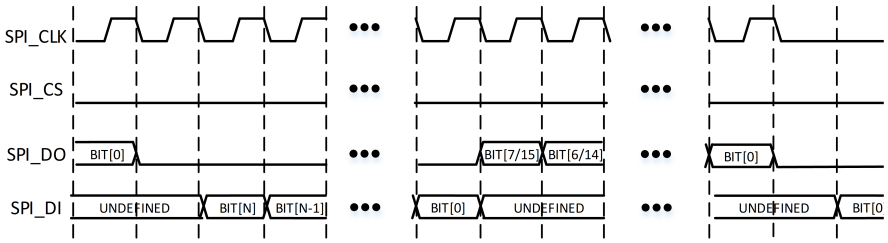

图 7-9: Microwire 协议连续传输时序

7.2.6.1 相关系统资源

SPI 控制器通信需要正确设置 PINMUX。需要配置 PINMUX 的接口有 SPI_CS/SPI_CLK/SPI_DI/SPI_DO。需要注意的是在三线半双工通信时，SPI_DI 和 SPI_DO 配置到同一个 PIN 上，且该 SPI_DO 该 PIN 的功能选为 SPI_DIO。

7.2.6.2 通信过程

进行 SPI 控制器通信需要以下操作。

1. 设置 PINMUX，将对应的 PIN 设置到 SPI 通信功能。
2. 通信协议设置：
   - 通过 TOP_CTRL 寄存器中的 FRF 来配置通信协议。
   - FRF=0：SPI 协议
   - FRF=1：TI-SSP 协议
   - FRF=2：Microwire 协议
3. Master/Slave 模式设置：
   - SPI_CS/SPI_CLK 可以分别配置 Master/Slave 模式。Master 模式即由 SPI 控制器驱动，Slave 模式即 SPI 控制器接收外部驱动的信号。
   - 通过 TOP_CTRL 寄存器中的 SFRMDIR 来配置 SPI_CS 的 Master/Slave 模式：
   - SFRMDIR=0：Master 模式，SFRMDIR=1：Slave 模式
   - 通过 TOP_CTRL 寄存器中的 SCLKDIR 来配置 SPI_CLK 的 Master/Slave 模式：
   - SCLKDIR=0：Master 模式，SCLKDIR=1：Slave 模式
   - 一般情况下，SFRMDIR 和 SCLKDIR 配置为相同的模式。
4. 时钟频率设置：
   - 设置 SPI 时钟的流程是：
     (a) 设置寄存器 CLK_CTRL 中的 CLK_DIV 配置分频时钟分频比
     (b) 设置寄存器 CLK_CTRL 中的 CLK_SEL 选择时钟来源，CLK_SEL=0：选择分频时钟，CLK_SEL=1：选择源时钟。
     (c) 设置寄存器 CLK_CTRL 中的 CLK_SSP_EN 以使能 SPI 时钟，1：使能 SPI 时钟。
   - SPI 的时钟由源时钟及源时钟分频时钟二选一得到。分频时钟的频率为源时钟频率除以 CLK_DIV。源时钟频率在 HPSYS 中为 48MHz，在 LPSYS 中为 24MHz。
5. 数据宽度设置：
   - 支持 8-32bit 的数据宽度，设置寄存器 TOP_CTRL 中的 DSS 可以配置数据位宽，数据位宽 =DSS+1.
6. 操作数据：
   - 数据分为发送数据和接收数据，将待发送的数据写入 TXFIFO，从 RXFIFO 中读取已经收的数据。
   - 数据操作可以通过 CPU 运行软件直接访问 FIFO 来完成，也可以通过 DMA 完成。

- 当用 CPU 操作数据时，一般来说 SPI 控制器会通过中断通知 CPU 来写 TXFIFO 或读 RXFIFO。TXFIFO 对应的中断通过将寄存器中 TIE 设为 1 来使能，使能后当 TXFIFO 中的数据个数小于或等于寄存器中的 TFT 值时，SPI 控制器发出 TX 中断通知 CPU。RXFIFO 对应的中断通过将寄存器中 RIE 设为 1 来使能，使能后当 RXFIFO 中的数据个数大于寄存器中的 RFT 值时，SPI 控制器发出 RX 中断通知 CPU。
- CPU 也可以通过轮询 FIFO 状态来操作 FIFO。FIFO STATUS 寄存器

STATUS 寄存器	意义
TNF	0：TXFIFO 已满；1：TXFIFO 非满。
TFL	TXFIFO 中的数据数。当读到值为 0 时，TXFIFO 时满或空，需结合 TNF 的值来判断。
TUR	1：TXFIFO 发生果 UNDERRUN，即 TXFIFO 为空的状态下 SPI 控制器有过 TXFIFO 读取操作。
RNE	0：RXFIFO 为空；1：RXFIFO 非空。
RFL	RXFIFO 中的数据数。当读到值为 0xF 时，RXFIFO 是空或满，需结合 RNE 的值来判断。
ROR	1：RXFIFO 发生果 OVERRUN，即 RXFIFO 为满的状态下 SPI 控制器有过 RXFIFO 写入操作。

- CPU 通过读 STATUS 寄存器，在 TXFIFO 非满的前提下，可以往 TXFIFO 中添加需要发送的数据；在 RXFIFO 非空的情况下可以从 RXFIFO 中读取收到的数据
- 当使用 DMA 操作数据时，SPI 控制器通过向 DMA 发出请求启动 DMA 来进行数据操作。将 RSRE 写 1 使能 RX 数据的 DMA 功能，在 RX FIFO 中的数据多于 RFT 时，SPI 会发出 DMA 请求。将 TSRE 写 1 使能 TX 数据的 DMA 功能，在 RX FIFO 中的数据多于 RFT 时，SPI 会发出 DMA 请求。

7. 使能 SPI 控制器
   - 将寄存器 TOP_CTRL 中的 SSE 设为 1 以使能 SPI 控制器。
8. 关闭 SPI 控制器
   - 查询 STATUS 寄存器中的 BUSY，若 BUSY 为 0，表示 SPI 控制器当前不在工作，然后将 SSE 写 0，即可关闭 SPI 控制器。
9. SPI_CS 信号控制
   - 在有的通信场景里，需要若干笔数据的传输过程中 SPI_CS 始终为低。默认设置下，如果过程中出现 TXFIFO 为空的情况，可能会导致 SPI_CS 中间拉高，待 TXFIFO 非空后再次拉低。可通过软件参与保证通信过程中 SPI_CS 信号维持稳定低电平。在进行一次通信前将寄存器 TOP_CTRL 中的 HOLD_FRAME_LOW 设置为 1，以确保通信过程中 SPI_CS 维持低电平。注意在该次通信完成后将 HOLD_FRAME_LOW 设为 0，为后续通信做准备。

- 使用时按照以下流程设置 SPI 控制器：
  1. 设置 pinmux
  2. 设置通信协议
  3. 设置时钟频率
  4. 设置数据位宽
  5. 设置主从模式
  6. 使能 SPI 控制器
  7. 访问 FIFO 开始收发
  8. 完成收发，关闭 SPI 控制器

7.2.6.3 Receive-Only 模式

SPI 控制器支持 Receive-Only 模式，该模式下当数据格式是 SPI 或 TI-SSP 时，无论 TXFIFO 中是否有待发送数据，SPI 控制器都将驱动 SPI_CLK 翻转，同时从 SPI_DI 上收到的数据将存入 RXFIFO。Receive-Only 模式的使用设置如下：

- 设置 RWOT_CCM 寄存器，该寄存器值表示需要的 SPI_CLK 周期数。
- 将 RWOT_CTRL 寄存器中的 SET_RWOT_CYCLE 和 RWOT_CYCLE 都设为 1，使能 RWOT 的计数器。
- 将 RWOT_CTRL 寄存器中的 RWOT 设为 1，使能 Receive-Only 模式。

完成以上设置后使能 SPI 控制器则无论 TXFIFO 是否为空，SPI 控制器都将驱动 SPI_CLK 翻转。收到的数据会存入 RXFIFO。

7.2.6.4 三线模式

通过软件辅助 SPI 控制器支持三线模式。三线模式可以实现半双工通信。需要的配置和使用流程如下：

1. 设置 PINMUX，需要通过具有 SPI_DIO 功能的 PIN 进行通信，并将该 PIN 的功能选为 SPI_DIO。
2. 选择 SPI 协议，配置时钟频率，设置数据位宽，设置主从模式。
3. 将 SPI 控制器寄存器 TRIWIRE_CTRL 中的 SPI_TRI_WIRE_EN 设为 1。使能 SPI 控制器。
4. 在发送数据时，将寄存器 TRIWIRE_CTRL 中的 TXD_OEN 设为 0。向 TXFIFO 里写入待发送数据。三线模式下，发送数据时，SPI 控制器不会写 RXFIFO，所以发完数据后，软件无需处理 RXFIFO。
5. 在接收数据时，将寄存器 TRIWIRE_CTRL 中的 TXD_OEN 设为 1。如果 SPI_CLK 是主模式，则需要 SPI 控制器驱动 SPI_CLK。有两种方法驱动 SPI_CLK：
   - 向 TXFIFO 中写入与待接收数据相同数目的数据以驱动 SPI_CLK。
   - 使用 Recerve-Only 模式，流程如下：
     (a) 关闭 SPI 控制器的使能。
     (b) 设置 RWOT_CCM 寄存器，该寄存器值表示需要的 SPI_CLK 周期数。
     (c) 将 RWOT_CTRL 寄存器中的 SET_RWOT_CYCLE 和 RWOT_CYCLE 都设为 1，使能 RWOT 的计数器。
     (d) 将 RWOT_CTRL 寄存器中的 RWOT 设为 1，使能 Receive-Only 模式。
     (e) 完成以上设置后使能 SPI 控制器。
     (f) 从 RXFIFO 读取数据。
6. 完成收发后，关闭 SPI 控制器。

一般来说这种半双工通信模式会要求过程中 SPI_CS 维持稳定低电平。如需维持稳定低电平，请参考 SPI_CS 信号控制设置。

7.2.7 SPI 寄存器

表 7-2: SPI 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00			**TOP_CTRL**	Top Control Register
[31:19]			RSVD	

续表下页...

表 7-2: SPI 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[18]	rw	1'b0	TTELP	TXD Three-state Enable On Last Phase 0 = TXDx is three-stated 1/2 clock cycle after the beginning of the LSB 1 = TXDx output signal is three-stated on the clock edge that ends the LSB
[17]	rw	1'b0	TTE	TXD Three-State Enable 0 = TXDx output signal is not three-stated 1 = TXD is three-stated when not transmitting data
[16]	rw	1'b0	SCFR	Slave Clock Free Running 0 = Clock input to SSPSCLKx is continuously running 1 = Clock input to SSPSCLKx is only active during data transfers.
[15]	rw	1'b0	IFS	Invert Frame Signal 0 = SSPSFRMx polarity is determined by the PSP polarity bits 1 = SSPSFRMx will be inverted from normal-SSPSFRMx (as defined by the PSP polarity bits). (Works in all frame formats: SPI, SSP, and PSP)
[14]	rw	1'b0	HOLD_FRAME_LOW	Hold Frame Low Control 1=After this field is set to 1 and the SSP is operating in master mode, the output frame clock ssp_sfrm_gpio will hold low. Used for SPI and NMW Format Rx FIFO Auto Full Control, which makes the frame clock is still low during there's no bit clock, or the data transfers before the stop clock will be discarded.
[13]	rw	1'b0	TRAIL	Trailing Byte 0 = Trailing bytes are handled by the <var Product Number> 1 = Trailing bytes are handled by DMA bursts
[12]			RSVD	
[11]	rw	1'b0	SPH	Motorola SPI SSPSCLK phase setting 0 = SSPSCLKx is inactive until one cycle after the start of a frame and active until 1/2 cycle before the end of a frame 1 = SSPSCLKx is inactive until 1/2 cycle after the start of a frame and active until one cycle before the end of a frame
[10]	rw	1'b0	SPO	Motorola SPI SSPSCLK Polarity Setting 0 = The inactive or idle state of SSPSCLKx is low 1 = The inactive or idle state of SSPSCLKx is high
[9:5]	rw	5'h0	DSS	SSP Work data size, register bits value 0~31 indicated data size 1~32 bits, usually use data size 8bits, 16bits, 24bits, 32bits
[4]	rw	1'b0	SFRMDIR	SSP Frame (SSPSFRMx) Direction 0 = Master mode, SSPx port drives SSPSFRMx 1 = Slave mode, SSPx port receives SSPSFRMx
[3]	rw	1'b0	SCLKDIR	SSP Serial Bit Rate Clock (SSPSCLKx) Direction 0 = Master mode, SSPx port drives SSPSCLKx 1 = Slave mode, SSPx port receives SSPSCLKx
[2:1]	rw	2'h0	FRF	Frame Format 0x0 = Motorola* Serial Peripheral Interface (SPI) 0x1 = Texas Instruments* Synchronous Serial Protocol (SSP) 0x2 = National Semiconductor Microwire* 0x3 = Programmable Serial Protocol (PSP)
[0]	rw	1'b0	SSE	Synchronous Serial Port Enable 0 = SSPx port is disabled 1 = SSPx port is enabled
0x04			**FIFO_CTRL**	FIFO Control Register
[31:18]			RSVD	

续表下页...

表 7-2: SPI 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[17]	rw	1'h0	RXFIFO_AUTO_FULL_CTRL	Rx FIFO Auto Full Control =1After this field is set to 1 and the SSP is operating in master mode, the SSP FSM returns to IDLE state and stops the ssp_sclk_gpio. When Rx FIFO is full, the SSP FSM continues transferring data after the Rx FIFO is not full. This field is used to avoid an Rx FIFO overrun issue. 1= Enable Rx FIFO auto full control
[16]	rw	1'h0	FPCKE	FIFO Packing Enable 0 = FIFO packing mode disabled 1 = FIFO packing mode enabled
[15:14]	rw	2'h0	TXFIFO_WR_ENDIAN	apb_pwdata Write to Tx FIFO Endian 0x0 = txfifo_wdata[31:0] = apb_pwdata[31:0] 0x1 = fifo_wdata[31:0] = apb_pwdata[15:0], apb_pwdata[31:16] 0x2 = txfifo_wdata[31:0] = apb_pwdata[7:0], apb_pwdata[15:8], apb_pwdata[23:16], apb_pwdata[31:24] 0x3 = txfifo_wdata[31:0] = apb_pwdata[23:16], apb_pwdata[31:24], apb_pwdata[7:0], apb_pwdata[15:8]
[13:12]	rw	2'h0	RXFIFO_RD_ENDIAN	apb_prdata Read from Rx FIFO Endian 0x0 = apb_prdata[31:0] = rxfifo_wdata[31:0] 0x1 = apb_prdata[31:0] = rxfifo_wdata[15:0], rxfifo_wdata[31:16] 0x2 = apb_prdata[31:0]= rxfifo_wdata[7:0], rx-fifo_wdata[15:8], rxfifo_wdata[23:16], rxfifo_wdata[31:24] 0x3 = apb_prdata[31:0]= rxfifo_wdata[23:16], rx-fifo_wdata[31:24], rxfifo_wdata[7:0], rxfifo_wdata[15:8]
[11]	rw	1'h0	RSRE	Receive Service Request Enable 0 = DMA service request is disabled 1 = DMA service request is enabled
[10]	rw	1'h0	TSRE	Transmit Service Request Enable 0 = DMA service request is disabled 1 = DMA service request is enabled
[9:5]	rw	5'h0	RFT	RXFIFO Trigger Threshold This field sets the threshold level at which RXFIFO asserts interrupt. The level should be set to the preferred threshold value minus 1.
[4:0]	rw	5'h0	TFT	TXFIFO Trigger Threshold This field sets the threshold level at which TXFIFO asserts interrupt. The level should be set to the preferred threshold value minus 1.
0x08			**INTE**	Interrupt Enable Register
[31:7]			RSVD	
[6]	rw	1'h0	EBCEI	Enable Bit Count Error Interrupt 0 = Interrupt due to a bit count error is disabled 1 = Interrupt due to a bit count error is enabled
[5]	rw	1'h0	TIM	Transmit FIFO Underrun Interrupt Mask 0 = TUR events generate an SSP interrupt 1 = TUR events do NOT generate an SSP interrupt
[4]	rw	1'h0	RIM	Receive FIFO Overrun Interrupt Mask 0 = ROR events generate an SSP interrupt 1 = ROR events do NOT generate an SSP interrupt
[3]	rw	1'h0	TIE	Transmit FIFO Interrupt Enable 0 = TXFIFO threshold-level-reached interrupt is disabled 1 = TXFIFO threshold-level-reached interrupt is enabled
[2]	rw	1'h0	RIE	Receive FIFO Interrupt Enable 0 = RXFIFO threshold-level-reached interrupt is disabled 1 = RXFIFO threshold-level-reached interrupt is enabled

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表 7-2: SPI 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[1]	rw	1'h0	TINTE	Receiver Time-out Interrupt Enable 0 = Receiver time-out interrupt is disabled 1 = Receiver time-out interrupt is enabled
[0]	rw	1'h0	PINTE	Peripheral Trailing Byte Interrupt Enable 0 = Peripheral trailing byte interrupt is disabled 1 = Peripheral trailing byte interrupt is enabled
0x0C			**TO**	SPI Time Out Register
[31:24]			RSVD	
[23:0]	r	24'h0	TIMEOUT	Timeout Value TIMEOUT value is the value (0 to 2<super 24>-1) that defines the time-out interval. The time-out interval is given by the equation shown in the TIMEOUT Interval Equation.
0x10			**DATA**	SPI DATA Register
[31:0]	rw	32'h0	DATA	DATA This field is used for data to be written to the TXFIFO read from the RXFIFO.
0x14			**STATUS**	Status Register
[31:24]			RSVD	
[23]	r	1'h0	OSS	Odd Sample Status 0 = RxFIFO entry has two samples 1 = RxFIFO entry has one sample Note that this bit needs to be looked at only when FIFO Packing is enabled (<FIFO Packing Enable> field in SSP FIFO Control Register is set). Otherwise, this bit is zero. When SSPx port is in Packed mode and the CPU is used instead of DMA to read the RxFIFO, the CPU should make sure that <Receive FIFO Not Empty> = 1 AND this field = 0 before it attempts to read the RxFIFO.
[22]	r	1'h0	TX_OSS	TX FIFO Odd Sample Status When SSPx port is in packed mode, the number of samples in the TX FIFO is: (<Transmit FIFO Level>*2 + this field), when <Transmit FIFO Not Full> = 1 32, when <Transmit FIFO Not Full> = 0. The TX FIFO cannot accept new data when <Transmit FIFO Not Full> = 1 and <Transmit FIFO Level> = 15 and this field = 1. (The TX FIFO has 31 samples). 0 = TxFIFO entry has an even number of samples 1 = TxFIFO entry has an odd number of samples Note that this bit needs to be read only when FIFO Packing is enabled (<FIFO Packing Enable> in the SSP FIFO Control Register is set). Otherwise, this bit is zero.
[21]	w1c	1'h0	BCE	Bit Count Error 0 = The SSPx port has not experienced a bit count error 1 = The SSPSFRMx signal was asserted when the bit counter was not zero
[20]	w1c	1'h0	ROR	Receive FIFO Overrun 0 = RXFIFO has not experienced an overrun 1 = Attempted data write to full RXFIFO, causes an interrupt request
[19]			RSVD	
[18:15]	r	4'h0	RFL	Receive FIFO Level This field is the number of entries minus one in RXFIFO. When the value 0x1F is read, the RXFIFO is either empty or full, and software should read the <Receive FIFO Not Empty> field.
[14]	r	1'h0	RNE	Receive FIFO Not Empty 0 = RXFIFO is empty 1 = RXFIFO is not empty

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表 7-2: SPI 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[13]	r	1'h0	RFS	Receive FIFO Service Request 0 = RXFIFO level is at or below RFT threshold (RFT) or SSPx port is disabled 1 = RXFIFO level exceeds RFT threshold (RFT), causes an interrupt request
[12]	w1c	1'h0	TUR	Transmit FIFO Underrun 0 = The TXFIFO has not experienced an underrun 1 = A read from the TXFIFO was attempted when the TXFIFO was empty, causes an interrupt if it is enabled (<Transmit FIFO Underrun Interrupt Mask> in the SSP INT EN Register is 0)
[11]			RSVD	
[10:7]	r	4'h0	TFL	Transmit FIFO Level This field is the number of entries in TXFIFO.When the value 0x0 is read, the TXFIFO is either empty or full, and software should read the <Transmit FIFO Not Full> field.
[6]	r	1'h0	TNF	Transmit FIFO Not Full 0 = TXFIFO is full 1 = TXFIFO is not full
[5]	r	1'h0	TFS	Transmit FIFO Service Request 0 = TX FIFO level exceeds the TFT threshold (TFT + 1) or SSPx port disabled 1 = TXFIFO level is at or below TFT threshold (TFT + 1), causes an interrupt request
[4]	w1c	1'h0	EOC	End Of Chain 0 = DMA has not signaled an end of chain condition 1 = DMA has signaled an end of chain condition
[3]	w1c	1'h0	TINT	Receiver Time-out Interrupt 0 = No receiver time-out is pending 1 = Receiver time-out pending, causes an interrupt request
[2]	w1c	1'h0	PINT	Peripheral Trailing Byte Interrupt 0 = No peripheral trailing byte interrupt is pending 1 = Peripheral trailing byte interrupt is pending
[1]	r	1'h0	CSS	Clock Synchronization Status 0 = The SSPx port is ready for slave clock operations 1 = The SSPx port is currently busy synchronizing slave mode signals
[0]	r	1'h0	BSY	SSP Busy 0 = SSPx port is idle or disabled 1 = SSPx port is currently transmitting or receiving framed data
0x24			**RWOT_CTRL**	SSP RWOT Control Register
[31:5]			RSVD	
[4]	rw	1'h0	MASK_RWOT_LAST_SAMPLE	Mask last_sample_flag in RWOT Mode 1= Mask 0 = Unmask
[3]	rw	1'h0	CLR_RWOT_CYCLE	Clear SSP Internal rwot_counter This field clears the rwot_counter to 0. This field is self cleared by SSP after SSE = 1. 1 = Clear rwot_counter
[2]	rw	1'h0	SET_RWOT_CYCLE	Set RWOT Cycle This field is used to set the value of the SSP_RWOT_CCM register to the SSP internal rwot_counter. This field is self-cleared by SSP after SSE = 1. 1 = Set rwot_counter
[1]	rw	1'h0	CYCLE_RWOT_EN	Enable SSP RWOT Cycle Counter Mode 1 = Enable
[0]	rw	1'h0	RWOT	Receive Without Transmit 0 = Transmit/receive mode 1 = Receive without transmit mode
0x28			**RWOT_CCM**	SSP RWOT Counter Cycles Match Register

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表 7-2: SPI 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:0]	rw	32'h0	SSPRWOTCCM	It's just total ssp_sclk_gpio Cycles The value of this register defines the total number of ssp_sclk_gpio cycles when SSP works in master and RWOT mode. When the rwot_counter matches this value, SSP returns to IDLE state and does not output ssp_sclk_gpio anymore.
0x2C			**RWOT_CVWRn**	SSP RWOT Counter Value Write for Red Request Register
[31:0]	rw	32'h0	SSPRWOTCVWR	SSPRWOTCVWR This register prevents the risk of instability on rwot_counter value reading, it's only valid after SSP has been enabled Write 0 = No effect Write 1 = Capture value of rwot_counter Read: Returns the captured value of rwot_counter
0x3C			**CLK_CTRL**	SSP CLK Control Register
[31:9]			RSVD	
[8]	rw	1'h0	CLK_SSP_EN	
[7]	rw	1'h0	CLK_SEL	0: select clk_div as clk_ssp 1: select clk_sys as clk_ssp
[6:0]	rw	7'h0	CLK_DIV	div ratio from clk_sys
0x54			**TRIWIRE_CTRL**	SSP Three Wire Mode Control Register
[31:3]			RSVD	
[2]	rw	1'h0	SSP_WORK_WIDTH_DYN_CHANGE	SSP_WORK_WIDTH_DYN_CHNAGE 1=SP can dynamicly change SSP_TOP_CTRL[9:5] without disabling SSP_TOP_CTRL[0] and re-enabling SSP_TOP_CTRL[0]
[1]	rw	1'h0	TXD_OEN	TXD_OEN 1=TXD is input 0=TXD is output
[0]	rw	1'h0	SPI_TRI_WIRE_EN	SPI_THREE_WIRE_MODE_EN 1=enable

7.3 UART

芯片共有 6 个 USART，其中 USART 1，USART2 和 USART3 位于 HPSYS，输入输出连接至 IO(PA)，可向 DMAC1 发送请求；USART4，USART5 和 USART 6 位于 LPSYS，输入输出连接至 IO(PB)，可向 DMAC2 发送请求。

通用异步收发器支持全双工模式，提供高达 6Mbps 的波特率和多种可配置的数据格式，为与外部标准化设备通信提供了灵活而有效的数据交互手段。同时它还支持 DMA，实现多包收发。

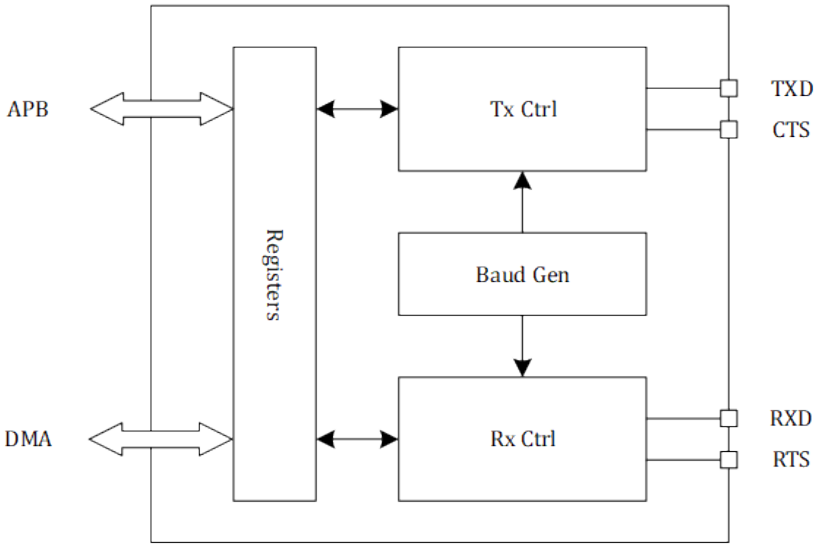

图 7-10: 通用异步收发器

通用异步收发器主要特性：

- 全双工异步通信
- 可配置 16 倍过采样或 8 倍过采样，选择频率优先或者时钟容忍度优先
- 灵活波特率配置，当输入时钟为 48MHz 且过采样率为 16 时，波特率为 3Mbps
- 可配置包长度（7/8/9 bits）
- 可配置停止位（1/2 bits）
- 硬件流控（CTS/RTS）
- DMA 多包发送和接收
- 接收奇偶校验和发送奇偶生成
- 接收和发送中断，以及其他错误中断

波特率计算说明

假设输入时钟固定为 48MHz，波特率计算公式如下：

$$Baud\ Rate = \frac{48MHz}{(BRR_{INT} + \frac{BRR_{FRAC}}{16})(16\ or\ 8)}$$

7.3.1 USART 寄存器

表 7-3: UART 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00			**CR1**	Control Register 1
[31:29]			RSVD	

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表 7-3: USART 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[28:27]	rw	2'h0	M	Mode bit indicates the length of the packet, including data bits and parity. Stop bits not included. 0: 6 bits (e.g. 6 data bits + no parity bit) 1: 7 bits (e.g. 6 data bits + 1 parity bit) 2: 8 bits (e.g. 7 data bits + 1 parity bit, or 6 data bits + 2 parity bits) 3: 9 bits (e.g. 8 data bits + 1 parity bit, or 7 data bits + 2 parity bits)
[26]			RSVD	
[25]			RSVD	
[24:20]			RSVD	
[19:15]			RSVD	
[14]	rw	1'h0	OVER8	Oversampling mode 0: Oversampling by 16 1: Oversampling by 8
[13]			RSVD	
[12]			RSVD	
[11]			RSVD	
[10]	rw	1'h0	PCE	Parity check enable. If enabled, parity bit is inserted at the MSB position 0: parity check disabled 1: parity check enabled
[9]	rw	1'h0	PS	Parity select 0: even parity 1: odd parity
[8]	rw	1'h0	PEIE	Parity error interrupt enable 0: interrupt disabled 1: interrupt is generated whenever PE=1 in the ISR register
[7]	rw	1'h0	TXEIE	Tx empty interrupt enable 0: interrupt disabled 1: interrupt is generated whenver TXE=1 in the ISR register
[6]	rw	1'h0	TCIE	Transfer compelete interrupt enable 0: interrupt disabled 1: interrupt is generated whenever TC=1 in the ISR register
[5]	rw	1'h0	RXNEIE	Rx not empty interrupt enable 0: interrupt disabled 1: interrupt is generated whenever RXNE=1 in the ISR register
[4]	rw	1'h0	IDLEIE	Idle line interrupt enable 0: interrupt disabled 1: interrupt is generated whenever IDLE=1 in the ISR register
[3]	rw	1'h0	TE	Transmitter enable 0: transmitter is disabled 1: transmitter is enabled
[2]	rw	1'h0	RE	Receiver enable 0: receiver is disabled 1: receiver is enabled
[1]			RSVD	
[0]	rw	1'h0	UE	USART enable 0: disabled 1: enabled
0x04			**CR2**	Control Register 2
[31:24]			RSVD	

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表 7-3: USART 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[23]			RSVD	
[22:21]			RSVD	
[20]			RSVD	
[19]			RSVD	
[18]			RSVD	
[17]			RSVD	
[16]			RSVD	
[15]			RSVD	
[14]			RSVD	
[13:12]	rw	2'h0	STOP	Stop bits 0/1: 1 stop bit 2/3: 2 stop bits
[11]			RSVD	
[10]			RSVD	
[9]			RSVD	
[8]			RSVD	
[7]			RSVD	
[6]			RSVD	
[5]			RSVD	
[4]			RSVD	
[3:0]			RSVD	
0x08			**CR3**	Control Register 3
[31:25]			RSVD	
[24]			RSVD	
[23]			RSVD	
[22]			RSVD	
[21:20]			RSVD	
[19:17]			RSVD	
[16]			RSVD	
[15]			RSVD	
[14]			RSVD	
[13]			RSVD	
[12]	rw	1'h0	OVRDIS	Overrun disable 0: overrun error flag (ORE) will be set if new data received but previous data not read. New data will not overwrite the content in RDR register. 1: overrun disabled. If new data is received before previous data is read, the new data will overwrite the content in RDR register and ORE flag remains unset.
[11]	rw	1'h0	ONEBIT	One bit sampling mode 0: 3-bit sampling mode, the sampling value is determined by the voted result out of 3 bits 1: 1-bit sampling mode
[10]	rw	1'h0	CTSIE	CTS interrupt enable 0: interrupt disabled 1: interrupt is generated whenever CTSIF=1 in the ISR register
[9]	rw	1'h0	CTSE	CTS enable 0: CTS hardware flow control disabled 1: CTS hardware flow control enabled, data is transmitted only when CTS input is asserted low

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表 7-3: USART 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[8]	rw	1'h0	RTSE	RTS enable 0: RTS hardware flow control disabled 1: RTS hardware flow control enabled, RTS output is asserted low when new data can be received
[7]	rw	1'h0	DMAT	Transmitter DMA enable 0: DMA mode disabled for transmission 1: DMA mode enabled for transmission
[6]	rw	1'h0	DMAR	Receiver DMA enable 0: DMA mode disabled for reception 1: DMA mode enabled for reception
[5]			RSVD	
[4]			RSVD	
[3]			RSVD	
[2]			RSVD	
[1]			RSVD	
[0]	rw	1'h0	EIE	Error interrupt enable 0: interrupt disabled 1: interrupt is generated whenever FE=1 or ORE=1 or NF=1 in the ISR register
0x0C			**BRR**	Baud Rate Register
[31:16]			RSVD	
[15:4]	rw	12'h3	INT	Integer part of baud rate prescaler If OVER8 = 0, Baud Rate = 48000000 / (INT + FRAC/16) / 16 If OVER8 = 1, Baud Rate = 48000000 / (INT + FRAC/16) / 8 For example: OVER=0, INT=3, FRAC=0, Baud Rate = 48000000/(3+0)/16 = 1Mbps OVER=0, INT=3, FRAC=4, Baud Rate = 48000000/(3+4/16)/16 = 923077 = 921600 + 1.6‰ OVER=1, INT=52, FRAC=1, Baud Rate = 48000000/(52+1/16)/8 = 115246 = 115200 + 0.4‰
[3:0]	rw	4'h0	FRAC	Fractional part of baud rate prescaler
0x18			**RQR**	Request Register
[31:5]			RSVD	
[4]	w	1'h0	TXFRQ	Tx data flush request Reserved-Do not modify
[3]	w	1'h0	RXFRQ	Rx data flush request. Write 1 to clear the RXNE flag and discard the current data in RDR
[2]			RSVD	
[1]			RSVD	
[0]			RSVD	
0x1C			**ISR**	Interrupt and Status Register
[31:26]			RSVD	
[25]			RSVD	
[24:23]			RSVD	
[22]			RSVD	
[21]			RSVD	
[20]			RSVD	
[19]			RSVD	
[18]			RSVD	
[17]			RSVD	

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表 7-3: USART 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[16]			RSVD	
[15]			RSVD	
[14]			RSVD	
[13]			RSVD	
[12]			RSVD	
[11]			RSVD	
[10]	r	1'h0	CTS	CTS input. Read this bit to get the raw status of the CTS line.
[9]	r	1'h0	CTSIF	CTS interrupt flag. This bit is set by hardware whenever CTS input toggles. 0: no change on the CTS line 1: there is a change on the CTS line
[8]			RSVD	
[7]	r	1'h1	TXE	Tx data empty 0: data is ready in TDR 1: data is already transferred to shift register, i.e. transmission is in progress or complete
[6]	r	1'h1	TC	transmission complete. This bit is set by hardware if the transmission is complete 0: transmission is not complete 1: transmission is complete
[5]	r	1'h0	RXNE	Rx data not empty. This bit is set by hardware when the received data is transferred into RDR register. 0: data is not received 1: data is ready in RDR to be read
[4]	r	1'h0	IDLE	Idle line detected 0: no idle line is detected 1: idle line is detected
[3]	r	1'h0	ORE	Overrun error. When new data is received but Rx buffer is not empty (i.e. previous data is not read yet), ORE is asserted and current RDR content is not lost. This feature can be disabled by set CR3_OVRDIS to 1. 0: no overrun error 1: overrun error is detected
[2]	r	1'h0	NF	Noise flag. Noise means the samping values in the 3-bit sampling mode are not the same. 0: no noise is detected 1: noise is detected
[1]	r	1'h0	FE	Framing error. This bit is set by hardware when stop bit is not correctly received 0: no framing error is detected 1: framing error is detected
[0]	r	1'h0	PE	Parity error. This bit is set when a parity error is detected in the received packet. 0: no parity error 1: parity error detected
0x20			**ICR**	Interrupt flag Clear Register
[31:21]			RSVD	
[20]			RSVD	
[19:18]			RSVD	
[17]			RSVD	
[16:13]			RSVD	
[12]			RSVD	
[11]			RSVD	
[10]			RSVD	

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表 7-3: USART 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[9]	w1c	1'h0	CTSCF	CTS clear flag. Writing 1 to this bit clears the CTSIF flag in the ISR register.
[8]			RSVD	
[7]			RSVD	
[6]	w1c	1'h0	TCCF	Transmission complete clear flag. Writing 1 to this bit clears the TC flag in the ISR register.
[5]			RSVD	
[4]	w1c	1'h0	IDLECF	Idle line detected clear flag. Writing 1 to this bit clears the IDLECF flag in the ISR register.
[3]	w1c	1'h0	ORECF	Overrun error clear flag. Writing 1 to this bit clears the ORE flag in the ISR register.
[2]	w1c	1'h0	NCF	Noise detected clear flag. Writing 1 to this bit clears the NF flag in the ISR register.
[1]	w1c	1'h0	FECF	Framing error clear flag. Writing 1 to this bit clears the FE flag in the ISR register.
[0]	w1c	1'h0	PECF	Parity error clear flag. Wriring 1 to this bit clears the PE flag in the ISR register.
0x24			**RDR**	Receive Data Register
[31:9]			RSVD	
[8:0]	r	9'h0	RDR	Received data
0x28			**TDR**	Transmit Data Register
[31:9]			RSVD	
[8:0]	rw	9'h0	TDR	Transmit data
0x2C			**MISCR**	Miscellaneous Register
[31]	rw	1'h0	AUTOCAL	
[30:8]			RSVD	
[7:4]	rw	4'h2	RTSBIT	assert RTS ahead of the frame completion (in number of bits) Reserved-Do not modify
[3:0]	rw	4'h6	SMPLINI	initial sample count, count down from this value to zero to reach the middle of the start bit in Rx Reserved-Do not modify
0x30			**DRDR**	Debug Receive Data Register
[31:0]	r	32'h0	DATA	DbgUART is still a preliminary version in this project.
0x34			**DTDR**	Debug Receive Data Register
[31:0]	rw	32'h0	DATA	
0x38			**EXR**	Mutual Exclusive Register
[31:5]			RSVD	
[4]	r	1'b0	ID	
[3:1]			RSVD	
[0]	rw	1'h1	BUSY	

7.4 PTC

芯片共有 2 个 PTC，其中 PTC1 位于 HPSYS，PTC2 位于 LPSYS。

7.4.1 简介

PTC (Peripheral Task Controller) 是一个独立的外设控制器，可以不需要唤醒 CPU，自动完成各个外设的相互调度和控制任务。基于选定外设的事件触发，PTC 能够自动改写各外设的工作模式或工作状态，并且能够将这些任务串联构成自动触发的任务序列，从而完成复杂且快速响应的任务链。在任务链的进行过程中，CPU 可以一直保持睡眠，进而有效节省功耗。

PTC 共有 8 个通道，每个通道可以选择独立的触发源，并可配置独立的任务。可执行的任务包括两类：将指定数据直接写入指定地址；将指定地址的内容读出，与指定数据进行异或/与/或/加法操作后再写回。每个通道任务完成时，可产生触发信号从而触发其它通道的任务。每个通道可配置触发次数。部分通道支持触发后经过可配置的延时再执行任务。

7.4.2 主要特性

- 8 个独立配置的通道可同时工作
- 每个通道触发可在 128 个触发源中选择，包括 PTC 自身的触发源
- 可访问 AHB 和 APB 外设地址空间，只支持 word 对齐访问
- 支持直接写数据，或读后改写
- 支持 32 位异或/与/或/加法运算
- 可配置触发次数 1~1023，或无限次触发
- 可配置触发延迟 0~65535 个 HCLK 周期
- 固定优先级仲裁，通道编号越小优先级越高
- 4 个 word 的寄存器空间用于数据缓存

7.4.3 功能描述

7.4.3.1 通道触发

每个通道可以在 128 个触发源中选择 1 个作为触发，选择寄存器为 TCRx_TRIGSEL。触发源通常由各个外设产生，用于表示外设的特定事件发生，比如 DMA 传输结束，IO 翻转，定时器更新等，也包含了 PTC 自己的通道完成事件。触发源的极性可以通过 TCRx_TRIGPOL 选择。触发源选择 IO 输入信号时，每 32 个 IO 中仅能同时选出 4 个作为触发源，具体选择通过 PTC 的 GPIO31_0,GPIO63_32 等寄存器。IO 触发源不支持防抖动。

通道也可由 CPU 配置 TCRx_SWTRIG 寄存器直接触发。当 TCRx_TRIGSEL 为 0 时，通道仅能通过 TCRx_SWTRIG 寄存器触发。

表 7-4: PTC1 触发源

TRIGSEL	PTC1 trigger source								TRIGSEL
127	PTC1_CH8	PTC1_CH7	PTC1_CH6	PTC1_CH5	PTC1_CH4	PTC1_CH3	PTC1_CH2	PTC1_CH1	120
119	USB_RX	USB_TX	I2S1_OF	I2S1_UF	/	TRNG_RANDGEN	TRNG_SEEDGEN	HCPU_SLEEPDEEP	112
111	EPIC_LINEHIT	EPIC_DONE	NNACC1_DONE	LCDC1_ERR	LCDC1_LINE	LCDC1_LINEHIT	LCDC1_FMARK	LCDC1_DONE	104
103	LCDC1_BUSY	/	EZIP1_ROW	EZIP1_DONE	USART3_TXBYTE	USART3_RXBYTE	EXTDMA_HT	EXTDMA_TC	96
95	/	/	/	/	USART2_TXBYTE	USART2_RXBYTE	USART1_TXBYTE	USART1_RXBYTE	88
87	SDMMC2_DATIDLE	SDMMC2_CMDBUSY	SDMMC1_TC	SDMMC1_CC	SPI2_START	SPI2_DONE	SPI1_START	SPI1_DONE	80
79	I2C3_RF	I2C3_TE	I2C3_DMADONE	FACC1_DONE	I2C2_RF	I2C2_TE	I2C2_DMADONE	AES_DONE	72
71	I2C1_RF	I2C1_TE	I2C1_DMADONE	FFT1_DONE	PA95_64_D	PA95_64_C	PA95_64_B	PA95_64_A	64
63	PA63_32_D	PA63_32_C	PA63_32_B	PA63_32_A	PA31_0_D	PA31_0_C	PA31_0_B	PA31_0_A	56
55	MAILBOX1_C4INT7	MAILBOX1_C3INT7	MAILBOX1_C2INT7	MAILBOX1_C1INT7	/	/	/	/	48
47	BUSMON1_OF8	BUSMON1_OF7	BUSMON1_OF6	BUSMON1_OF5	BUSMON1_OF4	BUSMON1_OF3	BUSMON1_OF2	BUSMON1_OF1	40
39	DMAC1_HT8	DMAC1_HT7	DMAC1_HT6	DMAC1_HT5	DMAC1_HT4	DMAC1_HT3	DMAC1_HT2	DMAC1_HT1	32
31	DMAC1_TC8	DMAC1_TC7	DMAC1_TC6	DMAC1_TC5	DMAC1_TC4	DMAC1_TC3	DMAC1_TC2	DMAC1_TC1	24
23	/	ATIM1_COM	ATIM1_CH4	ATIM1_CH3	ATIM1_CH2	ATIM1_CH1	ATIM1_TRIG	ATIM1_UPDATE	16
15	BTIM2_UPDATE	BTIM1_UPDATE	GPTIM2_CH4	GPTIM2_CH3	GPTIM2_CH2	GPTIM2_CH1	GPTIM2_TRIG	GPTIM2_UPDATE	8
7	GPTIM1_CH4	GPTIM1_CH3	GPTIM1_CH2	GPTIM1_CH1	GPTIM1_TRIG	GPTIM1_UPDATE	HCPU_SLEEPING	0	0

表 7-5: PTC2 触发源

TRIGSEL	PTC1 trigger source								TRIGSEL
127	PTC2_CH8	PTC2_CH7	PTC2_CH6	PTC2_CH5	PTC2_CH4	PTC2_CH3	PTC2_CH2	PTC2_CH1	120
119	LPCOMP2_SENS	LPCOMP1_SENS	/	TSEN_DONE	/	/	RF_UNLOCK	RF_PKTDET	112
111	BT_EDRSYNC	BT_RCCALDONE	BT_ISOSYNC	BT_SLPSTATUS	BT_FRAME	BT_BLEEVENT	BT_PKTDET	BT_CRCERR	104
103	BT_RXDONE	BT_PHYRX	BT_RFRX	BT_TXDONE	BT_PHYTX	BT_RFTX	BT_KICKOFF	BT_INPROCESS	96
95	/	/	USART6_TXBYTE	USART6_RXBYTE	USART5_TXBYTE	USART5_RXBYTE	USART4_TXBYTE	USART4_RXBYTE	88
87	BT_MODE	BT_COLLISION	BT_PRIORITY	BT_ACTIVE	SPI4_START	SPI4_DONE	SPI3_START	SPI3_DONE	80
79	I2C7_RF	I2C7_TE	I2C7_DMADONE	/	I2C6_RF	I2C6_TE	I2C6_DMADONE	/	72
71	I2C5_RF	I2C5_TE	I2C5_DMADONE	/	/	/	/	/	64
63	PB63_32_D	PB63_32_C	PB63_32_B	PB63_32_A	PB31_0_D	PB31_0_C	PB31_0_B	PB31_0_A	56
55	MAILBOX2_C2INT7	MAILBOX2_C2INT6	MAILBOX2_C2INT5	MAILBOX2_C2INT4	MAILBOX2_C1INT7	MAILBOX2_C1INT6	MAILBOX2_C1INT5	MAILBOX2_C1INT4	48
47	BT_EDR3	BT_EDR2	BT_BRLASTBIT	BT_EDRLASTBIT	BUSMON2_OF4	BUSMON2_OF3	BUSMON2_OF2	BUSMON2_OF1	40
39	DMAC2_HT8	DMAC2_HT7	DMAC2_HT6	DMAC2_HT5	DMAC2_HT4	DMAC2_HT3	DMAC2_HT2	DMAC2_HT1	32
31	DMAC2_TC8	DMAC2_TC7	DMAC2_TC6	DMAC2_TC5	DMAC2_TC4	DMAC2_TC3	DMAC2_TC2	DMAC2_TC1	24
23	LCPU_SLEEPDEEP	LCPU_SLEEPING	GPTIM5_CH4	GPTIM5_CH3	GPTIM5_CH2	GPTIM5_CH1	GPTIM5_TRIG	GPTIM5_UPDATE	16
15	BTIM4_UPDATE	BTIM3_UPDATE	GPTIM4_CH4	GPTIM4_CH3	GPTIM4_CH2	GPTIM4_CH1	GPTIM4_TRIG	GPTIM4_UPDATE	8
7	GPTIM3_CH4	GPTIM3_CH3	GPTIM3_CH2	GPTIM3_CH1	GPTIM3_TRIG	GPTIM3_UPDATE	/	0	0

7.4.3.2 通道任务

通道可执行的任务包括两类，通过 TCRx_OP 配置。当 TCRx_OP 为 0 时，通道触发以后，会将 TDRx 寄存器中的数据内容直接写入 TARx 寄存器指向的地址。当 TCRx_OP 为 0x4~0x7 时，通道触发以后会首先将 TARx 寄存器指向的地址的数据读出，与 TDRx 寄存器中的数据进行异或/与/或/加法运算后再写回 TARx 寄存器指向的地址。TARx 寄存器通常指向外设的寄存器地址，因此通道任务的通常目的是当触发源的特定事件发生后，对外设进行自动配置，从而改变外设的工作模式或工作状态。

默认情况下，TCRx_REPEN 为 0，通道可无限次被触发执行任务。当 TCRx_REPEN 为 1 时，可以通过 RCRx_REP 寄存器指定通道执行任务的次数，最大为 1023 次。当 RCRx_REP 大于 0 时，通道每产生一次触发，就执行一次任务，并将 RCRx_REP 减 1；直到 RCRx_REP 减到 0 以后，即使触发条件产生，也不会开启任务执行。

通道对 TARx 寄存器指向的地址进行写入操作后，会产生通道完成事件，可作为另一个通道的 PTC 触发源，同时产生 ISR_TCIFx 标志，并当 IER_TCIEx 为 1 时产生中断。当 TCRx_REPIRQ 为 1 时，仅当 RCRx_REP 指定次数任务全部完成后才产生中断，否则每次任务完成后都产生中断。当 TCRx_REPTRIG 为 1 时，仅当 RCRx_REP 指定次数任务全部完成后才产生通道完成的 PTC 触发，否则每次任务完成后都产生 PTC 触发。

如果 TARx 寄存器指向的地址是 PTC 无法访问的总线地址，通道在访问时会产生总线错误，可产生 ISR_TEIFx 标志，并当 IER_TEIE 为 1 时产生中断。

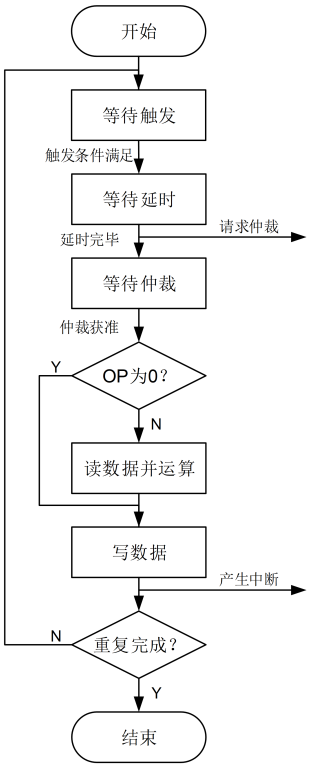

图 7-11: PTC 通道执行流程图

7.4.3.3 通道仲裁

PTC 共有 8 个通道，依照通道编号越小优先级越高的原则进行仲裁。每个通道被触发后进入仲裁。当多个通道同时进入仲裁时，编号最小的通道首先被获准启动任务执行，其余通道处于悬挂状态，直到编号最小的通道任务执行完毕后，再重新进行仲裁。

7.4.4 PTC 寄存器

表 7-6: PTC 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00			**ISR**	interrupt status register
[31:24]			RSVD	
[23]	r	1'h0	TEIF8	transfer error flag for task 8
[22]	r	1'h0	TEIF7	transfer error flag for task 7
[21]	r	1'h0	TEIF6	transfer error flag for task 6
[20]	r	1'h0	TEIF5	transfer error flag for task 5
[19]	r	1'h0	TEIF4	transfer error flag for task 4
[18]	r	1'h0	TEIF3	transfer error flag for task 3
[17]	r	1'h0	TEIF2	transfer error flag for task 2
[16]	r	1'h0	TEIF1	transfer error flag for task 1
[15:8]			RSVD	
[7]	r	1'h0	TCIF8	task complete interrupt flag for task 8
[6]	r	1'h0	TCIF7	task complete interrupt flag for task 7
[5]	r	1'h0	TCIF6	task complete interrupt flag for task 6

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表 7-6: PTC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[4]	r	1'h0	TCIF5	task complete interrupt flag for task 5
[3]	r	1'h0	TCIF4	task complete interrupt flag for task 4
[2]	r	1'h0	TCIF3	task complete interrupt flag for task 3
[1]	r	1'h0	TCIF2	task complete interrupt flag for task 2
[0]	r	1'h0	TCIF1	task complete interrupt flag for task 1
0x04			**ICR**	interrupt clear register
[31:17]			RSVD	
[16]	w1s	1'h0	CTEIF	clear transfer error flag
[15:8]			RSVD	
[7]	w1s	1'h0	CTCIF8	clear task complete interrupt flag for task 8
[6]	w1s	1'h0	CTCIF7	clear task complete interrupt flag for task 7
[5]	w1s	1'h0	CTCIF6	clear task complete interrupt flag for task 6
[4]	w1s	1'h0	CTCIF5	clear task complete interrupt flag for task 5
[3]	w1s	1'h0	CTCIF4	clear task complete interrupt flag for task 4
[2]	w1s	1'h0	CTCIF3	clear task complete interrupt flag for task 3
[1]	w1s	1'h0	CTCIF2	clear task complete interrupt flag for task 2
[0]	w1s	1'h0	CTCIF1	clear task complete interrupt flag for task 1
0x08			**IER**	interrupt enable register
[31:17]			RSVD	
[16]	rw	1'h0	TEIE	enable transfer error flag
[15:8]			RSVD	
[7]	rw	1'h0	TCIE8	enable task complete interrupt for task 8
[6]	rw	1'h0	TCIE7	enable task complete interrupt for task 7
[5]	rw	1'h0	TCIE6	enable task complete interrupt for task 6
[4]	rw	1'h0	TCIE5	enable task complete interrupt for task 5
[3]	rw	1'h0	TCIE4	enable task complete interrupt for task 4
[2]	rw	1'h0	TCIE3	enable task complete interrupt for task 3
[1]	rw	1'h0	TCIE2	enable task complete interrupt for task 2
[0]	rw	1'h0	TCIE1	enable task complete interrupt for task 1
0x10			**TCR1**	task 1 control register
[31:24]			RSVD	
[23]	rw	1'h0	REPIRQ	repetition interrupt 0: interrupt will be generated after each operation 1: interrupt will be generated after operation for REP times
[22]	rw	1'h0	REPTRIG	repetition trigger 0: ptc trigger will be generated after each operation 1: ptc trigger will be generated after operation for REP times
[21]	rw	1'h0	REPEN	repetition enable 0: task will be triggerd no matter what value REP is 1: task will only be triggerd when REP is not 0
[20]	w1s	1'h0	SWTRIG	software trigger task will be triggerd at once after SWTRIG set. SWTRIG will be cleared automatically.
[19]	rw	1'h0	TRIGPOL	trigger polarity 0: select positive edge of trigger 1: select negative edge of trigger

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表 7-6: PTC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[18:16]	rw	3'h0	OP	task operation 3'b000: direct write data 3'b100: read then XOR with data and write back 3'b101: read then OR with data and write back 3'b110: read then AND with data and write back 3'b111: read then add with data and write back
[15:8]			RSVD	
[7:0]	rw	8'h0	TRIGSEL	select trigger source 0: task will only be triggered by SWTRIG others: task will be triggered by selected source or SWTRIG
0x14			**TAR1**	task 1 address register
[31:0]	rw	32'h0	ADDR	peripheral address to access to
0x18			**TDR1**	task 1 data register
[31:0]	rw	32'h0	DATA	data value for task operation
0x1C			**RCR1**	task 1 repetition and delay counter register
[31:16]	rw	16'h0	DLY	Delay time before task operation after triggered 0: no delay others: delay DLY HCLK cycles before task operation DLY is read as left delay time. DLY will be reloaded automatically after each operation.
[15:10]			RSVD	
[9:0]	rw	10'h0	REP	Repetition counter value if REPEN is 1, task will only be triggerd when REP is not 0. when REP is larger than 0, it will be decrease by 1 automatically each time task triggered.
0x20			**TCR2**	
[31:24]			RSVD	
[23]	rw	1'h0	REPIRQ	repetition interrupt 0: interrupt will be generated after each operation 1: interrupt will be generated after operation for REP times
[22]	rw	1'h0	REPTRIG	repetition trigger 0: ptc trigger will be generated after each operation 1: ptc trigger will be generated after operation for REP times
[21]	rw	1'h0	REPEN	repetition enable 0: task will be triggerd no matter what value REP is 1: task will only be triggerd when REP is not 0
[20]	w1s	1'h0	SWTRIG	software trigger task will be triggerd at once after SWTRIG set. SWTRIG will be cleared automatically.
[19]	rw	1'h0	TRIGPOL	trigger polarity 0: select positive edge of trigger 1: select negative edge of trigger
[18:16]	rw	3'h0	OP	task operation 3'b000: direct write data 3'b100: read then XOR with data and write back 3'b101: read then OR with data and write back 3'b110: read then AND with data and write back 3'b111: read then add with data and write back
[15:8]			RSVD	

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表 7-6: PTC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[7:0]	rw	8'h0	TRIGSEL	select trigger source
0x24			**TAR2**	
[31:0]	rw	32'h0	ADDR	peripheral address to access to
0x28			**TDR2**	
[31:0]	rw	32'h0	DATA	data value for task operation
0x2C			**RCR2**	task 2 repetition and delay counter register
[31:16]	rw	16'h0	DLY	Delay time before task operation after triggered 0: no delay others: delay DLY HCLK cycles before task operation DLY is read as left delay time. DLY will be reloaded automatically after each operation.
[15:10]			RSVD	
[9:0]	rw	10'h0	REP	Repetition counter value if REPEN is 1, task will only be triggerd when REP is not 0. when REP is larger than 0, it will be decrease by 1 automatically each time task triggered.
0x30			**TCR3**	
[31:24]			RSVD	
[23]	rw	1'h0	REPIRQ	repetition interrupt 0: interrupt will be generated after each operation 1: interrupt will be generated after operation for REP times
[22]	rw	1'h0	REPTRIG	repetition trigger 0: ptc trigger will be generated after each operation 1: ptc trigger will be generated after operation for REP times
[21]	rw	1'h0	REPEN	repetition enable 0: task will be triggerd no matter what value REP is 1: task will only be triggerd when REP is not 0
[20]	w1s	1'h0	SWTRIG	software trigger task will be triggerd at once after SWTRIG set. SWTRIG will be cleared automatically.
[19]	rw	1'h0	TRIGPOL	trigger polarity 0: select positive edge of trigger 1: select negative edge of trigger
[18:16]	rw	3'h0	OP	task operation 3'b000: direct write data 3'b100: read then XOR with data and write back 3'b101: read then OR with data and write back 3'b110: read then AND with data and write back 3'b111: read then add with data and write back
[15:8]			RSVD	
[7:0]	rw	8'h0	TRIGSEL	select trigger source
0x34			**TAR3**	
[31:0]	rw	32'h0	ADDR	peripheral address to access to
0x38			**TDR3**	
[31:0]	rw	32'h0	DATA	data value for task operation
0x3C			**RCR3**	task 3 repetition and delay counter register

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表 7-6: PTC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:16]	rw	16'h0	DLY	Delay time before task operation after triggered 0: no delay others: delay DLY HCLK cycles before task operation DLY is read as left delay time. DLY will be reloaded automatically after each operation.
[15:10]			RSVD	
[9:0]	rw	10'h0	REP	Repetition counter value if REPEN is 1, task will only be triggerd when REP is not 0. when REP is larger than 0, it will be decrease by 1 automatically each time task triggered.
0x40			**TCR4**	
[31:24]			RSVD	
[23]	rw	1'h0	REPIRQ	repetition interrupt 0: interrupt will be generated after each operation 1: interrupt will be generated after operation for REP times
[22]	rw	1'h0	REPTRIG	repetition trigger 0: ptc trigger will be generated after each operation 1: ptc trigger will be generated after operation for REP times
[21]	rw	1'h0	REPEN	repetition enable 0: task will be triggerd no matter what value REP is 1: task will only be triggerd when REP is not 0
[20]	w1s	1'h0	SWTRIG	software trigger task will be triggerd at once after SWTRIG set. SWTRIG will be cleared automatically.
[19]	rw	1'h0	TRIGPOL	trigger polarity 0: select positive edge of trigger 1: select negative edge of trigger
[18:16]	rw	3'h0	OP	task operation 3'b000: direct write data 3'b100: read then XOR with data and write back 3'b101: read then OR with data and write back 3'b110: read then AND with data and write back 3'b111: read then add with data and write back
[15:8]			RSVD	
[7:0]	rw	8'h0	TRIGSEL	select trigger source
0x44			**TAR4**	
[31:0]	rw	32'h0	ADDR	peripheral address to access to
0x48			**TDR4**	
[31:0]	rw	32'h0	DATA	data value for task operation
0x4C			**RCR4**	task 4 repetition and delay counter register
[31:16]	rw	16'h0	DLY	Delay time before task operation after triggered 0: no delay others: delay DLY HCLK cycles before task operation DLY is read as left delay time. DLY will be reloaded automatically after each operation.
[15:10]			RSVD	

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表 7-6: PTC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[9:0]	rw	10'h0	REP	Repetition counter value if REPEN is 1, task will only be triggerd when REP is not 0. when REP is larger than 0, it will be decrease by 1 automatically each time task triggered.
0x50			**TCR5**	
[31:24]			RSVD	
[23]	rw	1'h0	REPIRQ	repetition interrupt 0: interrupt will be generated after each operation 1: interrupt will be generated after operation for REP times
[22]	rw	1'h0	REPTRIG	repetition trigger 0: ptc trigger will be generated after each operation 1: ptc trigger will be generated after operation for REP times
[21]	rw	1'h0	REPEN	repetition enable 0: task will be triggerd no matter what value REP is 1: task will only be triggerd when REP is not 0
[20]	w1s	1'h0	SWTRIG	software trigger task will be triggerd at once after SWTRIG set. SWTRIG will be cleared automatically.
[19]	rw	1'h0	TRIGPOL	trigger polarity 0: select positive edge of trigger 1: select negative edge of trigger
[18:16]	rw	3'h0	OP	task operation 3'b000: direct write data 3'b100: read then XOR with data and write back 3'b101: read then OR with data and write back 3'b110: read then AND with data and write back 3'b111: read then add with data and write back
[15:8]			RSVD	
[7:0]	rw	8'h0	TRIGSEL	select trigger source
0x54			**TAR5**	
[31:0]	rw	32'h0	ADDR	peripheral address to access to
0x58			**TDR5**	
[31:0]	rw	32'h0	DATA	data value for task operation
0x5C			**RCR5**	task 5 repetition counter register
[31:10]			RSVD	
[9:0]	rw	10'h0	REP	Repetition counter value if REPEN is 1, task will only be triggerd when REP is not 0. when REP is larger than 0, it will be decrease by 1 automatically each time task triggered.
0x60			**TCR6**	
[31:24]			RSVD	
[23]	rw	1'h0	REPIRQ	repetition interrupt 0: interrupt will be generated after each operation 1: interrupt will be generated after operation for REP times
[22]	rw	1'h0	REPTRIG	repetition trigger 0: ptc trigger will be generated after each operation 1: ptc trigger will be generated after operation for REP times

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表 7-6: PTC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[21]	rw	1'h0	REPEN	repetition enable 0: task will be triggerd no matter what value REP is 1: task will only be triggerd when REP is not 0
[20]	w1s	1'h0	SWTRIG	software trigger task will be triggerd at once after SWTRIG set. SWTRIG will be cleared automatically.
[19]	rw	1'h0	TRIGPOL	trigger polarity 0: select positive edge of trigger 1: select negative edge of trigger
[18:16]	rw	3'h0	OP	task operation 3'b000: direct write data 3'b100: read then XOR with data and write back 3'b101: read then OR with data and write back 3'b110: read then AND with data and write back 3'b111: read then add with data and write back
[15:8]			RSVD	
[7:0]	rw	8'h0	TRIGSEL	select trigger source
0x64			**TAR6**	
[31:0]	rw	32'h0	ADDR	peripheral address to access to
0x68			**TDR6**	
[31:0]	rw	32'h0	DATA	data value for task operation
0x6C			**RCR6**	task 6 repetition counter register
[31:10]			RSVD	
[9:0]	rw	10'h0	REP	Repetition counter value if REPEN is 1, task will only be triggerd when REP is not 0. when REP is larger than 0, it will be decrease by 1 automatically each time task triggered.
0x70			**TCR7**	
[31:24]			RSVD	
[23]	rw	1'h0	REPIRQ	repetition interrupt 0: interrupt will be generated after each operation 1: interrupt will be generated after operation for REP times
[22]	rw	1'h0	REPTRIG	repetition trigger 0: ptc trigger will be generated after each operation 1: ptc trigger will be generated after operation for REP times
[21]	rw	1'h0	REPEN	repetition enable 0: task will be triggerd no matter what value REP is 1: task will only be triggerd when REP is not 0
[20]	w1s	1'h0	SWTRIG	software trigger task will be triggerd at once after SWTRIG set. SWTRIG will be cleared automatically.
[19]	rw	1'h0	TRIGPOL	trigger polarity 0: select positive edge of trigger 1: select negative edge of trigger

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表 7-6: PTC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[18:16]	rw	3'h0	OP	task operation 3'b000: direct write data 3'b100: read then XOR with data and write back 3'b101: read then OR with data and write back 3'b110: read then AND with data and write back 3'b111: read then add with data and write back
[15:8]			RSVD	
[7:0]	rw	8'h0	TRIGSEL	select trigger source
0x74			**TAR7**	
[31:0]	rw	32'h0	ADDR	peripheral address to access to
0x78			**TDR7**	
[31:0]	rw	32'h0	DATA	data value for task operation
0x7C			**RCR7**	task 7 repetition counter register
[31:10]			RSVD	
[9:0]	rw	10'h0	REP	Repetition counter value if REPEN is 1, task will only be triggerd when REP is not 0. when REP is larger than 0, it will be decrease by 1 automatically each time task triggered.
0x80			**TCR8**	
[31:24]			RSVD	
[23]	rw	1'h0	REPIRQ	repetition interrupt 0: interrupt will be generated after each operation 1: interrupt will be generated after operation for REP times
[22]	rw	1'h0	REPTRIG	repetition trigger 0: ptc trigger will be generated after each operation 1: ptc trigger will be generated after operation for REP times
[21]	rw	1'h0	REPEN	repetition enable 0: task will be triggerd no matter what value REP is 1: task will only be triggerd when REP is not 0
[20]	w1s	1'h0	SWTRIG	software trigger task will be triggerd at once after SWTRIG set. SWTRIG will be cleared automatically.
[19]	rw	1'h0	TRIGPOL	trigger polarity 0: select positive edge of trigger 1: select negative edge of trigger
[18:16]	rw	3'h0	OP	task operation 3'b000: direct write data 3'b100: read then XOR with data and write back 3'b101: read then OR with data and write back 3'b110: read then AND with data and write back 3'b111: read then add with data and write back
[15:8]			RSVD	
[7:0]	rw	8'h0	TRIGSEL	select trigger source
0x84			**TAR8**	
[31:0]	rw	32'h0	ADDR	peripheral address to access to
0x88			**TDR8**	
[31:0]	rw	32'h0	DATA	data value for task operation
0x8C			**RCR8**	task 8 repetition counter register
[31:10]			RSVD	

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表 7-6: PTC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[9:0]	rw	10'h0	REP	Repetition counter value if REPEN is 1, task will only be triggerd when REP is not 0. when REP is larger than 0, it will be decrease by 1 automatically each time task triggered.
0xD0			**MEM1**	temporary memory 1
[31:0]	rw	32'h0	DATA	memory to store temporary variables
0xD4			**MEM2**	temporary memory 2
[31:0]	rw	32'h0	DATA	memory to store temporary variables
0xD8			**MEM3**	temporary memory 3
[31:0]	rw	32'h0	DATA	memory to store temporary variables
0xDC			**MEM4**	temporary memory 4
[31:0]	rw	32'h0	DATA	memory to store temporary variables
0xE0			**GPIO31_0**	
[31:29]			RSVD	
[28:24]	rw	5'h0	SELD	select trigger D of GPIO 31~0
[23:21]			RSVD	
[20:16]	rw	5'h0	SELC	select trigger C of GPIO 31~0
[15:13]			RSVD	
[12:8]	rw	5'h0	SELB	select trigger B of GPIO 31~0
[7:5]			RSVD	
[4:0]	rw	5'h0	SELA	select trigger A of GPIO 31~0 0: select GPIO 0 1: select GPIO 1 ..... 31: select GPIO 31
0xE4			**GPIO63_32**	
[31:29]			RSVD	
[28:24]	rw	5'h0	SELD	select trigger D of GPIO 63~32
[23:21]			RSVD	
[20:16]	rw	5'h0	SELC	select trigger C of GPIO 63~32
[15:13]			RSVD	
[12:8]	rw	5'h0	SELB	select trigger B of GPIO 63~32
[7:5]			RSVD	
[4:0]	rw	5'h0	SELA	select trigger A of GPIO 63~32 0: select GPIO 32 1: select GPIO 33 ..... 31: select GPIO 63
0xE8			**GPIO95_64**	
[31:29]			RSVD	
[28:24]	rw	5'h0	SELD	select trigger D of GPIO 95~64
[23:21]			RSVD	
[20:16]	rw	5'h0	SELC	select trigger C of GPIO 95~64
[15:13]			RSVD	
[12:8]	rw	5'h0	SELB	select trigger B of GPIO 95~64
[7:5]			RSVD	

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表 7-6: PTC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[4:0]	rw	5'h0	SELA	select trigger A of GPIO 95~64 0: select GPIO 64 1: select GPIO 65 ..... 31: select GPIO 95

7.5 USB

USB 位于 HPSYS。

本芯片集成了一路全速（FS）USB2.0 Host/Device 接口，符合 USB 2.0 的协议规范，具有如下功能：

- 软件可配置的端点设置，支持挂起/恢复
- 支持动态 FIFO 大小
- 支持会话请求协议和主机协商协议
- 支持全速以及慢速模式
- 片内集成 USB2.0 FS PHY
- 拥有 ep0~ep7 8 个通道，其中 ep2~ep4 只支持 rx(即 host 只支持 IN，device 只支持 OUT)，ep2~ep4 只支持 tx(即 host 只支持 OUT，device 只支持 IN)

8 模拟外设

8.1 GPADC

GPADC 位于 LPSYS，可向 DMAC2 发送请求。

8.1.1 简介

GPADC 是一个 12bit 精度 SARADC，支持 0-3.3V 输入电压，输出为 12bit 数据。输入电压可为单端或差分，输出数据可通过 APB 总线或 DMA 接口读取。

8.1.2 主要特性

- 输入电压范围：0~3.3V，12Bit 分辨率
- 支持单端模式和双端模式
- 支持 8 路单端模拟输入或 4 对差分模拟输入
- 支持单次测量模式和循环测量模式
- 每次测量可以划分为 8 个时隙，各时隙可以单独配置模拟输入通道
- 支持软件（写寄存器）和硬件（如计时器）触发方式
- 支持 DMA 通道
- 采样频率可配，最高采样频率 4MHz
- 转换完成后产生中断

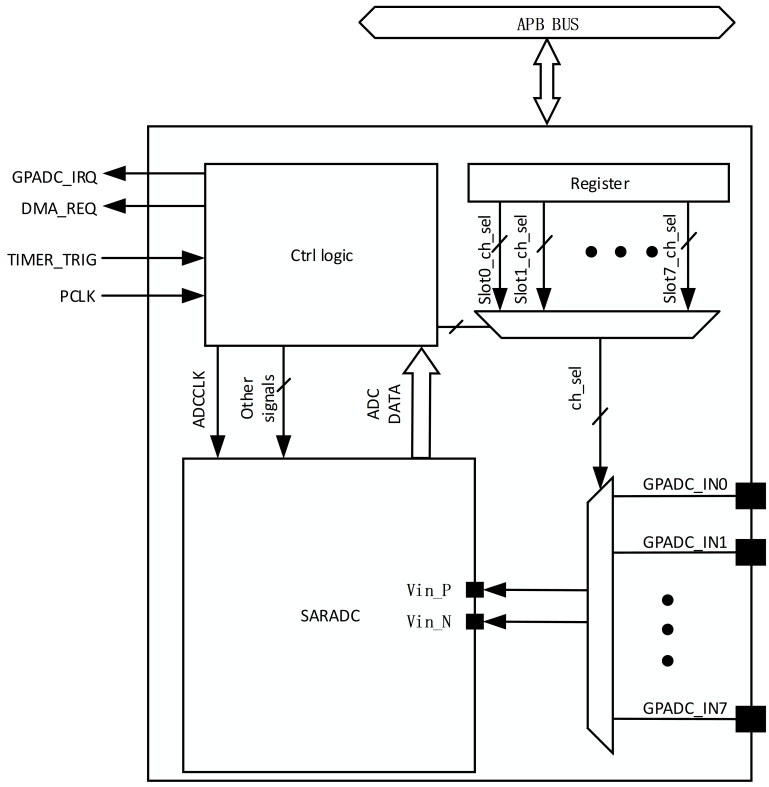

图 8-1: GPADC 框图

8.1.3 功能描述

8.1.3.1 GPADC 时钟产生

GPADC 时钟由 PCLK 分频产生，通过配置 ADC_CTRL_REG 的 DATA_SAMP_DLY 和 ADC_CTRL_REG2 中的 CONV_WIDTH 和 SAMP_WIDTH 设置 ADCCLK 频率，计算公式为：

$$f_{ADCCLK} = f_{PCLK}/(DATA\_SAMP\_DLY + CONV\_WIDTH + SAMP\_WIDTH + 2)$$

因为 ADCCLK 由 PCLK 分频产生，设置 ADCCLK 频率时需要注意确认 PCLK 频率。

8.1.3.2 时隙配置

每一轮 GPADC 采样，共有 8 个时隙按顺序依次工作，通过设置 ADC_SLOT*_REG 中的 SLOT_EN 每个时隙可单独使能或禁用；通过设置 ADC_SLOT*_REG 中的 PCHNL_SEL 和 NCHNL_SEL，可独立配置各时隙的输入通道。

8.1.3.3 单端/差分模式

将寄存器 ADC_CFG_REG 中的 ANAU_GPADC_SE 置为 1，则 GPADC 为单端输入模式，只需设置各时隙对应配置寄存器中的 PCHNL_SEL 来选择输入通道。

将寄存器 ADC_CFG_REG 中的 ANAU_GPADC_SE 置为 0，则 GPADC 为差分输入模式，设置各时隙对应配置寄存器中的 PCHNL_SEL 和 NCHNL_SEL 来选择 Vin_P 和 Vin_N 对应的输入通道。

8.1.3.4 输入通道选择

GPADC 共有 8 路输入通道，通过设置 ADC_SLOT*_REG 中的 PCHNL_SEL 和 NCHNL_SEL，可配置各时隙所要采样的输入通道。

如果为单端模式，只需设置 PCHNL_SEL 来选择输入通道。

8.1.3.5 采样模式

若 ADC_CTRL_REG 中的 ADC_OP_MODE 置 0，则 GPADC 处于单次采样模式，该模式下每次启动 GPADC 后，GPADC 将按照各时隙配置完成一轮采样，然后回到等待触发状态。

若 ADC_CTRL_REG 中的 ADC_OP_MODE 置 1，则 GPADC 处于连续采样模式，该模式下每次启动 GPADC 后，GPADC 将循环按照各时隙配置循环进行采样。将 ADC_CTRL_REG 的 ADC_STOP 置 1 可使 GPADC 回到等待触发状态。

8.1.3.6 启动 GPADC

- 写寄存器启动
  将寄存器 ADC_CTRL_REG 中的 ADC_START 置 1，可以启动 GPADC。
  触发 GPADC 后，如果 GPADC 处于单次采样模式，则完成一轮采样后，回到等待触发状态。如果 GPADC 处于连续采样模式，则需将 ADC_CTRL_REG 的 ADC_STOP 置 1 使 GPADC 回到等待触发状态。
- Timer 触发
  GPADC 支持 TIMER 触发，使能 TIMER 触发功能需要将 ADC_CTRL_REG 中的 TIMER_TRIG_EN 置为 1。共有 8 个触发源，可通过寄存器 ADC_CTRL_REG 中的 TIMER_TRIG_SRC_SEL 选择触发源。对应关系如下表：

TIMER_TRIG_SRC_SEL	TRIG_SRC
0	GPTIM3 TRGO
1	GPTIM4 TRGO
2	GPTIM5 TRGO
3	BTIM3 TRGO
4	BTIM4 TRGO
5	GPTIM3 CH0 输出
6	GPTIM3 CH1 输出
7	GPTIM3 CH2 输出

  触发 GPADC 后，如果 GPADC 处于单次采样模式，则完成一轮采样后，回到等待触发状态。如果 GPADC 处于连续采样模式，则需将 ADC_CTRL_REG 的 ADC_STOP 置 1 使 GPADC 回到等待触发状态。

8.1.3.7 数据访问

GPADC 转换得到的数据可以通过以下两种方式访问：

- 寄存器读取
  软件可以通过读寄存器直接读取 GPADC 转换结果。各时隙对应数据存放在寄存器 ADC_RDATA* 中，寄存器和各时隙数据的对应关系如下表：

ADC_RDATA0[31:0]	
SLOT1_RDATA	SLOT0_RDATA
ADC_RDATA1[31:0]	
SLOT3_RDATA	SLOT2_RDATA
ADC_RDATA2[31:0]	
SLOT5_RDATA	SLOT4_RDATA
ADC_RDATA3[31:0]	
SLOT7_RDATA	SLOT6_RDATA

在寄存器 ADC_RDATA* 中，各时隙对应的 GPADC 输出数据的 LSB 向右对齐到寄存器的 0 比特或者 16 比特。以 ADC_RDATA0 为例说明时隙数据在寄存器里的对齐方式，对齐方式如下表：

SLOT0_RDATA（ADC_RDATA0[31:16]）																SLOT0_RDATA（ADC_RDATA0[15:0]）															
0	0	0	0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	0	0	0	0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

- DMA 模式
  通过 LPSYS 中的 DMAC2 读取 GPADC 的转换结果。使用流程为：
  将寄存器 ADC_CTRL_REG 的 DMA_EN 置 1。
  将 DMA 的源地址设置为 0x50016034。ADC 数据在该地址的对齐方式是：

Bit[15：0]															
0	0	0	0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

  其他 DMA 设置参考 DMAC 章节。

8.1.3.8 通知机制

GPADC 在结束采样转换的时会产生中断，上报给 CPU。

该中断可以通过给寄存器 GPADC_IRQ 的 GPADC_IMR 置 1 来屏蔽。

该中断可以通过给寄存器 GPADC_IRQ 的 GPADC_ICR 置 1 来清中断。

8.1.3.9 配置启动流程

使用 GPADC 一般经过以下流程：

- 配置 PINMUX。
- 配置 GPADC 时钟频率，输入通路选择等信息。
- 将寄存器 ADC_CFG_REG1 中的 ANAU_GPADC_EN_BG 置 1 使能 Bandgap。
- 将寄存器 ADC_CFG_REG1 中的 ANAU_GPADC_LDOREF_EN 置 1 使能给 GPADC 提供参考电压的 LDO。
- 将寄存器 ADC_CFG_REG1 中的 FRC_ADC_EN 设置为 1 使能 GPADC。
- 触发 GPADC，开始采样，读取数据。
- 采样完成后将寄存器 ADC_CTRL_REG 中的 FRC_EN_ADC 置 0，关闭 GPADC 模块。如果是连续采样模式还需要先将寄存器 ADC_CTRL_REG 中的 ADC_STOP 先置 1 再置 0 来中断采样流程。
- 将寄存器 ADC_CFG_REG1 中的 ANAU_GPADC_LDOREF_EN 置 0 关闭给 GPADC 提供参考电压的 LDO。
- 将寄存器 ADC_CFG_REG1 中的 ANAU_GPADC_EN_BG 置 0 关闭 Bandgap

过程需要满足一些电路稳定时间。

- Pinmux 配置后，PAD 连到输入通道的电压需要一定的稳定时间，时间由 PAD 所接的 RC 数值决定。
- 打开 bandgap 后，再打开提供参考电压的 LDO, LDO 需要 200us 稳定时间。
- 使能 GPADC 后需要至少 200us 的启动时间。
- 最后通过写寄存器触发或 Timer 触发启动 GPADC。

8.1.4 GPADC 寄存器

表 8-1: GPADC 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00			**ADC_CFG_REG1**	ADC Analog Config Register 1
[31:30]			RSVD	
[29:25]	rw	5'h16	ANAU_GPADC_CMM	Tune CDAC CM voltage 375mV range (increasing) / 25mV step, 8: for 0.5V Vcm,in
[24:22]	rw	3'h3	ANAU_GPADC_CMPCL	Tune ADC comparator CL= 3: 40f, range: 10fF (0) ~ 80fF (7) / 10fF step
[21:20]	rw	2'h2	ANAU_GPADC_VSP	Set comparator input CM in sampling phase, 0.539V (0) / 0.578V (1) / 0.642V (2) / 0.784V (3)
[19]	rw	1'h0	ANAU_GPADC_LDOREF_EN	Enable LDORF for ADC VREF
[18:15]	rw	4'hA	ANAU_GPADC_LDOVREF_SEL	Set reference voltage for LDOREF, range = 0.35V(0) ~ 0.65V(15), step = 20mV
[14:12]	rw	3'h1	ANAU_GPADC_SEL_PCH	Select P-side input channel for GPADC, 0 for channel 0, 7 for channel 7, effective when force on
[11:9]	rw	3'h0	ANAU_GPADC_SEL_NCH	Select N-side input channel for GPADC, 0 for channel 0, 7 for channel 7, effective when force on
[8]	rw	1'h0	ANAU_GPADC_MUTE	Short GPADC P & N input to CMREF, i.e., VREF/2
[7]	rw	1'h0	ANAU_GPADC_SE	Set GPADC in single-ended mode, signal range at P-input: 0 ~ VREF
[6]	rw	1'h0	ANAU_GPADC_EN_V18	
[5:3]	rw	3'h2	ANAU_GPADC_CL_DLY	
[2]	rw	1'h0	ANAU_GPADC_P_INT_EN	
[1]			RSVD	
[0]	rw	1'h0	ANAU_GPADC_CMREF_FAST_EN	
0x04			**ADC_Slot0_REG**	ADC Slot0 Config Register
[31:14]			RSVD	
[13:11]	rw	3'h1	NCHNL_SEL	
[10:8]	rw	3'h0	PCHNL_SEL	
[7:1]			RSVD	
[0]	rw	1'h1	SLOT_EN	
0x08			**ADC_Slot1_REG**	ADC Slot1 Config Register
[31:14]			RSVD	
[13:11]	rw	3'h1	NCHNL_SEL	
[10:8]	rw	3'h0	PCHNL_SEL	
[7:1]			RSVD	
[0]	rw	1'h1	SLOT_EN	
0x0C			**ADC_Slot2_REG**	ADC Slot2 Config Register
[31:14]			RSVD	
[13:11]	rw	3'h1	NCHNL_SEL	
[10:8]	rw	3'h0	PCHNL_SEL	

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表 8-1: GPADC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[7:1]			RSVD	
[0]	rw	1'h1	SLOT_EN	
0x10			**ADC_Slot3_REG**	ADC Slot3 Config Register
[31:14]			RSVD	
[13:11]	rw	3'h1	NCHNL_SEL	
[10:8]	rw	3'h0	PCHNL_SEL	
[7:1]			RSVD	
[0]	rw	1'h1	SLOT_EN	
0x14			**ADC_Slot4_REG**	ADC Slot4 Config Register
[31:14]			RSVD	
[13:11]	rw	3'h1	NCHNL_SEL	
[10:8]	rw	3'h0	PCHNL_SEL	
[7:1]			RSVD	
[0]	rw	1'h1	SLOT_EN	
0x18			**ADC_Slot5_REG**	ADC Slot5 Config Register
[31:14]			RSVD	
[13:11]	rw	3'h1	NCHNL_SEL	
[10:8]	rw	3'h0	PCHNL_SEL	
[7:1]			RSVD	
[0]	rw	1'h1	SLOT_EN	
0x1C			**ADC_Slot6_REG**	ADC Slot6 Config Register
[31:14]			RSVD	
[13:11]	rw	3'h1	NCHNL_SEL	
[10:8]	rw	3'h0	PCHNL_SEL	
[7:1]			RSVD	
[0]	rw	1'h1	SLOT_EN	
0x20			**ADC_Slot7_REG**	ADC Slot7 Config Register
[31:14]			RSVD	
[13:11]	rw	3'h1	NCHNL_SEL	
[10:8]	rw	3'h0	PCHNL_SEL	
[7:1]			RSVD	
[0]	rw	1'h1	SLOT_EN	
0x24			**ADC_RDATA0**	ADC Read Data0
[31:28]			RSVD	
[27:16]	r	12'h0	SLOT1_RDATA	
[15:12]			RSVD	
[11:0]	r	12'h0	SLOT0_RDATA	
0x28			**ADC_RDATA1**	ADC Read Data1
[31:28]			RSVD	
[27:16]	r	12'h0	SLOT3_RDATA	
[15:12]			RSVD	
[11:0]	r	12'h0	SLOT2_RDATA	
0x2C			**ADC_RDATA2**	ADC Read Data2
[31:28]			RSVD	
[27:16]	r	12'h0	SLOT5_RDATA	
[15:12]			RSVD	
[11:0]	r	12'h0	SLOT4_RDATA	
0x30			**ADC_RDATA3**	ADC Read Data3

续表下页...

表 8-1: GPADC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:28]			RSVD	
[27:16]	r	12'h0	SLOT7_RDATA	
[15:12]			RSVD	
[11:0]	r	12'h0	SLOT6_RDATA	
0x34			**ADC_DMA_RDATA**	ADC Read Data For DMA
[31:29]			RSVD	
[28:16]	r	13'h0	DMA_RDATA_RAW	
[15:13]			RSVD	
[12:0]	r	13'h0	DMA_RDATA	
0x38			**ADC_CTRL_REG**	ADC Control Register
[31:21]			RSVD	
[20:17]	rw	4'h4	DATA_SAMP_DLY	
[16]	rw	1'b0	DMA_DATA_SEL	0: combined data 1: raw data
[15]	rw	1'b0	TIMER_TRIG_TYP	0: pulse no edge detect needed 1: level,need edge detect
[14:12]	rw	3'h0	TIMER_TRIG_SRC_SEL	Timer trigger source select
[11]	rw	1'b0	FRC_EN_ADC	Enable GPADC core
[10]	rw	1'b0	CHNL_SEL_FRC_EN	Enable input channel setting in ADC_CFG_REG1
[9]	rw	1'b1	TIMER_TRIG_EN	Enable timer trigger function
[8]			RSVD	
[7]	rw	1'b1	DMA_EN	Enable DMA interface
[6:3]	rw	4'h6	INIT_TIME	GPADC will wait INIT_TIME ADCCLK cycles to start sample/conversion after being trigged
[2]	rw	1'b0	ADC_STOP	Write 1 to stop GPADC in continuous mode(need write 0 to clear)
[1]	w1s	1'b0	ADC_START	Write 1 to start GPADC,(don't need clear)
[0]	rw	1'b0	ADC_OP_MODE	0: single conversion mode 1: continuous conversion mode
0x3C			**ADC_CTRL_REG2**	ADC Control Register2
[31:24]	rw	8'h80	CONV_WIDTH	
[23:0]	rw	24'h8000	SAMP_WIDTH	
0x40			**GPADC_STATUS**	GPADC Status Register
[31:12]			RSVD	
[11:9]	r	3'h0	CUR_SLOT	
[8:1]	r	8'h0	SLOT_DONE	
[0]	r	1'h0	ADC_DONE	
0x44			**GPADC_IRQ**	GPADC IRQ Register
[31:4]			RSVD	
[3]	r	1'b0	GPADC_ISR	
[2]	r	1'b0	GPADC_IRSR	
[1]	rw	1'b0	GPADC_IMR	
[0]	w1s	1'b0	GPADC_ICR	

8.2 TSEN

TSEN 位于 LPSYS。

8.2.1 简介

TSEN 通过采样内部温敏电阻的电压将温度转换为数字编码，帮助系统实时监控芯片温度。

8.2.2 主要特性

- 分辨率为 0.2°C
- 精度为-3°C 到 3°C
- 支持温度范围为-40°C 到 125°C
- 主持轮询或中断方式读数

8.2.3 功能描述

8.2.3.1 时钟信号

TSEN 的工作时钟由 LPSYS 的 PCLK 分频而来。分频比由寄存器 TSEN_CTRL_REG 中的 ANAU_TSEN_CLK_DIV 来设置。频率计算关系为:

$$ftsen = fpclk/ANAU\_TSEN\_CLK\_DIV$$

8.2.3.2 读数流程

转换结果从寄存器 TSEN_RDATA 读取, 读取后的结果通过如下公式转换为温度：

$$Temp = (Dec(TSEN_RDATA) + 3000)/10100 * 749.2916 - 277.5391$$

通过轮询读数的流程：

启动 TSEN 后，轮询寄存器 TSEN_IRQ 中的 TSEN_IRSR，当 TSEN_IRSR 值为 1 时，标志温度数据已转换完成，。读数后将寄存器 TSEN_IRQ 中的 TSEN_ICR 置 1, 将 TSEN_IRSR 清零。

通过中断读数的流程：

使能 TSEN 中断，并将寄存器 TSEN_IRQ 中的 TSEN_IMR 置 0，启动 TSEN，转换完成后会给 CPU 发出 TSEN_IRQ 中断。处理中断, 将寄存器 TSEN_IRQ 中的 TSEN_ICR 置 1 清中断，读数。

8.2.3.3 使用过程

TSEN 的工作需要按照以下流程。

1. 根据 PCLK 频率配置分频比，TSEN 的时钟频率应为 1MHz 或 2MHz。
2. 将寄存器 BGR 中的 EN 置 1，打开 Bandgap。
3. 将寄存器 ANAU_ANA_TP 中的 ANAU_IARY_EN 置 1，打开 Iarray。
4. 将寄存器 TSEN_CTRL_REG 中的 ANAU_TSEN_EN 置 1，使能 TSEN 的时钟。
5. 将寄存器 TSEN_CTRL_REG 中的 ANAU_TSEN_PU 置 1，ANAU_TSEN_RUN 置 0。
6. 将寄存器 TSEN_CTRL_REG 中的 ANAU_TSEN_RSTB 先置 0 再置 1，低电平至少 20us。
7. 将寄存器 TSEN_CTRL_REG 中的 ANAU_TSEN_RUN 置 1，通过轮询或中断方式读取结果。也可以等待 3ms 绝对时间后读数。
8. 关闭 TSEN：将寄存器 TSEN_CTRL_REG 中的 ANAU_TSEN_RUN/ANAU_TSEN_PU/ANAU_TSEN_EN 置 0，ANAU_TSEN_RSTB 置 1。
9. 将寄存器 ANAU_ANA_TP 中的 ANAU_IARY_EN 置 0，关闭 Iarray。
10. 将寄存器 BGR 中的 EN 置 0，关闭 Bandgap。

8.2.4 TSEN 寄存器

表 8-2: TSEN 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00			**TSEN_CTRL_REG**	TSEN Analog Control Register
[31:18]			RSVD	
[17:12]	rw	6'h30	ANAU_TSEN_CLK_DIV	gen tsen clk by divide hclk by anau_tsen_clk_div
[11]	rw	1'h0	ANAU_TSEN_EN	Enable tsen digital module
[10]	r	1'h0	ANAU_TSEN_RDY	tsen ready
[9]	rw	1'h0	ANAU_TSEN_SER_PAR_SEL	serial-parallel output selection
[8]	rw	1'b0	ANAU_TSEN_SGN_EN	signature-mode enable
[7:6]	rw	2'h1	ANAU_TSEN_FCK_SEL	select internal clock frequency
[5:3]	rw	3'h1	ANAU_TSEN_IG_VBE	bias current selection to tune vba
[2]	rw	1'h0	ANAU_TSEN_RUN	enable tsen run
[1]	rw	1'h1	ANAU_TSEN_RSTB	resetb for tsen
[0]	rw	1'h0	ANAU_TSEN_PU	power up tsen
0x04			**TSEN_RDATA**	Tsen Read Data
[31:12]			RSVD	
[11:0]	r	12'h0	TSEN_RDATA	
0x08			**TSEN_IRQ**	Tsen IRQ Register
[31:4]			RSVD	
[3]	r	1'b0	TSEN_ISR	
[2]	r	1'b0	TSEN_IRSR	
[1]	rw	1'b0	TSEN_IMR	
[0]	w1s	1'b0	TSEN_ICR	
0x10			**ANAU_ANA_TP**	Tsen IRQ Register
[31:7]			RSVD	
[0]	rw	1'b0	ANAU_IARY_EN	
0x14			**BGR**	Bandgap registers
[31:12]			RSVD	
[11:8]	rw	4'hC	VREF12	select VREF 1.2V
[7:4]	rw	4'hC	VREF06	select VREF 0.6V
[3:1]			RSVD	
[0]	rw	1'h0	EN	Bandgap enable

9 定时器

9.1 ATIM

ATIM1 位于 HPSYS，输入输出连接至 IO(PA)，可向 DMAC1 发送请求。

9.1.1 简介

ATIM (Advanced Timer) 基于一个 32 比特计数器，可实现计时、测量输入信号的脉冲长度 (输入捕获) 或者产生输出波形 (输出比较和 PWM) 等功能。ATIM 支持 6 路带死区保护的 PWM 互补输出，支持多路 PWM 同时换相，并有 2 路刹车输入可快速将输出切换至安全状态。计数器本身可以进行递增、递减或者递增/递减计数，计数时钟可选系统 PCLK、IO 输入信号或级联输入信号，并可进行 1~65536 倍的预分频。ATIM 共有 6 个通道，可以分别独立配置为输入捕获或输出模式。计数、输入捕获和输出比较的结果可以产生中断、DMA 请求或 PTC 事件。ATIM 包含主从模式接口，可以进行多级级联，实现多级计数或同步触发等功能。

9.1.2 主要特性

- 32 位递增、递减、递增/递减自动重装载计数器
- 16 位可编程 (可以实时修改) 预分频器，计数器时钟频率的分频系数为 1~65536 之间的任意数值
- 16 位可配置重复计数
- 支持单笔计数模式 (OPM)，当重复计数完成后自动停止计数器
- 6 个独立通道
  - 通道 1~3 可分别配置为输入或输出模式，其中每个通道可输出两路带死区保护的互补 PWM
  - 通道 4 可配置为输入或输出模式，可输出单路 PWM
  - 通道 5~6 可配置为输出比较模式
- 输入模式
  - 上升沿/下降沿捕获
  - PWM 脉宽和周期捕获 (需占用两个通道)
  - 可选 4 个输入端口之一或 1 个外部触发端口，支持防抖动滤波和预降频
- 输出模式
  - 强制输出高/低电平
  - 计数到比较值时输出高/低/翻转电平
  - PWM 输出，可配脉宽和周期
  - 多通道 PWM 组合输出，可产生有相互关系的多路 PWM
  - 单脉冲/重触发单脉冲模式输出
- 主从模式
  - 支持多计数器互连，可在作为主设备产生控制信号的同时，作为从设备被外部输入或其它主设备控制
  - 控制模式包括复位、触发、门控等
  - 支持多计数器同步启动、复位等
- 编码模式输入，控制计数器递增/递减计数

- 支持用于定位的霍尔传感器电路
- 2 路刹车输入，支持防抖动滤波，可将输出快速置于安全状态。刹车信号源包括：
  - CPU 异常
  - 比较器
  - 外部输入
  - 软件触发
- 如下事件发生时产生中断/DMA 请求/PTC 触发：
  - 更新：计数器递增溢出/递减溢出，计数器初始化 (通过软件或者内部/外部触发)
  - 触发事件 (计数器启动、停止、初始化或者由内部/外部触发计数)
  - 输入捕获
  - 输出比较
  - 刹车
  - 换相

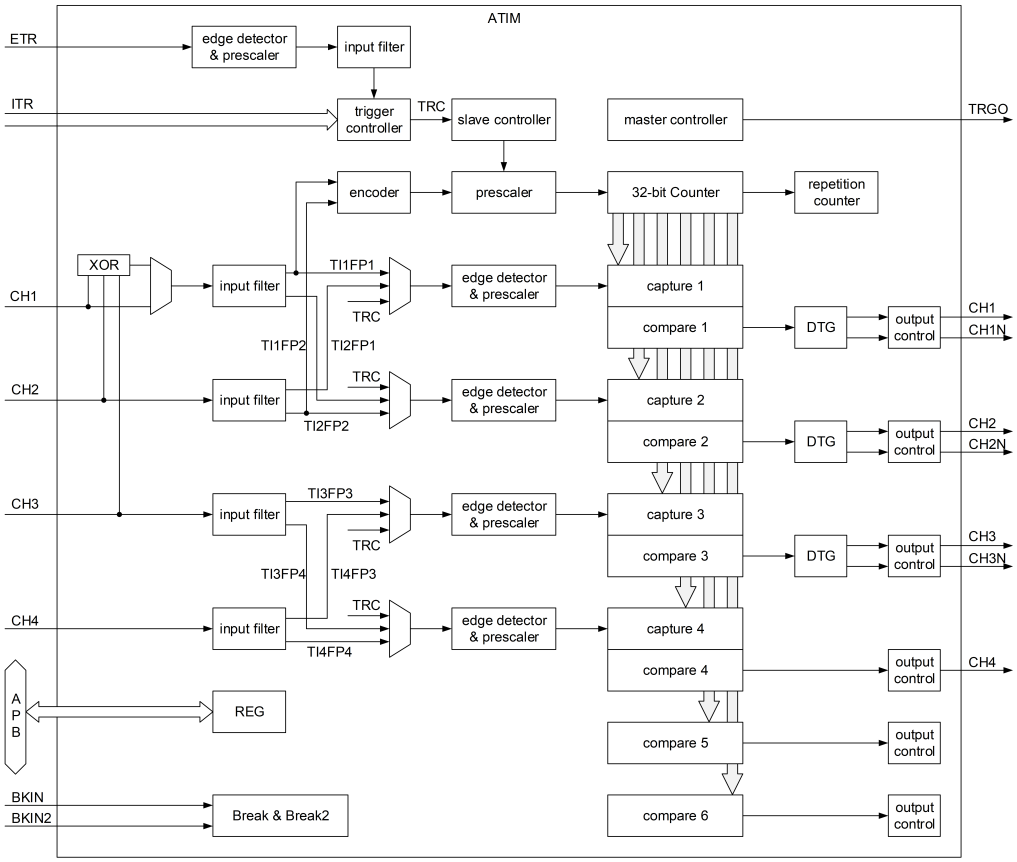


图 9-1: ATIM 结构图

9.1.3 ATIM 功能描述

9.1.3.1 计数器

ATIM 的各项功能均基于一个 32 比特的计数器。计数器基于事件计数，最基本的事件是一个 PCLK 时钟的翻转。根据不同配置，其它计数事件包括外部输入的翻转、其它定时器的输出翻转、正交编码器接口解码输出等。

计数事件经过预分频处理才会真正进入计数器。预分频的次数介于 1 到 65536 之间 (PSC+1)，即仅当发生了 (PSC+1) 次计数事件，计数器的值才真正改变一次。

计数器共有三种计数模式：递增，递减以及中心对齐。在递增计数模式下 (CR1_CMS=0 且 CR1_DIR=0)，计数器从 0 计数到自动重载值 ARR，然后重新从 0 开始计数并产生计数器上溢事件。在递减计数模式下 (CR1_CMS=0 且 CR1_DIR=1)，计数器从 ARR 开始递减计数到 0，然后重新从 ARR 开始计数并产生计数器下溢事件。在中心对齐模式下 (CR1_CMS 不为 0)，计数器从 0 开始计数到 ARR-1，产生计数器上溢事件，然后从 ARR 开始向下计数到 1 并产生计数器下溢事件，之后从 0 开始重新计数。

计数值可以通过 CNT 读出。计数的方向可以从 CR1_DIR 读出。

9.1.3.2 更新事件 (UEV)

更新事件用于标志一个计数单元的结束。最基本的更新事件产生于每次计数器上溢或下溢时 (未开启重复计数时)。软件将 EGR_UG 置 1 时，也将产生更新事件。更新事件可以产生中断、DMA 请求以及 PTC 触发，是定时器最基本的一项通知功能。

通过软件将 CR1_UDIS 置 1 可禁止产生更新事件。这可避免向预装载寄存器写入新值时更新影子寄存器。在 UDIS 位写入 0 之前不会产生任何更新事件。

如果 CR1_URS（更新请求选择）已置 1，则将 EGR_UG 置 1 会生成更新事件，但不会将 UIF 标志置 1（因此，不会发送任何中断或 DMA 请求）。这样一来，如果在发生捕获事件时将计数器清零，将不会同时产生更新中断和捕获中断。

发生更新事件时，将重新装载 RCR，ARR 以及 PSC 寄存器，且将更新标志 SR_UIF 置 1（CR1_URS=0 时）。该功能可以保证修改这些计数器的基本参数不影响当前计数单元，在下一个计数周期才生效。

9.1.3.3 重复计数

如果配置了重复计数器 (RCR>0)，每次计数器上溢或下溢时重复计数器会递减，并仅当重复计数器为 0 时才产生更新事件。更新事件发生时，重复计数器会重新装载 RCR 的值。

重复计数器的当前值不能读出。

9.1.3.4 影子寄存器

对 RCR，ARR 以及 PSC 寄存器的修改不会直接体现在当前计数单元中，而是等到更新事件发生时才真正更新进去。在更新事件发生前，计数器真正使用的是影子寄存器中的值。这样即使在计数中动态改变这些寄存器的值，也不会影响到当前计数单元的完整性，对于 PWM 输出等应用场景很有意义。

如果 CR1_APRE 为 0，ARR 寄存器将在配置后实时生效，不用等到更新事件发生。

输出比较寄存器 CCRx 也有影子寄存器。当 CCMRx_OCxPE 为 0 时，配置的 CCRx 会立即生效，否则要等到更新事件发生时才生效。

9.1.3.5 主从模式

定时器可同时处于主模式与从模式。主模式是指该定时器可以输出 TRGO 信号至芯片上其它定时器的 ITR 输入，用于控制其它定时器的计数行为。从模式是指该定时器的计数行为受外部输入 ETR，其它定时器输出至该定时

器的 ITR 信号，或定时器的通道输入 CHx 的控制。

多个定时器可通过主从模式实现定时器同步，以实现多级分频、同时启动、门控计数等功能。

主模式可在不同事件发生时输出 TRGO 信号，如更新、使能、输入捕获、输出比较等，由 CR2_MMS 选择。

从模式可以选择计数器复位、触发启动、计数使能、计数事件等行为，由 SMCR_SMS 选择。从模式依赖的触发信号 TRGI 可灵活配置，可以在 ETR，ITR 以及通道输入中选择，并可选择信号极性，进行预分频、滤波等操作。

- 定时器处于复位从模式 (SMCR_SMS=0100) 时，当 TRGI 发生变化时，计数器及其预分频器重新初始化。如果 CR1_URS 为 0，则会生成更新事件 UEV，然后所有预装载寄存器 ARR 和 CCRx 都将更新。
- 定时器处于门控从模式 (SMCR_SMS=0101) 时，当 TRGI 满足高电平或低电平要求时才进行计数，否则计数器不变。
- 定时器处于触发从模式 (SMCR_SMS=0110) 时，软件不需配置 CR1_CEN 开启计数，而是当 TRGI 满足特定触发要求时自动启动计数器。
- 定时器处于外部时钟从模式 (SMCR_SMS=0111) 时，计数事件修改为 TRGI 的上升沿，仅当 TRGI 发生翻转时才进行计数。
- 定时器处于复位触发从模式 (SMCR_SMS=1000) 时，TRGI 满足特定触发要求时复位计数器并自动重新开启。

9.1.3.6 通道输入输出

定时器的部分通道可以独立配置为输入捕获模式 (CCMRx_CCxS!=0) 或输出模式 (CCMRx_CCxS=0)。

在输入捕获模式下，通道在对应的触发信号有效时，将计数器的值记录进 CCRx，并产生中断等通知信号。该触发信号可在 ETR，ITR 以及通道输入 CHx 中选择，并可选择信号极性，进行预分频、滤波等操作。通道产生的通知信号包括中断、DMA 请求、PTC 触发等。输入捕获模式可实现记录外部信号改变的时刻、测量 PWM 周期和占空比等功能。

在输出模式下，通道将比较计数器的值与 CCRx 的大小，在通道输出 CHx/CHxN 上产生固定电平，或产生基于本通道以及其它通道比较结果的 PWM 输出信号，并产生中断等通知信号。产生 PWM 信号的脉冲个数、频率、占空比、相位等参数均可调节。多个通道还可以联合产生特定关系的 PWM 组合，如带死区保护的 6 路互补 PWM 等。通道产生的通知信号包括中断、DMA 请求、PTC 触发等。

在输出模式下，一旦出现紧急情况，可以通过断路输入信号 BKIN 和 BKIN2 紧急关闭输出使能，或将输出置于预设电平，以保护定时器连接的外部电路。

9.1.3.7 输入捕获模式

在输入捕获模式下，当通道相应的触发信号检测到跳变沿后，将使用 CCRx 来锁存计数器的值。发生捕获事件时，会将相应的 SR_CCxIF 标志置 1，并可发送中断、DMA 请求（如果已使能）或 PTC 触发信号。如果发生捕获事件时 SR_CCxIF 标志已处于高位，则会将重复捕获标志 SR_CCxOF 置 1。可通过软件将 SR_CCxIF 清零，方法是向 SR_CCxIF 写入 0，或读取存储在 CCRx 中的已捕获数据。向 SR_CCxOF 写入 0 后会将其清零。

以下示例说明了如何在 CH1 输入出现上升沿时将计数器的值捕获到 CCR1 中，具体操作步骤如下：

1. 选择有效输入：通道 1 要连接到 CH1 输入，因此向 CCMR1_CC1S 写入 01。
2. 根据连接到定时器的信号，对所需的输入滤波带宽进行配置。

假设 CH1 信号边沿变化时，最多在 5 个 PCLK 周期内发生抖动，需将滤波带宽设置为大于 5 个 PCLK 周期。将 CCMR1_IC1F 设置为 0011(0x3)，则在检测到连续 8 个采样点（以 PCLK 频率采样）均为新电平后，可以确认 CH1 的跳变沿。

3. 将 CCER_CC1P 和 CCER_CC1NP 写 0，选择 CH1 上的有效转换边沿为上升沿。
4. 对输入预分频器进行编程。
   在本例中我们希望每次有效转换时都执行捕获操作，因此禁用预分频器（CCMR1_IC1PS 写 00）。
5. CCER_CC1E 置 1，使能通道 1，允许将计数器的值捕获到 CCR1 中。
6. 如果需要，可将 DIER_CC1IE 置 1 来使能相关中断请求，或将 DIER_CC1DE 置 1 来使能 DMA 请求。

配置完成后，通道将在 CH1 输入出现上升沿时执行下列操作：

1. CCR1 寄存器记录计数器的值。
2. SR_CCxIF 标志置 1（中断标志）。如果至少发生了两次连续捕获，但 SR_CCxIF 未被清零，这样 SR_CCxOF 捕获溢出标志会被置 1。
3. 根据 CCER_CC1IE 生成中断。
4. 根据 DIER_CC1DE 生成 DMA 请求。

要处理重复捕获，建议在读出 SR_CCxOF 之前读取数据。这样可避免丢失在读取 SR_CCxOF 之后与读取数据之前可能出现的重复捕获信息。

通过软件将 EGR_CCxG 置 1 可立即产生一次捕获，并生成通道捕获中断和 DMA 请求。

9.1.3.8 PWM 输入捕获

PWM 输入捕获是输入捕获的一种扩展应用，可用于测量 PWM 输入信号的周期和占空比。为实现该功能，需要将两个通道都配置为输入捕获模式，触发信号分别映射成输入 PWM 的正边沿和负边沿，并开启计数器复位的从模式。

以下示例说明了如何用通道 1 和通道 2 测量从 CH1 输入的 PWM 的周期和占空比，具体操作步骤如下：

1. 选择通道 1 的有效输入为 CH1 输入，因此向 CCMR1_CC1S 写入 01。
2. 选择通道 1 输入信号的有效极性（用于在 CCR1 中捕获和计数器清零），将 CCER_CC1P 和 CCER_CC1NP 写 0，选择 CH1 上的有效转换边沿为上升沿。
3. 选择通道 2 的有效输入也为 CH1 输入，向 CCMR1_CC2S 写入 10(0x2)。
4. 选择通道 2 输入信号的有效极性（用于 CCR2 捕获），将 CCER_CC2P 写 1，CCER_CC1NP 写 0，选择 CH1 上的有效转换边沿为下降沿。
5. 设置从模式控制信号为 CH1，向 SMCR_TS 写入 101(0x5)，选择 TI1FP1。
6. 将从模式控制器配置为复位模式，向 SMCR_SMS 写入 0100(0x4)。
7. 使能通道 1 和通道 2，将 CCER_CC1E 和 CCER_CC2E 置 1。

配置完成后，在每个 CH1 的上升沿，计数器的值被记录在 CCR1 中，同时计数器被复位并重新开始计数；在每个 CH1 的下降沿，计数器的值被记录在 CCR2 中。将 CCR1 的值乘以 PCLK 的周期，可以算出 PWM 的周期。将 CCR2 的值乘以 PCLK 的周期，可以算出 PWM 高电平持续的时间，从而得到 PWM 的占空比。

9.1.3.9 输出比较模式

在输出比较模式下，当计数值与 CCRx 满足一定关系时，可以在对应 CHx 及 CHxN 上产生特定输出，通常用于控制输出波形，或指示已经过某一时间段。

具体而言，通道将在 CCRx 与计数器之间相匹配时执行下列操作：

1. 将为相应的 CHx 和 CHxN 输出分配一个可编程值，该值由比较模式寄存器 CCMRx_OCxM 和输出极性寄存器 CCER_CCxP/CCxNP 定义。匹配时，输出引脚既可保持其电平（CCMRx_OCxM=0000），也可设置为有效电平 (CCMRx_OCxM=0001)、无效电平 (CCMRx_OCxM=0010) 或进行翻转 (CCMRx_OCxM=0011)。
2. 将中断状态寄存器标志 SR_CCxIF 置 1。
3. 根据 CCER_CC1IE 生成中断。
4. 根据 DIER_CC1DE 和 CR2_CCDS 生成 DMA 请求。

配置 CCMRx_OCxPE，可将 CCRx 寄存器配置为带或不带影子寄存器。当 CCMRx_OCxPE 为 0 时，软件修改 CCRx 实时生效，可通过在每次中断中修改下一次匹配的 CCRx 来实现自定义波形的输出。

将 BDTR_MOE 设为 1 后 CH 和 CHxN 输出才生效。

9.1.3.10 基础 PWM 输出

利用输出比较模式，定时器可以产生周期、占空比、相位可控的多路 PWM 输出。PWM 输出的周期由 ARR 决定，占空比由 CCRx 决定。PWM 输出有多种模式，由每个通道的 CCMRx_OCxM 各自独立选择。最基本的单路 PWM 输出只需要占用一个通道，采用基础的 PWM 模式即可实现。复杂的 PWM 信号，或 PWM 组合则需要占用多个通道，并需仔细分配每个通道的 PWM 模式以及 CCRx。

在基础的 PWM 模式下，计数器值 CNT 与 CCRx 进行比较，并根据计数器的当前计数方向产生包含有效电平或无效电平的比较输出信号 OCxREF。有效电平的极性可通过 CCER_CCxP 配置，并根据 CCER_CCxE 和 BDTR_MOE 等寄存器使能 CHx 输出。将 BDTR_MOE 设为 1 后 PWM 输出才生效。

如在递增计数模式下，配置 CCMR1_OC1M 和 CCMR1_OC2M 为 0110(0x6)，则 PWM 输出如图9-2。其中计数值 CNT 小于 CCR1/2 时，输出高电平，否则输出低电平。

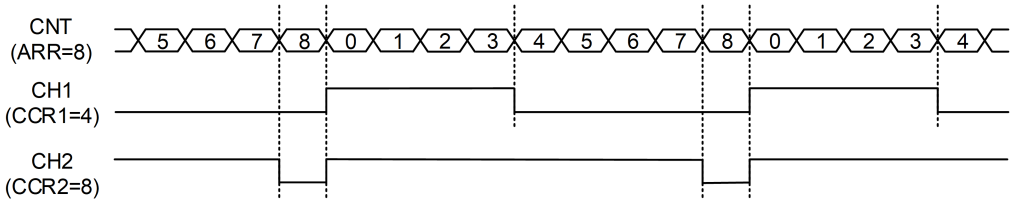


图 9-2: 递增计数模式下的 PWM 输出

如在中心对齐计数模式下，配置 CCMR1_OC1M 和 CCMR1_OC2M 为 0110(0x6)，则 PWM 输出如图9-3。其中递增阶段计数值 CNT 小于 CCR1/2 时，输出高电平，否则输出低电平；递减阶段计数值 CNT 大于 CCR1/2 时，输出低电平，否则输出高电平。

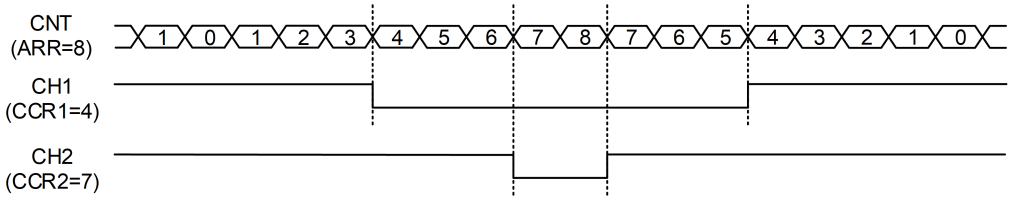


图 9-3: 中心对齐计数模式下的 PWM 输出

9.1.3.11 不对称 PWM 输出

在不对称 PWM 模式下，生成的两个 PWM 信号之间存在可编程相移。该模式仅限于计数器处于中心对齐模式时。生成的两个 PWM 信号频率相同，由 ARR 的值确定，而占空比和相移则各由一对 CCRx 寄存器确定。每一路输出 PWM 占用两个 CCRx 寄存器，分别控制递增计数和递减计数期间的行为，这样 PWM 的上升沿和下降沿时间点可以分别配置。CCR1 和 CCR2 共同控制 CH1/2 的输出，CCR3 和 CCR4 共同控制 CH3/4 的输出。

CH1/2 以及 CH3/4 可以独立选择不同的不对称 PWM 模式，配置 CCMRx_OCxM 为 1110(0xe) 或 1111(0xf)。

如配置 CCMR1_OC1M 和 CCMR2_OC3M 为 1110(0xe)，则 PWM 输出如图9-4。其中递增阶段 (0->ARR-1) 计数值 CNT 小于 CCR1/3 时，输出高电平，否则输出低电平；递减阶段 (ARR->1) 计数值 CNT 大于 CCR2/4 时，输出低电平，否则输出高电平。

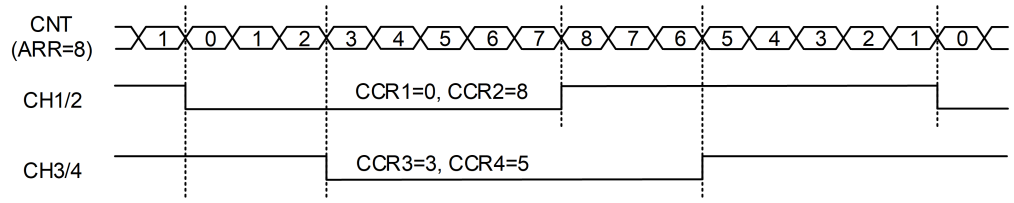


图 9-4: 不对称 PWM 输出

9.1.3.12 组合 PWM 输出

在组合 PWM 模式下，生成的两个 PWM 信号之间存在可编程延时和相移。计数器处于递增、递减或中心对齐模式均可，生成的两个 PWM 信号频率相同，由 ARR 的值确定，而占空比和相移则各由一对 CCRx 寄存器确定。每一路输出 PWM 占用两个 CCRx 寄存器，是由两路基础 PWM 输出波形的逻辑与运算或者逻辑或运算组合而成。CCR1 和 CCR2 共同控制 CH1/2 的输出，CCR3 和 CCR4 共同控制 CH3/4 的输出。

CH1/2 以及 CH3/4 可以独立选择不同的组合 PWM 模式，配置 CCMRx_OCxM 为 1100(0xc) 或 1101(0xd)。当 CH1 或 CH3 配置为组合 PWM 模式 1100(0xc) 时，CH2 或 CH4 必须配置为 0111(0x7) 或 1101(0xd) 或 1111(0xf)。当 CH1 或 CH3 配置为组合 PWM 模式 1101(0xd) 时，CH2 或 CH4 必须配置为 0110(0x6) 或 1100(0xc) 或 1110(0xe)。

如配置 CCMR1_OC1M 为 1101(0xd)，CCMR1_OC2M 为 0110(0x6)，CCMR2_OC3M 为 1100(0xc)，CCMR2_OC4M 为 0111(0x7)，则 PWM 输出如图9-5。其中计数值 CNT 小于 CCR1/4 时，OC1REF/OC4REF 为低电平，否则为高电平；计数值 CNT 小于 CCR2/3 时，OC2REF/OC3REF 为高电平，否则为低电平。CH1 输出是 OC1REF 和 OC2REF 的逻辑与运算。CH3 输出是 OC3REF 和 OC4REF 的逻辑或运算。

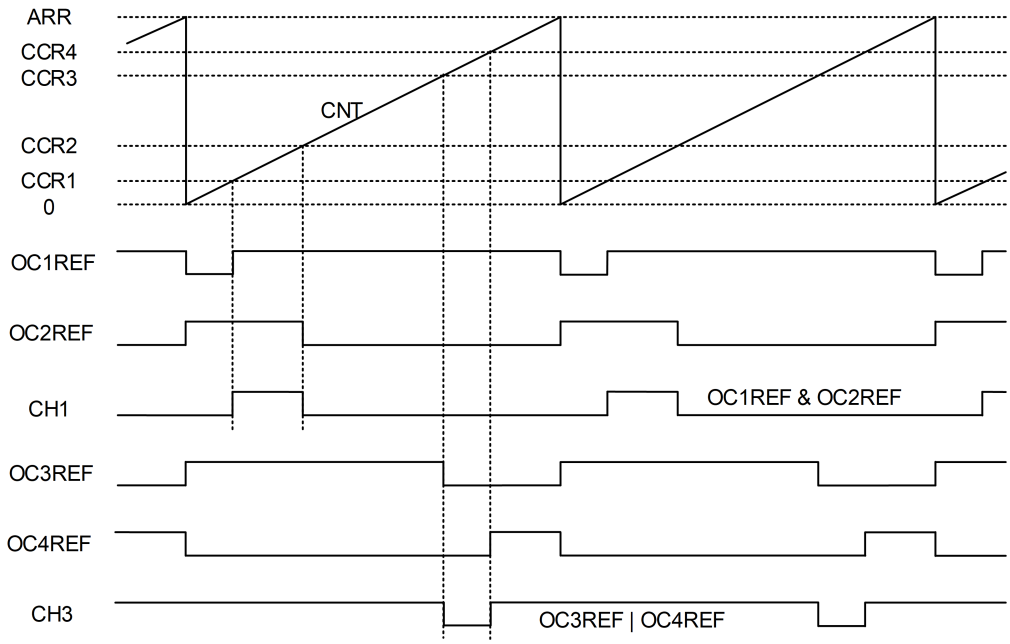


图 9-5: 组合 PWM 输出

9.1.3.13 带死区的互补 PWM 输出

ATIM 可以输出两路相位相反的互补 PWM 信号 CHx 与 CHxN，并在两路信号跳变的边沿插入一定延时。这段延时通常称为死区，用户必须根据与输出相连接的器件及其特性（如电平转换器的固有延迟、开关器件产生的延迟等）来调整死区时间。

ATIM 的通道 1/2/3 每个均可输出一组互补 PWM 信号，最多可同时输出 3 组共 6 路互补信号。其中每路输出可以通过 CCER_CCxP 和 CCER_CCxNP 独立选择输出极性。将 BDTR_MOE 以及对应通道的 CCER_CCxE 和 CCER_CCxNE 配置成 1 使能互补输出。

互补输出的示例如图9-6。CHx 的上升沿相对该通道产生的参考输出 OCxREF 的上升沿有一个死区时间的延时，而 CHxN 的上升沿相对该通道的 OCxREF 的下降沿有一个死区时间的延时。

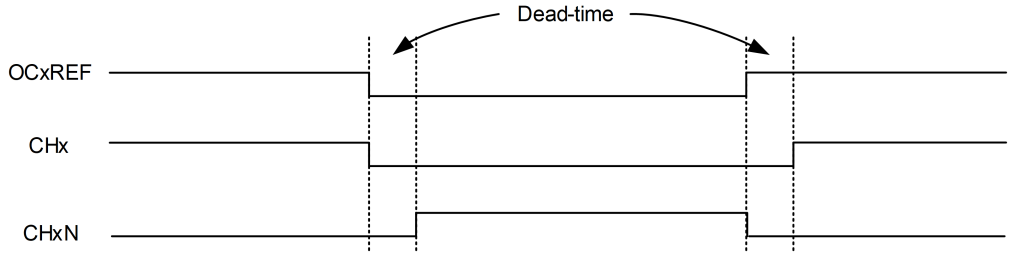


图 9-6: 带死区的互补 PWM 输出

死区时间在一定范围内可调节。当 BDTR_DTPSC 为 0 时，死区时间为 BDTR_DTG 乘以 PCLK 周期。当 BDTR_DTPSC 为 1 时，死区时间为 BDTR_DTG 乘以 16 倍 PCLK 周期。假如 PCLK 为 120MHz，死区时间可调范围为 0~136us。

9.1.3.14 紧急断路

断路功能的目的是保护由 ATIM 产生的 PWM 信号所驱动的功率开关。两个断路输入 BKIN 和 BKIN2 通常连接到功率级和三相逆变器的故障输出。激活时，断路电路会关闭 PWM 输出，并将其强制为预定义的安全状态。也可选择一些芯片内部事件来触发输出关断。BKIN 可以在死区持续时间后将输出强制为预定义的电平（有效或无效）。BKIN 能够将输出强制为无效状态。

断路期间的输出使能信号和输出电平取决于多个控制位：BDTR_MOE 允许通过软件使能/禁止输出；BDTR_OSSI 定义定时器将输出控制在无效状态下，还是释放控制权给 GPIO 控制器（通常使其处于高阻态模式）；CR2_OISx/OISxN 将输出设置为关断电平（有效或无效）。

ATIM 复位后，断路功能处于禁止状态，BDTR_MOE 处于低电平。将 BDTR_BKE/BKE2 置 1，可使能断路功能。可通过配置 BDTR_BKP/BKP2 选择断路输入的极性。也可由软件配置 EGR_BG/B2G 产生断路事件，不依赖于 BDTR_BKE/BKE2 的值。

断路电路内部还实施了写保护，用以保护应用的安全。通过该功能，用户可冻结多个参数配置，如死区持续时间、输出极性和禁止时的状态、PWM 模式、断路使能和极性等。该功能通过写 AF1_LOCK 寄存器实现，从 3 种保护级别中进行选择。

9.1.3.15 6 步 PWM

6 步 PWM 需要在 PWM 输出过程中的某一时刻同时切换各通道的 PWM 模式，可以通过 ATIM 的换向事件 (COM) 实现。当通道使用互补输出时，CCMRx_OCxM、CCER_CCxE 和 CCER_CCxNE 有预装载机制。用户可以预先编程下一步骤的配置，当发生换向事件时，预装载寄存器将传输到影子寄存器，同时更改所有通道的配置。COM 可由软件通过将 EGR_COM 置 1 生成，也可以由硬件在输入触发信号的上升沿生成。发生换向事件时，SR_COMIF 将会置 1。这时，如果 DIER_COMIE 为 1，将产生中断；如果 DIER_COMDE 为 1，将产生 DMA 请求。

9.1.3.16 单脉冲模式

将 CR1_OPM 写 1 可以使能单脉冲模式。该模式下计数器启动以后一旦发生更新事件，就会自动停止计数。该模式可以用于单次计数，或在一个激励信号的触发下启动，并在一段可编程的延时后产生一个脉宽可编程的脉冲。

例如，希望实现这样的功能，在 CH2 输入引脚检测到上升沿时，经过一定时间延迟，在 CH1 上产生单个一定宽度的正脉冲。配置方法如下：

1. CCMR1_CC2S=01，以将 TI2FP2 映射到通道 2。
2. CCER_CCxP 和 CCER_CCxNP 写 0，TI2FP2 反应 CH2 上升沿的变化。
3. SMCR_TS=110(0x6)，将 TI2FP2 配置为从模式控制器的触发 TRGI。
4. SMCR_SMS=110(0x6)，将从模式控制器配置为触发模式，触发后开启计数。
5. 根据需要的时间延迟与脉冲宽度配置 ARR 与 CCR1，定义时间延迟与脉冲宽度。
6. CCMR1_OC1M=0111(0x7)，配置为正脉冲 PWM。
7. CR1_OPM=1，一次触发只产生一个脉冲。
8. EGR_UG=1，手动刷新 ARR 与 CCR1 寄存器。

从模式为触发模式时不需要手动使能 CR1_CEN，一旦检测到触发信号生效，计数器就会自动使能。

9.1.3.17 编码器接口模式

编码器接口模式下，通道 1 和通道 2 可以用于连接外部正交编码器，将外部编码器的信号转化为定时器的计数值变化，从而获知外部编码器的工作状态。

如果计数器仅在 CH1 边沿处计数，SMCR_SMS 配置为 0001；如果计数器仅在 CH2 边沿处计数，SMCR_SMS 配置为 0010(0x2)；如果计数器在 CH1 和 CH2 边沿处均计数，SMCR_SMS 配置为 0011(0x3)。CCER_CC1P/CC2P 用于选择 CH1 和 CH2 极性。如果需要，还可对输入滤波器进行编程。两个输入的信号转换序列会产生计数脉冲和方向信号，根据该信号转换序列，计数器相应递增或递减计数，同时硬件对 CR1_DIR 进行相应修改。

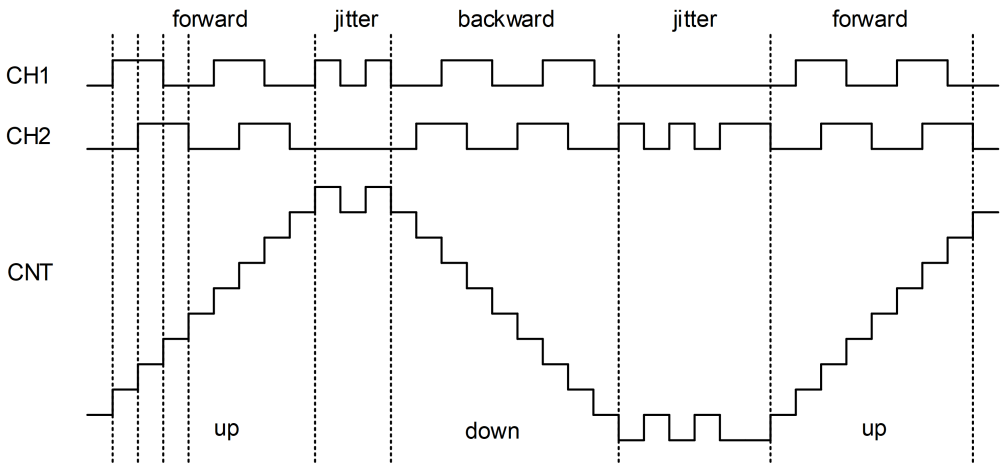
编码器接口模式下，计数器的计数事件是正交编码器接口的解码输出。计数器仅在 0 到 ARR 之间进行连续计数（根据计数的具体方向，从 0 递增计数到 ARR，或从 ARR 递减计数到 0）。因此，在启动前必须先配置 ARR。同样，捕获、比较、重复计数器和触发输出功能继续正常工作。在此模式下，计数器会根据正交编码器的速度和方向自动进行修改，因此，其内容始终表示编码器的位置。计数方向对应于所连传感器的旋转方向。下表汇总了可能的组合（假设 CH1 和 CH2 不同时切换）。

SMCR_SMS	条件	CH1 上升沿	CH1 上升沿	CH2 上升沿	CH2 上升沿
0001 或 0011	CH2=0	递增	递减	/	/
	CH2=1	递减	递增	/	/
0010 或 0011	CH1=0	/	/	递减	递增
	CH1=1	/	/	递增	递减

下图示意了计数器如何根据正交编码器的信号变化进行计数的，配置如下：

CCMR1_CC1S=01（CH1 映射到通道 1 上），CCMR2_CC2S=01（CH2 映射到通道 2 上），

CCER_CC1P/CC1NP/CC2P/CC2NP=0，SMCR_SMS=0011(0x3)，CR1_CEN=1。



9.1.3.18 定时器同步

多个定时器可通过主从模式连接在一起，实现定时器同步，以完成多级分频、同时启动、门控计数等功能。

将主模式定时器的 TRGO 设置为更新事件 (CR2_MMS=010)，连接至另一个设置为外部时钟从模式 (SMCR_SMS = 0111) 的定时器，可以实现定时器级联计数。此时主模式定时器相当于从模式定时器的预分频，计数总位宽等

于两个定时器各自的位宽相加。

将主模式定时器的 TRGO 设置为计数使能 (CR2_MMS=001)，连接至另一个设置为触发从模式 (SMCR_SMS=0110) 的定时器，可以实现定时器同步启动，从而对齐多个定时器的开启时机。

将主模式定时器的 TRGO 设置为比较输出 (CR2_MMS=100)，连接至另一个设置为门控从模式 (SMCR_SMS=0101) 的定时器，可以实现门控 PWM 输出。主模式定时器可以对从模式定时器输出的 PWM 载波进行调制输出。

9.1.3.19 通知机制

ATIM 能够产生中断、DMA 请求、PTC 触发等多种通知机制。能够触发通知的事件主要包括更新事件、触发事件、比较器匹配、输入捕获、断路输入、换向事件等。DIER 寄存器可以控制各种事件是否产生中断和 DMA 请求。各事件状态可在 SR 寄存器中查询。

9.1.4 ATIM 寄存器

表 9-1: ATIM 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00			**CR1**	TIM control register 1
[31:12]			RSVD	
[11]	rw	1'h0	UIFREMAP	UIF status bit remapping 0: No remapping. UIF status bit is not copied to CNT register bit 31 1: Remapping enabled. UIF status bit is copied to CNT register bit 31.
[10:8]			RSVD	
[7]	rw	1'h0	ARPE	Auto-reload preload enable 0: ARR register is not buffered 1: ARR register is buffered
[6:5]	rw	2'h0	CMS	Center-aligned mode selection 00: Edge-aligned mode. The counter counts up or down depending on the direction bit (DIR). 01: Center-aligned mode 1. The counter counts up and down alternatively. Output compare interrupt flags of channels configured in output (CCxS=00 in CCMRx register) are set only when the counter is counting down. 10: Center-aligned mode 2. The counter counts up and down alternatively. Output compare interrupt flags of channels configured in output (CCxS=00 in CCMRx register) are set only when the counter is counting up. 11: Center-aligned mode 3. The counter counts up and down alternatively. Output compare interrupt flags of channels configured in output (CCxS=00 in CCMRx register) are set both when the counter is counting up or down.
[4]	rw	1'h0	DIR	Direction 0: Counter used as upcounter 1: Counter used as downcounter
[3]	rw	1'h0	OPM	One-pulse mode 0: Counter is not stopped at update event 1: Counter stops counting at the next update event (clearing the bit CEN)

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表 9-1: ATIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[2]	rw	1'h0	URS	Update request source This bit is set and cleared by software to select the UEV event sources. 0: Any of the following events generate an update interrupt or DMA request if enabled. These events can be: Counter overflow/underflow Setting the UG bit Update generation through the slave mode controller 1: Only counter overflow/underflow generates an update interrupt or DMA request if enabled.
[1]	rw	1'h0	UDIS	Update disable This bit is set and cleared by software to enable/disable UEV event generation. 0: UEV enabled. The Update (UEV) event is generated by one of the following events: Counter overflow/underflow Setting the UG bit Update generation through the slave mode controller Buffered registers are then loaded with their preload values. 1: UEV disabled. The Update event is not generated, shadow registers keep their value (ARR, PSC, CCRx). However the counter and the prescaler are reinitialized if the UG bit is set or if a hardware reset is received from the slave mode controller.
[0]	rw	1'h0	CEN	Counter enable 0: Counter disabled 1: Counter enabled External clock, gated mode and encoder mode can work only if the CEN bit has been previously set by software. However trigger mode can set the CEN bit automatically by hardware. CEN is cleared automatically in one-pulse mode, when an update event occurs.
0x04			**CR2**	TIM control register 2
[31:19]			RSVD	
[18]	rw	1'h0	OIS6	Output Idle state 6 (OC6 output)
[17]			RSVD	
[16]	rw	1'h0	OIS5	Output Idle state 5 (OC5 output)
[15]			RSVD	
[14]	rw	1'h0	OIS4	Output Idle state 4 (OC4 output)
[13]	rw	1'h0	OIS3N	Output Idle state 3 (OC3N output)
[12]	rw	1'h0	OIS3	Output Idle state 3 (OC3 output)
[11]	rw	1'h0	OIS2N	Output Idle state 2 (OC2N output)
[10]	rw	1'h0	OIS2	Output Idle state 2 (OC2 output)
[9]	rw	1'h0	OIS1N	Output Idle state 1 (OC1N output) 0: OC1N=0 after a dead-time when MOE=0 1: OC1N=1 after a dead-time when MOE=0 This bit, as well as other OISxN, can not be modified as long as LOCK level 1, 2 or 3 has been programmed
[8]	rw	1'h0	OIS1	Output Idle state 1 (OC1 output) 0: OC1=0 (after a dead-time if OC1N is implemented) when MOE=0 1: OC1=1 (after a dead-time if OC1N is implemented) when MOE=0 This bit, as well as other OISx, can not be modified as long as LOCK level 1, 2 or 3 has been programmed

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表 9-1: ATIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[7]	rw	1'h0	TI1S	TI1 selection 0: The CH1 pin is connected to TI1 input 1: The CH1, CH2 and CH3 pins are connected to the TI1 input (XOR combination)
[6:4]	rw	3'h0	MMS	Master mode selection These bits allow to select the information to be sent in master mode to slave timers for synchronization (TRGO). The combination is as follows: 000: Reset - the UG bit from the EGR register is used as trigger output (TRGO). If the reset is generated by the trigger input (slave mode controller configured in reset mode) then the signal on TRGO is delayed compared to the actual reset. 001: Enable - the Counter enable signal, CNT_EN, is used as trigger output (TRGO). It is useful to start several timers at the same time or to control a window in which a slave timer is enabled. The Counter Enable signal is generated by a logic OR between CEN control bit and the trigger input when configured in gated mode. When the Counter Enable signal is controlled by the trigger input, there is a delay on TRGO, except if the master/slave mode is selected. 010: Update - The update event is selected as trigger output (TRGO). For instance a master timer can then be used as a prescaler for a slave timer. 011: Compare Pulse - The trigger output send a positive pulse when the CC1IF flag is to be set (even if it was already high), as soon as a capture or a compare match occurred. (TRGO) 100: Compare - OC1REFC signal is used as trigger output (TRGO) 101: Compare - OC2REFC signal is used as trigger output (TRGO) 110: Compare - OC3REFC signal is used as trigger output (TRGO) 111: Compare - OC4REFC signal is used as trigger output (TRGO)
[3]	rw	1'h0	CCDS	Capture/compare DMA selection 0: CCx DMA request sent when CCx event occurs 1: CCx DMA requests sent when update event occurs
[2]	rw	1'h0	CCUS	Capture/compare control update selection 0: When capture/compare control bits are preloaded (CCPC=1), they are updated by setting the COMG bit only 1: When capture/compare control bits are preloaded (CCPC=1), they are updated by setting the COMG bit or when an edge occurs on TRGI after Trigger selection This bit acts only on channels that have a complementary output.
[1]			RSVD	
[0]	rw	1'h0	CCPC	Capture/compare preloaded control 0: CCxE, CCxNE and OCxM bits are not preloaded 1: CCxE, CCxNE and OCxM bits are preloaded, after having been written, they are updated only when a commutation event (COM) occurs (COMG bit set or edge detected on TRGI after Trigger selection, depending on the CCUS bit). This bit acts only on channels that have a complementary output.
0x08			**SMCR**	TIM slave mode control register
[31:20]			RSVD	

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表 9-1: ATIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[19:16]	rw	4'h0	SMS	Slave mode selection When external signals are selected the active edge of the trigger signal (TRGI) is linked to the polarity selected on the external input. 0000: Slave mode disabled. 0001: Encoder mode 1 - Counter counts up/down on TI1FP1 edge depending on TI2FP2 level. 0010: Encoder mode 2 - Counter counts up/down on TI2FP2 edge depending on TI1FP1 level. 0011: Encoder mode 3 - Counter counts up/down on both TI1FP1 and TI2FP2 edges depending on the level of the other input. 0100: Reset Mode - Rising edge of the selected trigger input (TRGI) reinitializes the counter and generates an update of the registers. 0101: Gated Mode - The counter clock is enabled when the trigger input (TRGI) is high. The counter stops (but is not reset) as soon as the trigger becomes low. Both start and stop of the counter are controlled. 0110: Trigger Mode - The counter starts at a rising edge of the trigger TRGI (but it is not reset). Only the start of the counter is controlled. 0111: External Clock Mode 1 - Rising edges of the selected trigger (TRGI) clock the counter. 1000: Combined reset + trigger mode - Rising edge of the selected trigger input (TRGI) reinitializes the counter, generates an update of the registers and starts the counter.
[15]	rw	1'h0	ETP	External trigger polarity This bit selects whether ETR or ETR is used for trigger operations 0: ETR is non-inverted, active at high level or rising edge 1: ETR is inverted, active at low level or falling edge
[14]	rw	1'h0	ECE	External clock enable This bit enables External clock mode 2. 0: External clock mode 2 disabled 1: External clock mode 2 enabled. The counter is clocked by any active edge on the ETRF signal.
[13:12]	rw	2'h0	ETPS	External trigger prescaler External trigger signal ETRP frequency must be at most 1/4 of CK_INT frequency. A prescaler can be enabled to reduce ETRP frequency. It is useful when inputting fast external clocks. 00: Prescaler OFF 01: ETRP frequency divided by 2 10: ETRP frequency divided by 4 11: ETRP frequency divided by 8

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表 9-1: ATIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[11:8]	rw	4'h0	ETF	External trigger filter This bit-field then defines the frequency used to sample ETRP signal and the length of the digital filter applied to ETRP. The digital filter is made of an event counter in which N consecutive events are needed to validate a transition on the output: 0000: No filter, sampling is done at fCLK 0001: fSAMPLING=fCLK, N=2 0010: fSAMPLING=fCLK, N=4 0011: fSAMPLING=fCLK, N=8 0100: fSAMPLING=fCLK/2, N=6 0101: fSAMPLING=fCLK/2, N=8 0110: fSAMPLING=fCLK/4, N=6 0111: fSAMPLING=fCLK/4, N=8 1000: fSAMPLING=fCLK/8, N=6 1001: fSAMPLING=fCLK/8, N=8 1010: fSAMPLING=fCLK/16, N=5 1011: fSAMPLING=fCLK/16, N=6 1100: fSAMPLING=fCLK/16, N=8 1101: fSAMPLING=fCLK/32, N=5 1110: fSAMPLING=fCLK/32, N=6 1111: fSAMPLING=fCLK/32, N=8
[7]	rw	1'h0	MSM	Master/Slave mode 0: No action 1: The effect of an event on the trigger input (TRGI) is delayed to allow a perfect synchronization between the current timer and its slaves (through TRGO). It is useful if we want to synchronize several timers on a single external event.
[6:4]	rw	3'h0	TS	Trigger selection This bit-field selects the trigger input to be used to synchronize the counter. 000: Internal Trigger 0 (ITR0) 001: Internal Trigger 1 (ITR1) 010: Internal Trigger 2 (ITR2) 011: Internal Trigger 3 (ITR3) 100: TI1 Edge Detector (TI1F_ED) 101: Filtered Timer Input 1 (TI1FP1) 110: Filtered Timer Input 2 (TI2FP2) 111: External Trigger input (ETRF)
[3:0]			RSVD	
0x0C			**DIER**	TIM DMA/Interrupt enable register
[31:18]			RSVD	
[17]	rw	1'h0	CC6IE	Capture/Compare 6 interrupt enable 0: CC6 interrupt disabled. 1: CC6 interrupt enabled
[16]	rw	1'h0	CC5IE	Capture/Compare 5 interrupt enable 0: CC5 interrupt disabled. 1: CC5 interrupt enabled
[15]			RSVD	
[14]	rw	1'h0	TDE	Trigger DMA request enable 0: Trigger DMA request disabled. 1: Trigger DMA request enabled.

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表 9-1: ATIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[13]	rw	1'h0	COMDE	COM DMA request enable 0: COM DMA request disabled 1: COM DMA request enabled
[12]	rw	1'h0	CC4DE	Capture/Compare 4 DMA request enable 0: CC4 DMA request disabled. 1: CC4 DMA request enabled
[11]	rw	1'h0	CC3DE	Capture/Compare 3 DMA request enable 0: CC3 DMA request disabled. 1: CC3 DMA request enabled.
[10]	rw	1'h0	CC2DE	Capture/Compare 2 DMA request enable 0: CC2 DMA request disabled. 1: CC2 DMA request enabled.
[9]	rw	1'h0	CC1DE	Capture/Compare 1 DMA request enable 0: CC1 DMA request disabled. 1: CC1 DMA request enabled.
[8]	rw	1'h0	UDE	Update DMA request enable 0: Update DMA request disabled. 1: Update DMA request enabled
[7]	rw	1'h0	BIE	Break interrupt enable 0: Break interrupt disabled 1: Break interrupt enabled
[6]	rw	1'h0	TIE	Trigger interrupt enable 0: Trigger interrupt disabled. 1: Trigger interrupt enabled
[5]	rw	1'h0	COMIE	COM interrupt enable 0: COM interrupt disabled 1: COM interrupt enabled
[4]	rw	1'h0	CC4IE	Capture/Compare 4 interrupt enable 0: CC4 interrupt disabled. 1: CC4 interrupt enabled
[3]	rw	1'h0	CC3IE	Capture/Compare 3 interrupt enable 0: CC3 interrupt disabled. 1: CC3 interrupt enabled
[2]	rw	1'h0	CC2IE	Capture/Compare 2 interrupt enable 0: CC2 interrupt disabled. 1: CC2 interrupt enabled.
[1]	rw	1'h0	CC1IE	Capture/Compare 1 interrupt enable 0: CC1 interrupt disabled. 1: CC1 interrupt enabled
[0]	rw	1'h0	UIE	Update interrupt enable 0: Update interrupt disabled. 1: Update interrupt enabled
0x10			**SR**	TIM status register
[31:18]			RSVD	
[17]	rw0c	1'h0	CC6IF	Compare 6 interrupt flag
[16]	rw0c	1'h0	CC5IF	Compare 5 interrupt flag
[15]			RSVD	
[14]			RSVD	

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表 9-1: ATIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[13]	rw0c	1'h0	SBIF	System Break interrupt flag This flag is set by hardware as soon as the system break input goes active. It can be cleared by software if the system break input is not active. This flag must be reset to re-start PWM operation. 0: No break event occurred. 1: An active level has been detected on the system break input. An interrupt is generated if BIE=1 in the DIER register.
[12]	rw0c	1'h0	CC4OF	Capture/Compare 4 overcapture flag
[11]	rw0c	1'h0	CC3OF	Capture/Compare 3 overcapture flag
[10]	rw0c	1'h0	CC2OF	Capture/Compare 2 overcapture flag
[9]	rw0c	1'h0	CC1OF	Capture/Compare 1 overcapture flag This flag is set by hardware only when the corresponding channel is configured in input capture mode. It is cleared by software by writing it to '0'. 0: No overcapture has been detected. 1: The counter value has been captured in CCR1 register while CC1IF flag was already set
[8]	rw0c	1'h0	B2IF	Break 2 interrupt flag This flag is set by hardware as soon as the break 2 input goes active. It can be cleared by software if the break 2 input is not active. 0: No break event occurred. 1: An active level has been detected on the break 2 input. An interrupt is generated if BIE=1 in the DIER register.
[7]	rw0c	1'h0	BIF	Break interrupt flag This flag is set by hardware as soon as the break input goes active. It can be cleared by software if the break input is not active. 0: No break event occurred. 1: An active level has been detected on the break input. An interrupt is generated if BIE=1 in the DIER register.
[6]	rw0c	1'h0	TIF	Trigger interrupt flag This flag is set by hardware on trigger event. It is set when the counter starts or stops when gated mode is selected. It is cleared by software. 0: No trigger event occurred. 1: Trigger interrupt pending.
[5]	rw0c	1'h0	COMIF	COM interrupt flag This flag is set by hardware on COM event (when Capture/compare Control bits - CCxE, CCxNE, OCxM - have been updated). It is cleared by software. 0: No COM event occurred. 1: COM interrupt pending.
[4]	rw0c	1'h0	CC4IF	Capture/Compare 4 interrupt flag
[3]	rw0c	1'h0	CC3IF	Capture/Compare 3 interrupt flag
[2]	rw0c	1'h0	CC2IF	Capture/Compare 2 interrupt flag

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表 9-1: ATIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[1]	rw0c	1'h0	CC1IF	Capture/Compare 1 interrupt flag If channel CC1 is configured as output: This flag is set by hardware when the counter matches the compare value and in retriggerable one pulse mode. It is cleared by software. 0: No match. 1: The content of the counter CNT has matched the content of the CCR1 register. If channel CC1 is configured as input: This bit is set by hardware on a capture. It is cleared by software or by reading the CCR1 register. 0: No input capture occurred. 1: The counter value has been captured in CCR1 register.
[0]	rw0c	1'h0	UIF	Update interrupt flag This bit is set by hardware on an update event. It is cleared by software. 0: No update occurred 1: Update interrupt pending. This bit is set by hardware when the registers are updated: - At overflow or underflow regarding the repetition counter value (update if repetition counter = 0) and if UDIS=0 in the CR1 register. - When CNT is reinitialized by software using the UG bit in EGR register, if URS=0 and UDIS=0 in the CR1 register. - When CNT is reinitialized by a trigger event, if URS=0 and UDIS=0 in the CR1 register.
0x14			**EGR**	Event generation register
[31:9]			RSVD	
[8]	w	1'h0	B2G	Break 2 generation This bit is set by software in order to generate an event, it is automatically cleared by hardware. 0: No action 1: A break 2 event is generated. MOE bit is cleared and B2IF flag is set. Related interrupt can occur if enabled.
[7]	w	1'h0	BG	Break generation This bit is set by software in order to generate an event, it is automatically cleared by hardware. 0: No action 1: A break event is generated. MOE bit is cleared and BIF flag is set. Related interrupt or DMA transfer can occur if enabled.
[6]	w	1'h0	TG	Trigger generation This bit is set by software in order to generate an event, it is automatically cleared by hardware. 0: No action 1: The TIF flag is set in SR register. Related interrupt or DMA transfer can occur if enabled.
[5]	w	1'h0	COMG	Capture/Compare control update generation This bit can be set by software, it is automatically cleared by hardware 0: No action 1: When CCPC bit is set, it allows to update CCxE, CCxNE and OCxM bits This bit acts only on channels having a complementary output.
[4]	w	1'h0	CC4G	Capture/compare 4 generation
[3]	w	1'h0	CC3G	Capture/compare 3 generation
[2]	w	1'h0	CC2G	Capture/compare 2 generation

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表 9-1: ATIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[1]	w	1'h0	CC1G	Capture/compare 1 generation This bit is set by software in order to generate an event, it is automatically cleared by hardware. 0: No action 1: A capture/compare event is generated on channel 1: If channel CC1 is configured as output: CC1IF flag is set, Corresponding interrupt or DMA request is sent if enabled. If channel CC1 is configured as input: The current value of the counter is captured in CCR1 register. The CC1IF flag is set, the corresponding interrupt or DMA request is sent if enabled. The CC1OF flag is set if the CC1IF flag was already high.
[0]	w	1'h0	UG	Update generation This bit can be set by software, it is automatically cleared by hardware. 0: No action 1: Re-initialize the counter and generates an update of the registers. The prescaler counter is cleared too (anyway the prescaler ratio is not affected). The counter is cleared if the center-aligned mode is selected or if DIR=0 (upcounting), else it takes the auto-reload value (ARR) if DIR=1 (downcounting).
0x18			**CCMR1**	TIM capture/compare mode register 1
[31:28]	rw	4'h0	OC2M	Output compare 2 mode
[27]	rw	1'h0	OC2PE	Output compare 2 preload enable
[26:25]			RSVD	
[24]	rw	1'h0	OC2CE	Output compare 2 clear enable

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表 9-1: ATIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[23:20]	rw	4'h0	OC1M	Output compare 1 mode These bits define the behavior of the output reference signal OC1REF from which OC1 and OC1N are derived. OC1REF is active high whereas OC1 and OC1N active level depends on CC1P and CC1NP bits. 0000: Frozen - The comparison between the output compare register CCR1 and the counter CNT has no effect on the outputs. 0001: Set channel 1 to active level on match. OC1REF signal is forced high when the counter CNT matches the capture/compare register 1 (CCR1). 0010: Set channel 1 to inactive level on match. OC1REF signal is forced low when the counter CNT matches the capture/compare register 1 (CCR1). 0011: Toggle - OC1REF toggles when CNT=CCR1. 0100: Force inactive level - OC1REF is forced low. 0101: Force active level - OC1REF is forced high. 0110: PWM mode 1 - In upcounting, channel 1 is active as long as CNT<CCR1 else inactive. In downcounting, channel 1 is inactive (OC1REF=0) as long as CNT>CCR1 else active (OC1REF=1). 0111: PWM mode 2 - In upcounting, channel 1 is inactive as long as CNT<CCR1 else active. In downcounting, channel 1 is active as long as CNT>CCR1 else inactive. 1000: Retriggerable OPM mode 1 - In up-counting mode, the channel is active until a trigger event is detected (on TRGI signal). Then, a comparison is performed as in PWM mode 1 and the channels becomes inactive again at the next update. In down-counting mode, the channel is inactive until a trigger event is detected (on TRGI signal). Then, a comparison is performed as in PWM mode 1 and the channels becomes inactive again at the next update. 1001: Retriggerable OPM mode 2 - In up-counting mode, the channel is inactive until a trigger event is detected (on TRGI signal). Then, a comparison is performed as in PWM mode 2 and the channels becomes inactive again at the next update. In down-counting mode, the channel is active until a trigger event is detected (on TRGI signal). Then, a comparison is performed as in PWM mode 1 and the channels becomes active again at the next update. 1010: Reserved, 1011: Reserved, 1100: Combined PWM mode 1 - OC1REF has the same behavior as in PWM mode 1. OC1REFC is the logical OR between OC1REF and OC2REF. 1101: Combined PWM mode 2 - OC1REF has the same behavior as in PWM mode 2. OC1REFC is the logical AND between OC1REF and OC2REF. 1110: Asymmetric PWM mode 1 - OC1REF has the same behavior as in PWM mode 1. OC1REFC outputs OC1REF when the counter is counting up, OC2REF when it is counting down. 1111: Asymmetric PWM mode 2 - OC1REF has the same behavior as in PWM mode 2. OC1REFC outputs OC1REF when the counter is counting up, OC2REF when it is counting down. These bits can not be modified as long as LOCK level 3 has been programmed and CC1S=00 (the channel is configured in output). On channels having a complementary output, this bit field is preloaded. If the CCPC bit is set in the CR2 register then the OC1M active bits take the new value from the preloaded bits only when a COM event is generated.

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表 9-1: ATIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[19]	rw	1'h0	OC1PE	Output compare 1 preload enable 0: Preload register on CCR1 disabled. CCR1 can be written at anytime, the new value is taken in account immediately. 1: Preload register on CCR1 enabled. Read/Write operations access the preload register. CCR1 preload value is loaded in the active register at each update event. These bits can not be modified as long as LOCK level 3 has been programmed and CC1S='00' (the channel is configured in output).
[18:17]			RSVD	
[16]	rw	1'h0	OC1CE	Output compare 1 clear enable 0: OC1Ref is not affected by the ETRF input 1: OC1Ref is cleared as soon as a High level is detected on ETRF input
[15:12]	rw	4'h0	IC2F	Input capture 2 filter
[11:10]	rw	2'h0	IC2PSC	Input capture 2 prescaler
[9:8]	rw	2'h0	CC2S	Capture/Compare 2 selection This bit-field defines the direction of the channel (input/output) as well as the used input. 00: CC2 channel is configured as output 01: CC2 channel is configured as input, IC2 is mapped on TI2 10: CC2 channel is configured as input, IC2 is mapped on TI1 11: CC2 channel is configured as input, IC2 is mapped on TRC. This mode is working only if an internal trigger input is selected through the TS bit (SMCR register)
[7:4]	rw	4'h0	IC1F	Input capture 1 filter This bit-field defines the frequency used to sample TI1 input and the length of the digital filter applied to TI1. The digital filter is made of an event counter in which N consecutive events are needed to validate a transition on the output: 0000: No filter, sampling is done at fCLK 0001: fSAMPLING=fCLK, N=2 0010: fSAMPLING=fCLK, N=4 0011: fSAMPLING=fCLK, N=8 0100: fSAMPLING=fCLK/2, N=6 0101: fSAMPLING=fCLK/2, N=8 0110: fSAMPLING=fCLK/4, N=6 0111: fSAMPLING=fCLK/4, N=8 1000: fSAMPLING=fCLK/8, N=6 1001: fSAMPLING=fCLK/8, N=8 1010: fSAMPLING=fCLK/16, N=5 1011: fSAMPLING=fCLK/16, N=6 1100: fSAMPLING=fCLK/16, N=8 1101: fSAMPLING=fCLK/32, N=5 1110: fSAMPLING=fCLK/32, N=6 1111: fSAMPLING=fCLK/32, N=8

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表 9-1: ATIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[3:2]	rw	2'h0	IC1PSC	Input capture 1 prescaler This bit-field defines the ratio of the prescaler acting on CC1 input (IC1). The prescaler is reset as soon as CC1E=0 (CCER register). 00: no prescaler, capture is done each time an edge is detected on the capture input 01: capture is done once every 2 events 10: capture is done once every 4 events 11: capture is done once every 8 events
[1:0]	rw	2'h0	CC1S	Capture/Compare 1 selection This bit-field defines the direction of the channel (input/output) as well as the used input. 00: CC1 channel is configured as output 01: CC1 channel is configured as input, IC1 is mapped on TI1 10: CC1 channel is configured as input, IC1 is mapped on TI2 11: CC1 channel is configured as input, IC1 is mapped on TRC. This mode is working only if an internal trigger input is selected through TS bit (SMCR register)
0x1C			**CCMR2**	TIM capture/compare mode register 2
[31:28]	rw	4'h0	OC4M	Output compare 4 mode
[27]	rw	1'h0	OC4PE	Output compare 4 preload enable
[26:25]			RSVD	
[24]	rw	1'h0	OC4CE	Output compare 4 clear enable
[23:20]	rw	4'h0	OC3M	Output compare 3 mode
[19]	rw	1'h0	OC3PE	Output compare 3 preload enable
[18:17]			RSVD	
[16]	rw	1'h0	OC3CE	Output compare 3 clear enable
[15:12]	rw	4'h0	IC4F	Input capture 4 filter
[11:10]	rw	2'h0	IC4PSC	Input capture 4 prescaler
[9:8]	rw	2'h0	CC4S	Capture/Compare 4 selection This bit-field defines the direction of the channel (input/output) as well as the used input. 00: CC4 channel is configured as output 01: CC4 channel is configured as input, IC4 is mapped on TI4 10: CC4 channel is configured as input, IC4 is mapped on TI3 11: CC4 channel is configured as input, IC4 is mapped on TRC. This mode is working only if an internal trigger input is selected through TS bit (SMCR register)
[7:4]	rw	4'h0	IC3F	Input capture 3 filter
[3:2]	rw	2'h0	IC3PSC	Input capture 3 prescaler
[1:0]	rw	2'h0	CC3S	Capture/Compare 3 selection This bit-field defines the direction of the channel (input/output) as well as the used input. 00: CC3 channel is configured as output 01: CC3 channel is configured as input, IC3 is mapped on TI3 10: CC3 channel is configured as input, IC3 is mapped on TI4 11: CC3 channel is configured as input, IC3 is mapped on TRC. This mode is working only if an internal trigger input is selected through TS bit (SMCR register)
0x20			**CCER**	Capture/Compare enable register

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表 9-1: ATIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:22]			RSVD	
[21]	rw	1'h0	CC6P	Capture/Compare 6 output Polarity.
[20]	rw	1'h0	CC6E	Capture/Compare 6 output enable.
[19]			RSVD	
[18]			RSVD	
[17]	rw	1'h0	CC5P	Capture/Compare 5 output Polarity.
[16]	rw	1'h0	CC5E	Capture/Compare 5 output enable.
[15]	rw	1'h0	CC4NP	Capture/Compare 4 complementary output polarity
[14]			RSVD	
[13]	rw	1'h0	CC4P	Capture/Compare 4 output Polarity.
[12]	rw	1'h0	CC4E	Capture/Compare 4 output enable.
[11]	rw	1'h0	CC3NP	Capture/Compare 3 complementary output polarity
[10]	rw	1'h0	CC3NE	Capture/Compare 3 complementary output enable
[9]	rw	1'h0	CC3P	Capture/Compare 3 output Polarity.
[8]	rw	1'h0	CC3E	Capture/Compare 3 output enable.
[7]	rw	1'h0	CC2NP	Capture/Compare 2 complementary output polarity
[6]	rw	1'h0	CC2NE	Capture/Compare 2 complementary output enable
[5]	rw	1'h0	CC2P	Capture/Compare 2 output Polarity.
[4]	rw	1'h0	CC2E	Capture/Compare 2 output enable.
[3]	rw	1'h0	CC1NP	Capture/Compare 1 complementary output polarity CC1 channel configured as output: 0: OC1N active high. 1: OC1N active low. CC1 channel configured as input: This bit is used in conjunction with CC1P to define the polarity of TI1FP1 and TI2FP1. Refer to CC1P description. On channels having a complementary output, this bit is preloaded. If the CCPC bit is set in the CR2 register then the CC1NP active bit takes the new value from the preloaded bit only when a Commutation event is generated. This bit as well as other CCxNP is not writable as soon as LOCK level 2 or 3 has been programmed and CC1S=00 (channel configured as output).
[2]	rw	1'h0	CC1NE	Capture/Compare 1 complementary output enable 0: Off - OC1N is not active. OC1N level is then function of MOE, OSSI, OSSR, OIS1, OIS1N and CC1E bits. 1: On - OC1N signal is output on the corresponding output pin depending on MOE, OSSI, OSSR, OIS1, OIS1N and CC1E bits. On channels having a complementary output, this bit is preloaded. If the CCPC bit is set in the CR2 register then the CC1NE active bit takes the new value from the preloaded bit only when a Commutation event is generated.

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表 9-1: ATIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[1]	rw	1'h0	CC1P	Capture/Compare 1 output Polarity. CC1 channel configured as output: 0: OC1 active high 1: OC1 active low CC1 channel configured as input: CC1NP/CC1P bits select TI1FP1 and TI2FP1 polarity for trigger or capture operations. 00: noninverted/rising edge. Circuit is sensitive to TIxFP1 rising edge (capture, trigger in reset, external clock or trigger mode), TIxFP1 is not inverted (trigger in gated mode, encoder mode). 01: inverted/falling edge. Circuit is sensitive to TIxFP1 falling edge (capture, trigger in reset, external clock or trigger mode), TIxFP1 is inverted (trigger in gated mode, encoder mode). 10: reserved, do not use this configuration. 11: noninverted/both edges. Circuit is sensitive to both TIxFP1 rising and falling edges (capture, trigger in reset, external clock or trigger mode), TIxFP1 is not inverted (trigger in gated mode). This configuration must not be used for encoder mode. On channels having a complementary output, this bit is preloaded. If the CCPC bit is set in the CR2 register then the CC1P active bit takes the new value from the preloaded bit only when a Commutation event is generated. This bit as well as other CCxP is not writable as soon as LOCK level 2 or 3 has been programmed.
[0]	rw	1'h0	CC1E	Capture/Compare 1 output enable CC1 channel configured as output: 0: Off - OC1 is not active. OC1 level is then function of MOE, OSSI, OSSR, OIS1, OIS1N and CC1NE bits. 1: On - OC1 signal is output on the corresponding output pin depending on MOE, OSSI, OSSR, OIS1, OIS1N and CC1NE bits. CC1 channel configured as input: This bit determines if a capture of the counter value can actually be done into the input capture/compare register 1 (CCR1) or not. 0: Capture disabled. 1: Capture enabled. On channels having a complementary output, this bit is preloaded. If the CCPC bit is set in the CR2 register then the CC1E active bit takes the new value from the preloaded bit only when a Commutation event is generated.
0x24			**CNT**	Counter
[31:0]	rw	32'h0	CNT	bit 30 to 0 is the lower bits of counter value bit 31 depends on IUFREMAP in CR1. If UIFREMAP = 1 this bit is a read-only copy of the UIF bit of the ISR register If UIFREMAP = 0 this bit is counter value bit 31
0x28			**PSC**	Prescaler
[31:16]			RSVD	
[15:0]	rw	16'h0	PSC	Prescaler value The counter clock frequency is fCLK/(PSC+1). PSC contains the value to be loaded in the active prescaler register at each update event (including when the counter is cleared through UG bit of EGR register or through trigger controller when configured in "reset mode").
0x2C			**ARR**	Auto-reload register

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表 9-1: ATIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:0]	rw	32'h0	ARR	Auto-reload value ARR is the value to be loaded in the actual auto-reload register.
0x30			**RCR**	Repetition counter register
[31:16]			RSVD	
[15:0]	rw	16'h0	REP	Repetition counter value These bits allow the user to set-up the update rate of the compare registers when preload registers are enable, as well as the update interrupt generation rate, if this interrupt is enable. Each time the REP_CNT related downcounter reaches zero, an update event is generated and it restarts counting from REP value. As REP_CNT is reloaded with REP value only at the repetition update event, any write to the RCR register is not taken in account until the next repetition update event. It means in PWM mode (REP+1) corresponds to the number of PWM periods in edge-aligned mode or the number of half PWM period in center-aligned mode..
0x34			**CCR1**	Capture/Compare register 1
[31:0]	rw	32'h0	CCR1	Capture/Compare 1 value If channel CC1 is configured as output: CCR1 is the value to be loaded in the actual capture/compare 1 register (preload value).It is loaded permanently if the preload feature is not selected in the CCMR1 register (bit OC1PE). Else the preload value is copied in the active capture/compare 1 register when an update event occurs. The active capture/compare register contains the value to be compared to the counter CNT and signaled on OC1 output. If channel CC1is configured as input: CCR1 is the counter value transferred by the last input capture 1 event (IC1).
0x38			**CCR2**	Capture/Compare register 2
[31:0]	rw	32'h0	CCR2	Capture/Compare 2 value If channel CC2 is configured as output: CCR2 is the value to be loaded in the actual capture/compare 2 register (preload value).It is loaded permanently if the preload feature is not selected in the CCMR1 register (bit OC2PE). Else the preload value is copied in the active capture/compare 2 register when an update event occurs. The active capture/compare register contains the value to be compared to the counter CNT and signalled on OC2 output. If channel CC2 is configured as input: CCR2 is the counter value transferred by the last input capture 2 event (IC2).
0x3C			**CCR3**	Capture/Compare register 3
[31:0]	rw	32'h0	CCR3	Capture/Compare value If channel CC3 is configured as output: CCR3 is the value to be loaded in the actual capture/compare 3 register (preload value).It is loaded permanently if the preload feature is not selected in the CCMR2 register (bit OC3PE). Else the preload value is copied in the active capture/compare 3 register when an update event occurs. The active capture/compare register contains the value to be compared to the counter CNT and signalled on OC3 output. If channel CC3is configured as input: CCR3 is the counter value transferred by the last input capture 3 event (IC3).
0x40			**CCR4**	Capture/Compare register 4

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表 9-1: ATIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:0]	rw	32'h0	CCR4	Capture/Compare value 1. if CC4 channel is configured as output (CC4S bits): CCR4 is the value to be loaded in the actual capture/compare 4 register (preload value).It is loaded permanently if the preload feature is not selected in the CCMR2 register (bit OC4PE). Else the preload value is copied in the active capture/compare 4 register when an update event occurs. The active capture/compare register contains the value to be compared to the counter CNT and signalled on OC4 output. 2. if CC4 channel is configured as input (CC4S bits in CCMR4 register): CCR4 is the counter value transferred by the last input capture 4 event (IC4).
0x44			**BDTR**	TIM break and dead-time register
[31]	rw	1'h0	OSSR	Off-state selection for Run mode This bit is used when MOE=1 on channels having a complementary output which are configured as outputs. OSSR is not implemented if no complementary output is implemented in the timer. 0: When inactive, OC/OCN outputs are disabled (the timer releases the output control, forces a Hi-Z state). 1: When inactive, OC/OCN outputs are enabled with their inactive level as soon as CCxE=1 or CCxNE=1 (the output is still controlled by the timer). This bit can not be modified as soon as the LOCK level 2 has been programmed.
[30]	rw	1'h0	OSSI	Off-state selection for Idle mode This bit is used when MOE=0 due to a break event or by a software write, on channels configured as outputs. 0: When inactive, OC/OCN outputs are disabled (the timer releases the output control, imposes a Hi-Z state). 1: When inactive, OC/OCN outputs are first forced with their inactive level then forced to their idle level after the deadtime. The timer maintains its control over the output. This bit can not be modified as soon as the LOCK level 2 has been programmed.
[29]	rw	1'h0	BK2BID	Break2 bidirectional
[28]	rw	1'h0	BKBID	Break Bidirectional 0: Break input BRK in input mode 1: Break input BRK in bidirectional mode In the bidirectional mode (BKBID bit set to 1), the break input is configured both in input mode and in open drain output mode. Any active break event asserts a low logic level on the Break input to indicate an internal break event to external devices. This bit cannot be modified as long as LOCK level 1 has been programmed (LOCK bits in BDTR register).
[27]	rw	1'h0	BK2DSRM	Break2 Disarm
[26]	rw	1'h0	BKDSRM	Break Disarm 0: Break input BRK is armed 1: Break input BRK is disarmed This bit is cleared by hardware when no break source is active. The BKDSRM bit must be set by software to release the bidirectional output control (open-drain output in Hi-Z state) and then be polled it until it is reset by hardware, indicating that the fault condition has disappeared.

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表 9-1: ATIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[25]	rw	1'h0	BK2P	BK2P: Break 2 polarity 0: Break input BRK2 is active low 1: Break input BRK2 is active high This bit cannot be modified as long as LOCK level 1 has been programmed.
[24]	rw	1'h0	BK2E	Break 2 enable This bit enables the complete break 2 protection. 0: Break2 function disabled 1: Break2 function enabled This bit cannot be modified as long as LOCK level 1 has been programmed.
[23:20]	rw	4'h0	BK2F	Break 2 filter This bit-field defines the frequency used to sample BRK2 input and the length of the digital filter applied to BRK2. The digital filter is made of an event counter in which N consecutive events are needed to validate a transition on the output: 0000: No filter, BRK2 acts asynchronously 0001: fSAMPLING=fCLK, N=2 0010: fSAMPLING=fCLK, N=4 0011: fSAMPLING=fCLK, N=8 0100: fSAMPLING=fCLK/2, N=6 0101: fSAMPLING=fCLK/2, N=8 0110: fSAMPLING=fCLK/4, N=6 0111: fSAMPLING=fCLK/4, N=8 1000: fSAMPLING=fCLK/8, N=6 1001: fSAMPLING=fCLK/8, N=8 1010: fSAMPLING=fCLK/16, N=5 1011: fSAMPLING=fCLK/16, N=6 1100: fSAMPLING=fCLK/16, N=8 1101: fSAMPLING=fCLK/32, N=5 1110: fSAMPLING=fCLK/32, N=6 1111: fSAMPLING=fCLK/32, N=8 This bit cannot be modified as long as LOCK level 1 has been programmed.

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表 9-1: ATIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[19:16]	rw	4'h0	BKF	Break filter This bit-field defines the frequency used to sample BRK input and the length of the digital filter applied to BRK. The digital filter is made of an event counter in which N consecutive events are needed to validate a transition on the output: 0000: No filter, BRK acts asynchronously 0001: fSAMPLING=fCLK, N=2 0010: fSAMPLING=fCLK, N=4 0011: fSAMPLING=fCLK, N=8 0100: fSAMPLING=fCLK/2, N=6 0101: fSAMPLING=fCLK/2, N=8 0110: fSAMPLING=fCLK/4, N=6 0111: fSAMPLING=fCLK/4, N=8 1000: fSAMPLING=fCLK/8, N=6 1001: fSAMPLING=fCLK/8, N=8 1010: fSAMPLING=fCLK/16, N=5 1011: fSAMPLING=fCLK/16, N=6 1100: fSAMPLING=fCLK/16, N=8 1101: fSAMPLING=fCLK/32, N=5 1110: fSAMPLING=fCLK/32, N=6 1111: fSAMPLING=fCLK/32, N=8 This bit cannot be modified as long as LOCK level 1 has been programmed.
[15]	rw	1'h0	MOE	Main output enable This bit is cleared asynchronously by hardware as soon as one of the break inputs is active (BRK or BRK2). It is set by software or automatically depending on the AOE bit. It is acting only on the channels which are configured in output. 0: In response to a break 2 event. OC and OCN outputs are disabled In response to a break event or if MOE is written to 0: OC and OCN outputs are disabled or forced to idle state depending on the OSSI bit. 1: OC and OCN outputs are enabled if their respective enable bits are set (CCxE, CCxNE in CCER register).
[14]	rw	1'h0	AOE	Automatic output enable 0: MOE can be set only by software 1: MOE can be set by software or automatically at the next update event (if none of the break inputs BRK and BRK2 is active) This bit cannot be modified as long as LOCK level 1 has been programmed.
[13]	rw	1'h0	BKP	Break polarity 0: Break input BRK is active low 1: Break input BRK is active high This bit cannot be modified as long as LOCK level 1 has been programmed.
[12]	rw	1'h0	BKE	Break enable This bit enables the complete break protection. 0: Break function disabled 1: Break function enabled This bit cannot be modified as long as LOCK level 1 has been programmed.
[11]	rw	1'h0	DTPSC	Dead-time prescaler This bit-field enables dead-time prescaler. 0: dead-time is tCLK*(DTG+1) if DTG is not zero 1: dead-time is tCLK*(DTG+1)*16 if DTG is not zero This bit cannot be modified as long as LOCK level 1 has been programmed.

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表 9-1: ATIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[10]			RSVD	
[9:0]	rw	10'h0	DTG	Dead-time generator setup This bit-field, together with DTPSC, defines the duration of the dead-time inserted between the complementary outputs. If DTG=0, dead-time is disabled. Example if tCLK=8.33ns (120MHz), dead-time possible values are: 16.67ns to 8533.33 ns by 8.33 ns steps if DTPSC=0, 266.67ns to 136.53 us by 133.33 ns steps if DTPSC=1 This bit cannot be modified as long as LOCK level 1 has been programmed.
0x54			**CCMR3**	TIM capture/compare mode register 3
[31:28]	rw	4'h0	OC6M	Output compare 6 mode
[27]	rw	1'h0	OC6PE	Output compare 6 preload enable
[26:25]			RSVD	
[24]	rw	1'h0	OC6CE	Output compare 6 clear enable
[23:20]	rw	4'h0	OC5M	Output compare 5 mode
[19]	rw	1'h0	OC5PE	Output compare 5 preload enable
[18:17]			RSVD	
[16]	rw	1'h0	OC5CE	Output compare 5 clear enable
[15]	rw	1'h0	GC5C3	Group Channel 5 and Channel 3 Distortion on Channel 3 output: 0: No effect of OC5REF on OC3REFC 1: OC3REFC is the logical AND of OC3REFC and OC5REF This bit can either have immediate effect or be preloaded and taken into account after an update event (if preload feature is selected in TIMxCCMR2).
[14]	rw	1'h0	GC5C2	Group Channel 5 and Channel 2 Distortion on Channel 2 output: 0: No effect of OC5REF on OC2REFC 1: OC2REFC is the logical AND of OC2REFC and OC5REF This bit can either have immediate effect or be preloaded and taken into account after an update event (if preload feature is selected in TIMxCCMR1).
[13]	rw	1'h0	GC5C1	Group Channel 5 and Channel 1 Distortion on Channel 1 output: 0: No effect of OC5REF on OC1REFC5 1: OC1REFC is the logical AND of OC1REFC and OC5REF This bit can either have immediate effect or be preloaded and taken into account after an update event (if preload feature is selected in TIMxCCMR1).
[12:0]			RSVD	
0x58			**CCR5**	Capture/Compare register 5
[31:0]	rw	32'h0	CCR5	Capture/Compare 5 value CCR5 is the value to be loaded in the actual capture/compare 5 register (preload value). It is loaded permanently if the preload feature is not selected in the CCMR3 register (bit OC5PE). Else the preload value is copied in the active capture/compare 5 register when an update event occurs. The active capture/compare register contains the value to be compared to the counter CNT and signaled on OC5 output.
0x5C			**CCR6**	Capture/Compare register 6

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表 9-1: ATIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:0]	rw	32'h0	CCR6	Capture/Compare 6 value CCR6 is the value to be loaded in the actual capture/compare 6 register (preload value). It is loaded permanently if the preload feature is not selected in the CCMR3 register (bit OC6PE). Else the preload value is copied in the active capture/compare 6 register when an update event occurs. The active capture/compare register contains the value to be compared to the counter CNT and signaled on OC6 output.
0x60			**AF1**	Alternate function option register
[31:30]	rw	2'h0	LOCK	Lock configuration These bits offer a write protection against software errors. 00: LOCK OFF - No bit is write protected. 01: LOCK Level 1 = OISx and OISxN bits in CR2 register, BK2BID, BKBID, BK2DSRM, BKDSRM, BK2P, BK2E, BK2F[3:0], BKF[3:0], AOE, BKP, BKE, OSSI, OSSR, DTPSC and DTG bits in BDTR register, AF1 register and AF2 register can no longer be written. 10: LOCK Level 2 = LOCK Level 1 + CC Polarity bits (CCxP/CCxNP bits in CCER register, as long as the related channel is configured in output through the CCxS bits) as well as OSSR and OSSI bits can no longer be written. 11: LOCK Level 3 = LOCK Level 2 + CC Control bits (OCxM and OCxPE bits in CCMRx registers, as long as the related channel is configured in output through the CCxS bits) can no longer be written. The LOCK bits can be written to non-zero only once after reset.
[29:16]			RSVD	
[15:14]	rw	2'h0	ETRSEL	ETR source selection 00: ETR input is connected to I/O 01: LPCOMP output1 (if LPCOMP integrated) 10: LPCOMP output2 (if LPCOMP integrated) 11: ETR input is connected to I/O This bit cannot be modified as long as LOCK level 1 has been programmed.
[13:12]			RSVD	
[11]	rw	1'h0	BKCMP2P	BRK LPCOMP output2 polarity This bit selects the LPCOMP output2 sensitivity (if LPCOMP integrated). It must be programmed together with the BKP polarity bit. 0: LPCOMP output2 is active high 1: LPCOMP output2 is active low This bit cannot be modified as long as LOCK level 1 has been programmed.
[10]	rw	1'h0	BKCMP1P	BRK LPCOMP output1 polarity This bit selects the LPCOMP output1 sensitivity (if LPCOMP integrated). It must be programmed together with the BKP polarity bit. 0: LPCOMP output1 is active high 1: LPCOMP output1 is active low This bit cannot be modified as long as LOCK level 1 has been programmed.
[9]	rw	1'h0	BKINP	BRK BKIN input polarity This bit selects the BKIN input sensitivity. It must be programmed together with the BKP polarity bit. 0: BKIN input is active high 1: BKIN input is active low This bit cannot be modified as long as LOCK level 1 has been programmed.
[8:3]			RSVD	

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表 9-1: ATIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[2]	rw	1'h0	BKCMP2E	BRK LPCOMP output2 enable This bit enables the LPCOMP output2 (if LPCOMP integrated) for the timer's BRK input. LPCOMP output2 is 'ORed' with the other BRK sources. 0: LPCOMP output2 disabled 1: LPCOMP output2 enabled This bit cannot be modified as long as LOCK level 1 has been programmed.
[1]	rw	1'h0	BKCMP1E	BRK LPCOMP output1 enable This bit enables the LPCOMP output1 (if LPCOMP integrated) for the timer's BRK input. LPCOMP output1 is 'ORed' with the other BRK sources. 0: LPCOMP output1 disabled 1: LPCOMP output1 enabled This bit cannot be modified as long as LOCK level 1 has been programmed.
[0]	rw	1'h0	BKINE	BRK BKIN input enable This bit enables the BKIN input. BKIN input is 'Ored' with the other BRK sources. 0: BKIN input disabled 1: BKIN input enabled This bit cannot be modified as long as LOCK level 1 has been programmed.
0x64			**AF2**	Alternate function option register 2
[31:12]			RSVD	
[11]	rw	1'h0	BK2CMP2P	BRK2 LPCOMP output2 polarity This bit selects the LPCOMP output2 sensitivity (if LPCOMP integrated). It must be programmed together with the BK2P polarity bit. 0: LPCOMP output2 is active high 1: LPCOMP output2 is active low This bit cannot be modified as long as LOCK level 1 has been programmed.
[10]	rw	1'h0	BK2CMP1P	BRK2 LPCOMP output1 polarity This bit selects the LPCOMP output1 sensitivity (if LPCOMP integrated). It must be programmed together with the BK2P polarity bit. 0: LPCOMP output1 is active high 1: LPCOMP output1 is active low This bit cannot be modified as long as LOCK level 1 has been programmed.
[9]	rw	1'h0	BK2INP	BRK2 BKIN2 input polarity This bit selects the BKIN2 input sensitivity. It must be programmed together with the BK2P polarity bit. 0: BKIN2 input is active low 1: BKIN2 input is active high This bit cannot be modified as long as LOCK level 1 has been programmed.
[8:3]			RSVD	
[2]	rw	1'h0	BK2CMP2E	BRK2 LPCOMP output2 enable This bit enables the LPCOMP output2 (if LPCOMP integrated) for the timer's BRK2 input. LPCOMP output2 is 'ORed' with the other BRK2 sources. 0: LPCOMP output2 disabled 1: LPCOMP output2 enabled This bit cannot be modified as long as LOCK level 1 has been programmed.

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表 9-1: ATIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[1]	rw	1'h0	BK2CMP1E	BRK2 LPCOMP output1 enable This bit enables the LPCOMP output1 (if LPCOMP integrated) for the timer's BRK2 input. LPCOMP output1 is 'ORed' with the other BRK2 sources. 0: LPCOMP output1 disabled 1: LPCOMP output1 enabled This bit cannot be modified as long as LOCK level 1 has been programmed.
[0]	rw	1'h0	BK2INE	BRK2 BKIN input enable This bit enables the BKIN2 input. BKIN2 input is 'Ored' with the other BRK2 sources. 0: BKIN2 input disabled 1: BKIN2 input enabled This bit cannot be modified as long as LOCK level 1 has been programmed.

9.2 BTIM

芯片共有 4 个 BTIM，其中 BTIM1 和 BTIM2 位于 HPSYS，可向 DMAC1 发送请求；BTIM3 和 BTIM4 位于 LPSYS，可向 DMAC2 发送请求。

9.2.1 简介

BTIM (Basic Timer) 基于一个 32 比特递增计数器，可实现计时功能。计数时钟为系统 PCLK 或级联输入信号，并可进行 1~65536 倍的预分频。计时结果可以产生中断、DMA 请求或 PTC 触发。BTIM 包含主从模式接口，可以进行多级级联，实现多级计数或同步触发等功能。

9.2.2 主要特性

- 32 位递增自动重装载计数器
- 16 位可编程预分频器，计数器时钟频率的分频系数为 1~65536 之间的任意数值
- 支持单笔计数模式 (OPM)，计数完成后自动停止计数器
- 主从模式
  - 支持与其它定时器互连，可在作为主设备产生控制信号的同时，作为从设备被外部输入或其它主设备控制
  - 控制模式包括复位、触发、门控等
  - 支持多定时器同步启动、复位等
- 计数器溢出或初始化时产生中断/DMA

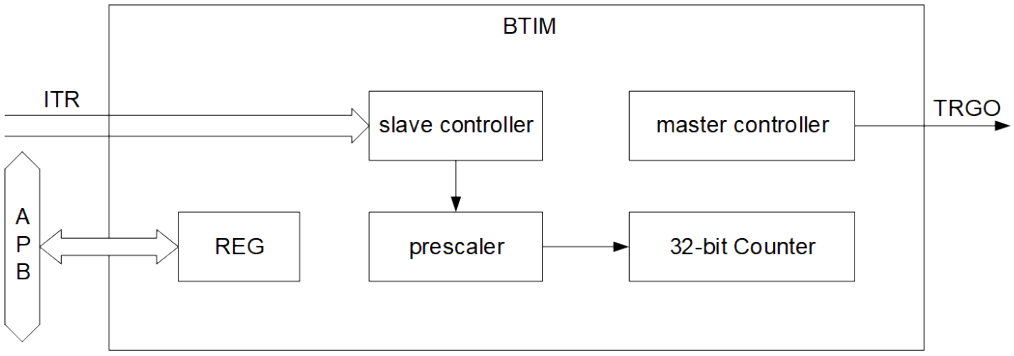

图 9-7: BTIM 结构图

9.2.3 BTIM 功能描述

9.2.3.1 计数器

BTIM 的各项功能均基于一个 32 比特的计数器。计数器基于事件计数，最基本的事件是一个 PCLK 时钟的翻转。根据不同配置，其它计数事件包括外部输入的翻转、其它定时器的输出翻转等。

计数事件经过预分频处理才会真正进入计数器。预分频的次数介于 1 到 65536 之间 (PSC+1)，即仅当发生了 (PSC+1) 次计数事件，计数器的值才真正改变一次。

计数器固定为递增计数模式，计数器从 0 计数到自动重载值 ARR，然后重新从 0 开始计数并产生计数器上溢事件。计数值可以通过 CNT 读出。

9.2.3.2 更新事件 (UEV)

更新事件用于标志一个计数单元的结束。最基本的更新事件产生于每次计数器上溢时。软件将 EGR_UG 置 1 时，也将产生更新事件。更新事件可以产生中断、DMA 请求以及 PTC 触发，是定时器最基本的一项通知功能。

通过软件将 CR1_UDIS 置 1 可禁止产生更新事件。这可避免向预装载寄存器写入新值时更新影子寄存器。在 UDIS 位写入 0 之前不会产生任何更新事件。

如果 CR1_URS（更新请求选择）已置 1，则将 EGR_UG 置 1 会生成更新事件，但不会将 UIF 标志置 1（因此，不会发送任何中断或 DMA 请求）。这样一来，如果在发生捕获事件时将计数器清零，将不会同时产生更新中断和捕获中断。

发生更新事件时，将重新装载 ARR 以及 PSC 寄存器，且将更新标志 SR_UIF 置 1（CR1_URS=0 时）。该功能可以保证修改这些计数器的基本参数不影响当前计数单元，在下一个计数周期才生效。

9.2.3.3 影子寄存器

对 ARR 以及 PSC 寄存器的修改不会直接体现在当前计数单元中，而是等到更新事件发生时才真正更新进去。在更新事件发生前，计数器真正使用的是影子寄存器中的值。这样即使在计数中动态改变这些寄存器的值，也不会影响到当前计数单元的完整性。

如果 CR1_APRE 为 0，ARR 寄存器将在配置后实时生效，不用等到更新事件发生。

9.2.3.4 主从模式

定时器可同时处于主模式与从模式。主模式是指该定时器可以输出 TRGO 信号至芯片上其它定时器的 ITR 输入，用于控制其它定时器的计数行为。从模式是指该定时器的计数行为受其它定时器输出至该定时器的 ITR 信号控制。

多个定时器可通过主从模式实现定时器同步，以实现多级分频、同时启动、门控计数等功能。

主模式可在不同事件发生时输出 TRGO 信号，如更新、使能等，由 CR2_MMS 选择。

从模式可以通过 SMCR_SMS 选择计数器复位、触发启动、计数事件等行为，同时可以选择门控模式。从模式依赖的触发信号 TRGI 和门控信号可在 ITR 中独立选择，并可选择门控信号极性。

定时器处于复位从模式 (SMCR_SMS=001) 时，当 TRGI 发生变化时，计数器及其预分频器重新初始化。如果 CR1_URS 为 0，则会生成更新事件 UEV，ARR 被更新。

定时器处于触发从模式 (SMCR_SMS=010) 时，软件不需配置 CR1_CEN 开启计数，而是在 TRGI 上升沿自动启动计数器。定时器处于复位触发从模式 (SMCR_SMS=011) 时，在 TRGI 的上升沿复位计数器并自动重新开启。

定时器处于外部时钟从模式 (SMCR_SMS=100) 时，计数事件修改为 TRGI 的上升沿，仅当 TRGI 发生翻转时才进行计数。

定时器开启门控从模式 (SMCR_GM=1) 时，当 TRGI 满足高电平或低电平要求 (SMCR_GTP) 时才进行计数，否则计数器不变。

9.2.3.5 单脉冲模式

将 CR1_OPM 写 1 可以使能单脉冲模式。该模式下计数器启动以后一旦发生更新事件，就会自动停止计数。该模式可以用于单次计数。

9.2.3.6 定时器同步

多个定时器可通过主从模式连接在一起，实现定时器同步，以完成多级分频、同时启动、门控计数等功能。

将主模式定时器的 TRGO 设置为更新事件，连接至另一个设置为外部时钟从模式的定时器，可以实现定时器级联计数。此时主模式定时器相当于从模式定时器的预分频，计数总位宽等于两个定时器各自的位宽相加。

将主模式定时器的 TRGO 设置为计数使能，并设置从模式为触发从模式，同时连接至另一个设置为触发从模式的定时器，可以实现多个定时器同步触发启动，从而对齐多个定时器的开启时机。该场景下主模式定时器还需将 SMCR_MSM 设为 1。

9.2.3.7 通知机制

BTIM 能够产生中断、DMA 请求、PTC 触发等多种通知机制。能够触发通知的事件为更新事件。DIER 寄存器可以控制各种事件是否产生中断和 DMA 请求。各事件状态可在 SR 寄存器中查询。

9.2.4 BTIM 寄存器

表 9-2: BTIM 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00			**CR1**	TIM control register 1
[31:8]			RSVD	
[7]	rw	1'h0	ARPE	Auto-reload preload enable 0: ARR register is not buffered 1: ARR register is buffered
[6:4]			RSVD	
[3]	rw	1'h0	OPM	One-pulse mode 0: Counter is not stopped at update event 1: Counter stops counting at the next update event (clearing the bit CEN)
[2]	rw	1'h0	URS	Update request source This bit is set and cleared by software to select the UEV event sources. 0: Any of the following events generate an update interrupt or DMA request if enabled. These events can be: Counter overflow Setting the UG bit Update generation through the slave mode controller 1: Only counter overflow generates an update interrupt or DMA request if enabled.
[1]	rw	1'h0	UDIS	Update disable This bit is set and cleared by software to enable/disable UEV event generation. 0: UEV enabled. The Update (UEV) event is generated by one of the following events: Counter overflow Setting the UG bit Update generation through the slave mode controller Buffered registers are then loaded with their preload values. 1: UEV disabled. The Update event is not generated, shadow registers keep their value (ARR, PSC). However the counter and the prescaler are reinitialized if the UG bit is set or if a hardware reset is received from the slave mode controller.
[0]	rw	1'h0	CEN	Counter enable 0: Counter disabled 1: Counter enabled Note: Gated mode can work only if the CEN bit has been previously set by software. However trigger mode can set the CEN bit automatically by hardware. CEN is cleared automatically in one-pulse mode, when an update event occurs.
0x04			**CR2**	TIM control register 2
[31:6]			RSVD	

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表 9-2: BTIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[5:4]	rw	2'h0	MMS	Master mode selection These bits allow to select the information to be sent in master mode to slave timers for synchronization (TRGO). The combination is as follows: 00: Reset:the UG bit from the EGR register is used as trigger output (TRGO). If the reset is generated by the trigger input (slave mode controller configured in reset mode) then the signal on TRGO is delayed compared to the actual reset. 01: Enable :the Counter enable signal, CNT_EN, is used as trigger output (TRGO). It is useful to start several timers at the same time or to control a window in which a slave timer is enabled. The Counter Enable signal is generated by a logic OR between CEN control bit and the trigger input when configured in gated mode. When the Counter Enable signal is controlled by the trigger input, there is a delay on TRGO, except if the master/slave mode is selected (see the MSM bit description in SMCR register). 10: Update:The update event is selected as trigger output (TRGO). For instance a master timer can then be used as a prescaler for a slave timer. 11: Gating:The delayed gating trigger is selected as trigger output (TRGO).
[3:0]			RSVD	
0x08			**SMCR**	TIM slave mode control register
[31:24]			RSVD	
[23]	rw	1'h0	GM	Gated Mode. The counter clock is enabled when the selected trigger input (TRGI) is active (according to gating trigger polarity). The counter stops (but is not reset) as soon as the trigger becomes inactive. Both start and stop of the counter are controlled. Gated mode and slave mode can be enabled simutanuously with different trigger selection.
[22]	rw	1'h0	GTP	Gating trigger polarity invert 0: active at high level 1: active at low level
[21:20]	rw	2'h0	GTS	Gating trigger selection in gated mode This bit-field selects the trigger input to be used to enable the counter gating. 00: Internal Trigger 0 (ITR0) 01: Internal Trigger 1 (ITR1) 10: Internal Trigger 2 (ITR2) 11: Internal Trigger 3 (ITR3)
[19]			RSVD	
[18:16]	rw	3'h0	SMS	Slave mode selection When external signals are selected the active edge of the trigger signal (TRGI) is linked to the polarity selected on the external input. 000: Slave mode disabled. 001: Reset Mode - Rising edge of the selected trigger input (TRGI) reinitializes the counter and generates an update of the registers. 010: Trigger Mode - The counter starts at a rising edge of the trigger TRGI (but it is not reset). Only the start of the counter is controlled. 011: Combined reset + trigger mode - Rising edge of the selected trigger input (TRGI) reinitializes the counter, generates an update of the registers and starts the counter. 100: External Clock Mode - Rising edges of the selected trigger (TRGI) clock the counter.
[15:8]			RSVD	

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表 9-2: BTIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[7]	rw	1'h0	MSM	Master/Slave mode. This bit should be asserted on master timer if synchronization if needed. 0: No action 1: The effect of an event on the trigger input (TRGI) is delayed to allow a perfect synchronization between the current timer and its slaves (through TRGO). It is useful if we want to synchronize several timers on a single external event.
[6]			RSVD	
[5:4]	rw	2'h0	TS	Trigger selection This bit-field selects the trigger input to be used to synchronize the counter. 00: Internal Trigger 0 (ITR0) 01: Internal Trigger 1 (ITR1) 10: Internal Trigger 2 (ITR2) 11: Internal Trigger 3 (ITR3)
[3:0]			RSVD	
0x0C			**DIER**	TIM DMA/Interrupt enable register
[31:9]			RSVD	
[8]	rw	1'h0	UDE	Update DMA request enable 0: Update DMA request disabled. 1: Update DMA request enabled
[7:1]			RSVD	
[0]	rw	1'h0	UIE	Update interrupt enable 0: Update interrupt disabled. 1: Update interrupt enabled
0x10			**SR**	TIM status register
[31:1]			RSVD	
[0]	rw0c	1'h0	UIF	Update interrupt flag This bit is set by hardware on an update event. It is cleared by software. 0: No update occurred 1: Update interrupt pending. This bit is set by hardware when the registers are updated: At overflow and if UDIS=0 in the CR1 register. When CNT is reinitialized by software using the UG bit in EGR register, if URS=0 and UDIS=0 in the CR1 register. When CNT is reinitialized by a trigger event (refer to the synchro control register description), if URS=0 and UDIS=0 in the CR1 register.
0x14			**EGR**	Event generation register
[31:1]			RSVD	
[0]	w1s	1'h0	UG	Update generation This bit can be set by software, it is automatically cleared by hardware. 0: No action 1: Re-initialize the counter and generates an update of the registers. Note that the prescaler counter is cleared too (anyway the prescaler ratio is not affected). The counter is cleared if the center-aligned mode is selected or if DIR=0 (upcounting), else it takes the auto-reload value (ARR) if DIR=1 (downcounting).
0x24			**CNT**	Counter
[31:0]	rw	32'h0	CNT	counter value
0x28			**PSC**	Prescaler
[31:16]			RSVD	

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表 9-2: BTIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[15:0]	rw	16'h0	PSC	Prescaler value The counter clock frequency is equal to fCLK / (PSC[15:0] + 1). PSC contains the value to be loaded in the active prescaler register at each update event (including when the counter is cleared through UG bit of EGR register or through trigger controller when configured in "reset mode").
0x2C			**ARR**	Auto-reload register
[31:0]	rw	32'h0	ARR	Auto-reload value ARR is the value to be loaded in the actual auto-reload register. The counter is blocked while the auto-reload value is null.

9.3 GPTIM

芯片共有 5 个 GPTIM，其中 GPTIM 1 和 GPTIM 2 位于 HPSYS，输入输出连接至 IO(PA)，可向 DMAC1 发送请求；GPTIM 3，GPTIM4 和 GPTIM5 位于 LPSYS，输入输出连接至 IO(PB)，可向 DMAC2 发送请求。

9.3.1 简介

GPTIM (General Purpose Timer) 基于一个 16 比特计数器，可实现计时、测量输入信号的脉冲长度 (输入捕获) 或者产生输出波形 (输出比较和 PWM) 等功能。计数器本身可以进行递增、递减或者递增/递减计数，计数时钟可选系统 PCLK，IO 输入信号或级联输入信号，并可进行 1~65536 倍的预分频。GPTIM 共有 4 个通道，可以分别独立配置为输入捕获或输出模式。计数、输入捕获和输出比较的结果可以产生中断、DMA 请求或 PTC 触发。GPTIM 包含主从模式接口，可以进行多级级联，实现多级计数或同步触发等功能。

9.3.2 主要特性

- 16 位递增、递减、递增/递减自动重装载计数器，最大计数 65535
- 16 位可编程 (可以实时修改) 预分频器，计数器时钟频率的分频系数为 1~65536 之间的任意数值
- 8 位可配置重复计数
- 支持单笔计数模式 (OPM)，当重复计数完成后自动停止计数器
- 4 个独立通道，可分别配置为输入或输出模式
- 输入模式
  - 上升沿/下降沿捕获
  - PWM 脉宽和周期捕获 (需占用两个通道)
  - 可选 4 个输入端口之一或 1 个外部触发端口，支持防抖动滤波和预降频
- 输出模式
  - 强制输出高/低电平
  - 计数到比较值时输出高/低/翻转电平
  - PWM 输出，可配脉宽和周期
  - 多通道 PWM 组合输出，可产生有相互关系的多路 PWM
  - 单脉冲/重触发单脉冲模式输出
- 主从模式
  - 支持多定时器互连，可在作为主设备产生控制信号的同时，作为从设备被外部输入或其它主设备控制

  - 控制模式包括复位、触发、门控等
  - 支持多定时器同步启动、复位等
- 编码模式输入，控制计数器递增/递减计数
- 如下事件发生时产生中断/DMA 请求/PTC 触发：
  - 更新：计数器递增溢出/递减溢出，计数器初始化 (通过软件或者内部/外部触发)
  - 触发事件 (计数器启动、停止、初始化或者由内部/外部触发计数)
  - 输入捕获
  - 输出比较

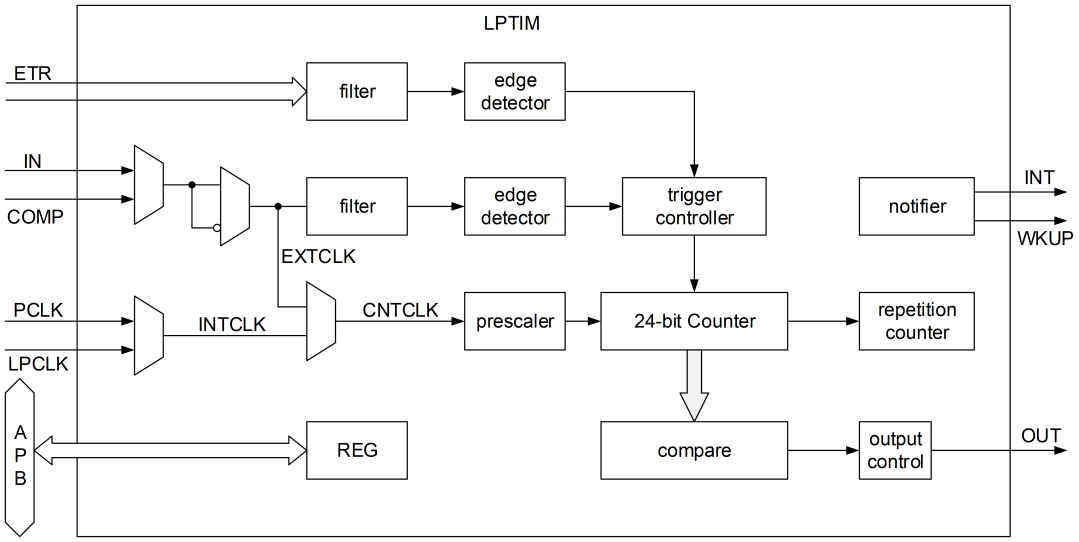


图 9-8: GPTIM 结构图

9.3.3 GPTIM 功能描述

9.3.3.1 计数器

GPTIM 的各项功能均基于一个 16 比特的计数器。计数器基于事件计数，最基本的事件是一个 PCLK 时钟的翻转。根据不同配置，其它计数事件包括外部输入的翻转、其它定时器的输出翻转、正交编码器接口解码输出等。

计数事件经过预分频处理才会真正进入计数器。预分频的次数介于 1 到 65536 之间 (PSC+1)，即仅当发生了 (PSC+1) 次计数事件，计数器的值才真正改变一次。

计数器共有三种计数模式：递增，递减以及中心对齐。在递增计数模式下 (CR1_CMS=0 且 CR1_DIR=0)，计数器从 0 计数到自动重载值 ARR，然后重新从 0 开始计数并产生计数器上溢事件。在递减计数模式下 (CR1_CMS=0 且 CR1_DIR=1)，计数器从 ARR 开始递减计数到 0，然后重新从 ARR 开始计数并产生计数器下溢事件。在中心对齐模式下 (CR1_CMS 不为 0)，计数器从 0 开始计数到 ARR-1，产生计数器上溢事件，然后从 ARR 开始向下计数到 1 并产生计数器下溢事件，之后从 0 开始重新计数。

计数值可以通过 CNT 读出。计数的方向可以从 CR1_DIR 读出。

9.3.3.2 更新事件 (UEV)

更新事件用于标志一个计数单元的结束。最基本的更新事件产生于每次计数器上溢或下溢时 (未开启重复计数时)。软件将 EGR_UG 置 1 时，也将产生更新事件。更新事件可以产生中断、DMA 请求以及 PTC 触发，是定时

器最基本的一项通知功能。

通过软件将 CR1_UDIS 置 1 可禁止产生更新事件。这可避免向预装载寄存器写入新值时更新影子寄存器。在 UDIS 位写入 0 之前不会产生任何更新事件。

如果 CR1_URS（更新请求选择）已置 1，则将 EGR_UG 置 1 会生成更新事件，但不会将 UIF 标志置 1（因此，不会发送任何中断或 DMA 请求）。这样一来，如果在发生捕获事件时将计数器清零，将不会同时产生更新中断和捕获中断。

发生更新事件时，将重新装载 RCR，ARR 以及 PSC 寄存器，且将更新标志 SR_UIF 置 1（CR1_URS=0 时）。该功能可以保证修改这些计数器的基本参数不影响当前计数单元，在下一个计数周期才生效。

9.3.3.3 重复计数

如果配置了重复计数器 (RCR>0)，每次计数器上溢或下溢时重复计数器会递减，并仅当重复计数器为 0 时才产生更新事件。更新事件发生时，重复计数器会重新装载 RCR 的值。

重复计数器的当前值不能读出。

9.3.3.4 影子寄存器

对 RCR，ARR 以及 PSC 寄存器的修改不会直接体现在当前计数单元中，而是等到更新事件发生时才真正更新进去。在更新事件发生前，计数器真正使用的是影子寄存器中的值。这样即使在计数中动态改变这些寄存器的值，也不会影响到当前计数单元的完整性，对于 PWM 输出等应用场景很有意义。

如果 CR1_APRE 为 0，ARR 寄存器将在配置后实时生效，不用等到更新事件发生。

输出比较寄存器 CCRx 也有影子寄存器。当 CCMRx_OCxPE 为 0 时，配置的 CCRx 会立即生效，否则要等到更新事件发生时才生效。

9.3.3.5 主从模式

定时器可同时处于主模式与从模式。主模式是指该定时器可以输出 TRGO 信号至芯片上其它定时器的 ITR 输入，用于控制其它定时器的计数行为。从模式是指该定时器的计数行为受外部输入 ETR，其它定时器输出至该定时器的 ITR 信号，或定时器的通道输入 CHx 的控制。

多个定时器可通过主从模式实现定时器同步，以实现多级分频、同时启动、门控计数等功能。

主模式可在不同事件发生时输出 TRGO 信号，如更新、使能、输入捕获、输出比较等，由 CR2_MMS 选择。

从模式可以选择计数器复位、触发启动、计数使能、计数事件等行为，由 SMCR_SMS 选择。从模式依赖的触发信号 TRGI 可灵活配置，可以在 ETR，ITR 以及通道输入中选择，并可选择信号极性，进行预分频、滤波等操作。

- 定时器处于复位从模式 (SMCR_SMS=0100) 时，当 TRGI 发生变化时，计数器及其预分频器重新初始化。如果 CR1_URS 为 0，则会生成更新事件 UEV，然后所有预装载寄存器 ARR 和 CCRx 都将更新。
- 定时器处于门控从模式 (SMCR_SMS=0101) 时，当 TRGI 满足高电平或低电平要求时才进行计数，否则计数器不变。
- 定时器处于触发从模式 (SMCR_SMS=0110) 时，软件不需配置 CR1_CEN 开启计数，而是当 TRGI 满足特定触发要求时自动启动计数器。

- 定时器处于外部时钟从模式 (SMCR_SMS=0111) 时，计数事件修改为 TRGI 的上升沿，仅当 TRGI 发生翻转时才进行计数。
- 定时器处于复位触发从模式 (SMCR_SMS=1000) 时，TRGI 满足特定触发要求时复位计数器并自动重新开启。

9.3.3.6 通道输入输出

定时器的部分通道可以独立配置为输入捕获模式 (CCMRx_CCxS!=0) 或输出模式 (CCMRx_CCxS=0)。

在输入捕获模式下，通道在对应的触发信号有效时，将计数器的值记录进 CCRx，并产生中断等通知信号。该触发信号可在 ETR，ITR 以及通道输入 CHx 中选择，并可选择信号极性，进行预分频、滤波等操作。通道产生的通知信号包括中断、DMA 请求、PTC 触发等。输入捕获模式可实现记录外部信号改变的时刻、测量 PWM 周期和占空比等功能。

在输出模式下，通道将比较计数器的值与 CCRx 的大小，在通道输出 CHx/CHxN 上产生固定电平，或产生基于本通道以及其它通道比较结果的 PWM 输出信号，并产生中断等通知信号。产生 PWM 信号的脉冲个数、频率、占空比、相位等参数均可调节。多个通道还可以联合产生特定关系的 PWM 组合。通道产生的通知信号包括中断、DMA 请求、PTC 触发等。

9.3.3.7 输入捕获模式

在输入捕获模式下，当通道相应的触发信号检测到跳变沿后，将使用 CCRx 来锁存计数器的值。发生捕获事件时，会将相应的 SR_CCxIF 标志置 1，并可发送中断、DMA 请求（如果已使能）或 PTC 触发信号。如果发生捕获事件时 SR_CCxIF 标志已处于高位，则会将重复捕获标志 SR_CCxOF 置 1。可通过软件将 SR_CCxIF 清零，方法是向 SR_CCxIF 写入 0，或读取存储在 CCRx 中的已捕获数据。向 SR_CCxOF 写入 0 后会将其清零。

以下示例说明了如何在 CH1 输入出现上升沿时将计数器的值捕获到 CCR1 中，具体操作步骤如下：

1. 选择有效输入：通道 1 要连接到 CH1 输入，因此向 CCMR1_CC1S 写入 01。
2. 根据连接到定时器的信号，对所需的输入滤波带宽进行配置。
   假设 CH1 信号边沿变化时，最多在 5 个 PCLK 周期内发生抖动，需将滤波带宽设置为大于 5 个 PCLK 周期。将 CCMR1_IC1F 设置为 0011(0x3)，则在检测到连续 8 个采样点（以 PCLK 频率采样）均为新电平后，可以确认 CH1 的跳变沿。
3. 将 CCER_CC1P 和 CCER_CC1NP 写 0，选择 CH1 上的有效转换边沿为上升沿。
4. 对输入预分频器进行编程。
   在本例中我们希望每次有效转换时都执行捕获操作，因此禁用预分频器（CCMR1_IC1PS 写 00）。
5. CCER_CC1E 置 1，使能通道 1，允许将计数器的值捕获到 CCR1 中。
6. 如果需要，可将 DIER_CC1IE 置 1 来使能相关中断请求，或将 DIER_CC1DE 置 1 来使能 DMA 请求。

配置完成后，通道将在 CH1 输入出现上升沿时执行下列操作：

1. CCR1 寄存器记录计数器的值。
2. SR_CCxIF 标志置 1（中断标志）。如果至少发生了两次连续捕获，但 SR_CCxIF 未被清零，这样 SR_CCxOF 捕获溢出标志会被置 1。
3. 根据 CCER_CC1IE 生成中断。
4. 根据 DIER_CC1DE 生成 DMA 请求。

要处理重复捕获，建议在读出 SR_CCxOF 之前读取数据。这样可避免丢失在读取 SR_CCxOF 之后与读取数据之前可能出现的重复捕获信息。

通过软件将 EGR_CCxG 置 1 可立即产生一次捕获，并生成通道捕获中断和 DMA 请求。

9.3.3.8 PWM 输入捕获

PWM 输入捕获是输入捕获的一种扩展应用，可用于测量 PWM 输入信号的周期和占空比。为实现该功能，需要将两个通道都配置为输入捕获模式，触发信号分别映射成输入 PWM 的正边沿和负边沿，并开启计数器复位的从模式。

以下示例说明了如何用通道 1 和通道 2 测量从 CH1 输入的 PWM 的周期和占空比，具体操作步骤如下：

1. 选择通道 1 的有效输入为 CH1 输入，因此向 CCMR1_CC1S 写入 01。
2. 选择通道 1 输入信号的有效极性（用于在 CCR1 中捕获和计数器清零），将 CCER_CC1P 和 CCER_CC1NP 写 0，选择 CH1 上的有效转换边沿为上升沿。
3. 选择通道 2 的有效输入也为 CH1 输入，向 CCMR1_CC2S 写入 10(0x2)。
4. 选择通道 2 输入信号的有效极性（用于 CCR2 捕获），将 CCER_CC2P 写 1，CCER_CC1NP 写 0，选择 CH1 上的有效转换边沿为下降沿。
5. 设置从模式控制信号为 CH1，向 SMCR_TS 写入 101(0x5)，选择 TI1FP1。
6. 将从模式控制器配置为复位模式，向 SMCR_SMS 写入 0100(0x4)。
7. 使能通道 1 和通道 2，将 CCER_CC1E 和 CCER_CC2E 置 1。

配置完成后，在每个 CH1 的上升沿，计数器的值被记录在 CCR1 中，同时计数器被复位并重新开始计数；在每个 CH1 的下降沿，计数器的值被记录在 CCR2 中。将 CCR1 的值乘以 PCLK 的周期，可以算出 PWM 的周期。将 CCR2 的值乘以 PCLK 的周期，可以算出 PWM 高电平持续的时间，从而得到 PWM 的占空比。

9.3.3.9 输出比较模式

在输出比较模式下，当计数值与 CCRx 满足一定关系时，可以在对应 CHx 及 CHxN 上产生特定输出，通常用于控制输出波形，或指示已经过某一时间段。

具体而言，通道将在 CCRx 与计数器之间相匹配时执行下列操作：

1. 将为相应的 CHx 和 CHxN 输出分配一个可编程值，该值由比较模式寄存器 CCMRx_OCxM 和输出极性寄存器 CCER_CCxP/CCxNP 定义。匹配时，输出引脚既可保持其电平（CCMRx_OCxM=0000），也可设置为有效电平 (CCMRx_OCxM=0001)、无效电平 (CCMRx_OCxM=0010) 或进行翻转 (CCMRx_OCxM=0011)。
2. 将中断状态寄存器标志 SR_CCxIF 置 1。
3. 根据 CCER_CC1IE 生成中断。
4. 根据 DIER_CC1DE 和 CR2_CCDS 生成 DMA 请求。

配置 CCMRx_OCxPE，可将 CCRx 寄存器配置为带或不带影子寄存器。当 CCMRx_OCxPE 为 0 时，软件修改 CCRx 实时生效，可通过在每次中断中修改下一次匹配的 CCRx 来实现自定义波形的输出。

9.3.3.10 基础 PWM 输出

利用输出比较模式，定时器可以产生周期、占空比、相位可控的多路 PWM 输出。PWM 输出的周期由 ARR 决定，占空比由 CCRx 决定。PWM 输出有多种模式，由每个通道的 CCMRx_OCxM 各自独立选择。最基本的单路

PWM 输出只需要占用一个通道，采用基础的 PWM 模式即可实现。复杂的 PWM 信号，或 PWM 组合则需要占用多个通道，并需仔细分配每个通道的 PWM 模式以及 CCRx。

在基础的 PWM 模式下，计数器值 CNT 与 CCRx 进行比较，并根据计数器的当前计数方向产生包含有效电平或无效电平的比较输出信号 OCxREF。有效电平的极性可通过 CCER_CCxP 配置，并根据 CCER_CCxE 和 BDTR_MOE 等寄存器使能 CHx 输出。

如在递增计数模式下，配置 CCMR1_OC1M 和 CCMR1_OC2M 为 0110(0x6)，则 PWM 输出如图9-9。其中计数值 CNT 小于 CCR1/2 时，输出高电平，否则输出低电平。

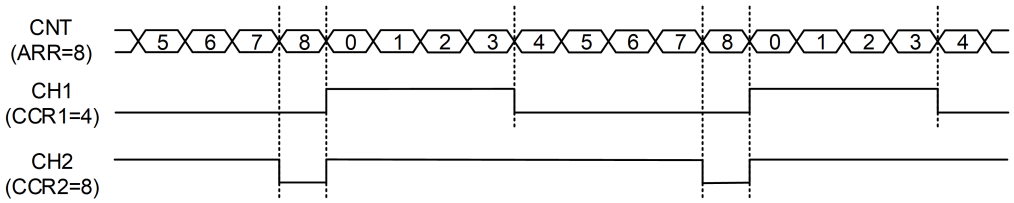


图 9-9: 递增计数模式下的 PWM 输出

如在中心对齐计数模式下，配置 CCMR1_OC1M 和 CCMR1_OC2M 为 0110(0x6)，则 PWM 输出如图9-10。其中递增阶段计数值 CNT 小于 CCR1/2 时，输出高电平，否则输出低电平；递减阶段计数值 CNT 大于 CCR1/2 时，输出低电平，否则输出高电平。

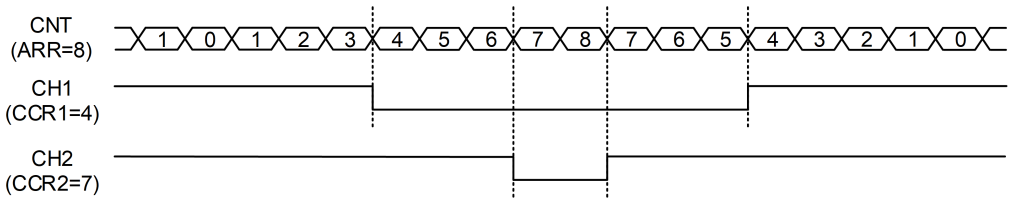


图 9-10: 中心对齐计数模式下的 PWM 输出

9.3.3.11 不对称 PWM 输出

在不对称 PWM 模式下，生成的两个 PWM 信号之间存在可编程相移。该模式仅限于计数器处于中心对齐模式时。生成的两个 PWM 信号频率相同，由 ARR 的值确定，而占空比和相移则各由一对 CCRx 寄存器确定。每一路输出 PWM 占用两个 CCRx 寄存器，分别控制递增计数和递减计数期间的行为，这样 PWM 的上升沿和下降沿时间点可以分别配置。CCR1 和 CCR2 共同控制 CH1/2 的输出，CCR3 和 CCR4 共同控制 CH3/4 的输出。

CH1/2 以及 CH3/4 可以独立选择不同的不对称 PWM 模式，配置 CCMRx_OCxM 为 1110(0xe) 或 1111(0xf)。

如配置 CCMR1_OC1M 和 CCMR2_OC3M 为 1110(0xe)，则 PWM 输出如图9-11。其中递增阶段 (0->ARR-1) 计数值 CNT 小于 CCR1/3 时，输出高电平，否则输出低电平；递减阶段 (ARR->1) 计数值 CNT 大于 CCR2/4 时，输出低电平，否则输出高电平。

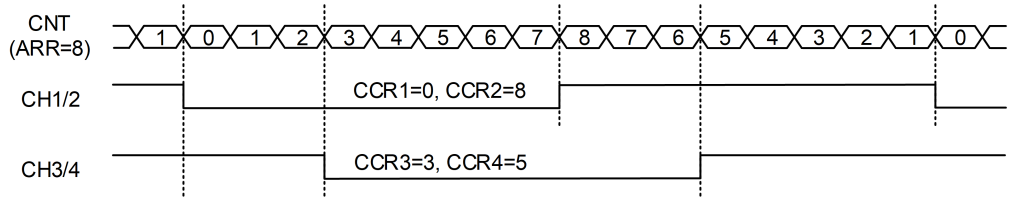


图 9-11: 不对称 PWM 输出

9.3.3.12 组合 PWM 输出

在组合 PWM 模式下，生成的两个 PWM 信号之间存在可编程延时和相移。计数器处于递增、递减或中心对齐模式均可，生成的两个 PWM 信号频率相同，由 ARR 的值确定，而占空比和相移则各由一对 CCRx 寄存器确定。每一路输出 PWM 占用两个 CCRx 寄存器，是由两路基础 PWM 输出波形的逻辑与运算或者逻辑或运算组合而成。CCR1 和 CCR2 共同控制 CH1/2 的输出，CCR3 和 CCR4 共同控制 CH3/4 的输出。

CH1/2 以及 CH3/4 可以独立选择不同的组合 PWM 模式，配置 CCMRx_OCxM 为 1100(0xc) 或 1101(0xd)。当 CH1 或 CH3 配置为组合 PWM 模式 1100(0xc) 时，CH2 或 CH4 必须配置为 0111(0x7) 或 1101(0xd) 或 1111(0xf)。当 CH1 或 CH3 配置为组合 PWM 模式 1101(0xd) 时，CH2 或 CH4 必须配置为 0110(0x6) 或 1100(0xc) 或 1110(0xe)。

如配置 CCMR1_OC1M 为 1101(0xd)，CCMR1_OC2M 为 0110(0x6)，CCMR2_OC3M 为 1100(0xc)，CCMR2_OC4M 为 0111(0x7)，则 PWM 输出如图9-12。其中计数值 CNT 小于 CCR1/4 时，OC1REF/OC4REF 为低电平，否则为高电平；计数值 CNT 小于 CCR2/3 时，OC2REF/OC3REF 为高电平，否则为低电平。CH1 输出是 OC1REF 和 OC2REF 的逻辑与运算。CH3 输出是 OC3REF 和 OC4REF 的逻辑或运算。

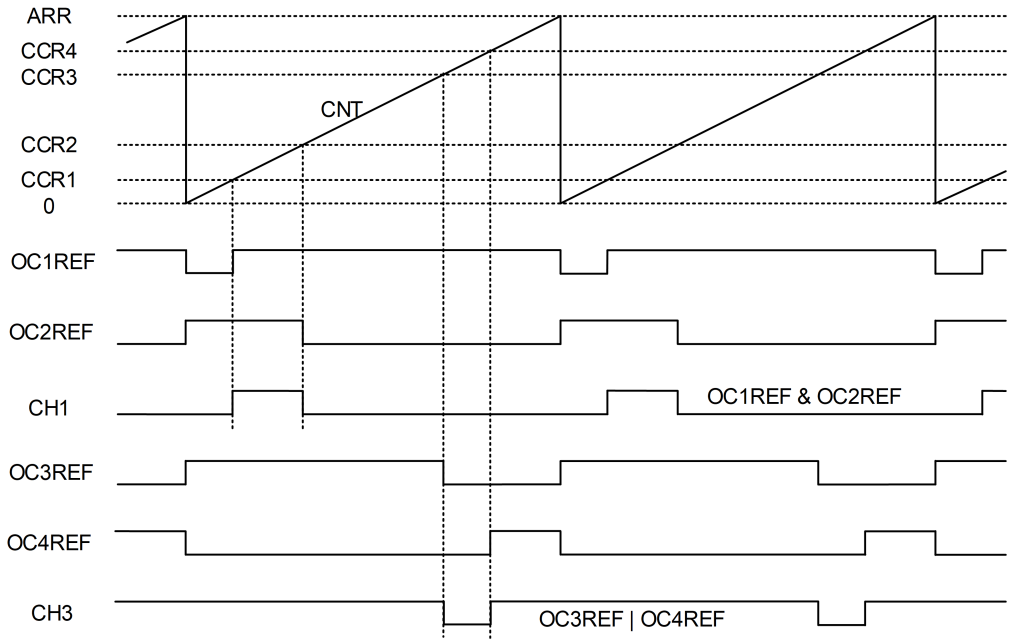


图 9-12: 组合 PWM 输出

9.3.3.13 单脉冲模式

将 CR1_OPM 写 1 可以使能单脉冲模式。该模式下计数器启动以后一旦发生更新事件，就会自动停止计数。该模式可以用于单次计数，或在一个激励信号的触发下启动，并在一段可编程的延时后产生一个脉宽可编程的脉冲。

例如，希望实现这样的功能，在 CH2 输入引脚检测到上升沿时，经过一定时间延迟，在 CH1 上产生单个一定宽度的正脉冲。配置方法如下：

1. CCMR1_CC2S=01，以将 TI2FP2 映射到通道 2。
2. CCER_CCxP 和 CCER_CCxNP 写 0，TI2FP2 反应 CH2 上升沿的变化。
3. SMCR_TS=110(0x6)，将 TI2FP2 配置为从模式控制器的触发 TRGI。
4. SMCR_SMS=110(0x6)，将从模式控制器配置为触发模式，触发后开启计数。
5. 根据需要的时间延迟与脉冲宽度配置 ARR 与 CCR1，定义时间延迟与脉冲宽度。
6. CCMR1_OC1M=0111(0x7)，配置为正脉冲 PWM。
7. CR1_OPM=1，一次触发只产生一个脉冲。
8. EGR_UG=1，手动刷新 ARR 与 CCR1 寄存器。

从模式为触发模式时不需要手动使能 CR1_CEN，一旦检测到触发信号生效，计数器就会自动使能。

9.3.3.14 编码器接口模式

编码器接口模式下，通道 1 和通道 2 可以用于连接外部正交编码器，将外部编码器的信号转化为定时器的计数值变化，从而获知外部编码器的工作状态。

如果计数器仅在 CH1 边沿处计数，SMCR_SMS 配置为 0001；如果计数器仅在 CH2 边沿处计数，SMCR_SMS 配置为 0010(0x2)；如果计数器在 CH1 和 CH2 边沿处均计数，SMCR_SMS 配置为 0011(0x3)。CCER_CC1P/CC2P 用于选择 CH1 和 CH2 极性。如果需要，还可对输入滤波器进行编程。两个输入的信号转换序列会产生计数脉冲和方向信号，根据该信号转换序列，计数器相应递增或递减计数，同时硬件对 CR1_DIR 进行相应修改。

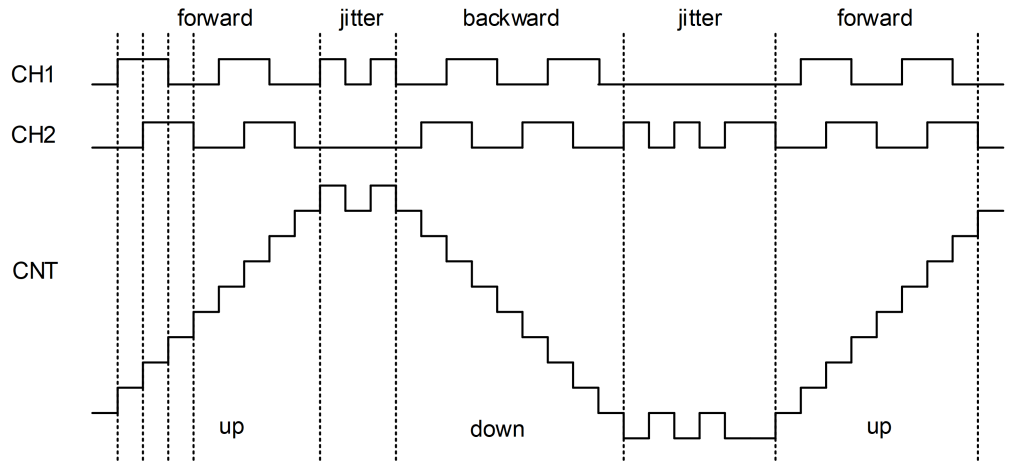
编码器接口模式下，计数器的计数事件是正交编码器接口的解码输出。计数器仅在 0 到 ARR 之间进行连续计数（根据计数的具体方向，从 0 递增计数到 ARR，或从 ARR 递减计数到 0）。因此，在启动前必须先配置 ARR。同样，捕获、比较、重复计数器和触发输出功能继续正常工作。在此模式下，计数器会根据正交编码器的速度和方向自动进行修改，因此，其内容始终表示编码器的位置。计数方向对应于所连传感器的旋转方向。下表汇总了可能的组合（假设 CH1 和 CH2 不同时切换）。

SMCR_SMS	条件	CH1 上升沿	CH1 上升沿	CH2 上升沿	CH2 上升沿
0001 或 0011	CH2=0	递增	递减	/	/
	CH2=1	递减	递增	/	/
0010 或 0011	CH1=0	/	/	递减	递增
	CH1=1	/	/	递增	递减

下图示意了计数器如何根据正交编码器的信号变化进行计数的，配置如下：

CCMR1_CC1S=01（CH1 映射到通道 1 上），CCMR2_CC2S=01（CH2 映射到通道 2 上），

CCER_CC1P/CC1NP/CC2P/CC2NP=0，SMCR_SMS=0011(0x3)，CR1_CEN=1。



9.3.3.15 定时器同步

多个定时器可通过主从模式连接在一起，实现定时器同步，以完成多级分频、同时启动、门控计数等功能。

将主模式定时器的 TRGO 设置为更新事件 (CR2_MMS=010)，连接至另一个设置为外部时钟从模式 (SMCR_SMS = 0111) 的定时器，可以实现定时器级联计数。此时主模式定时器相当于从模式定时器的预分频，计数总位宽等于两个定时器各自的位宽相加。

将主模式定时器的 TRGO 设置为计数使能 (CR2_MMS=001)，并设置从模式为触发从模式 (SMCR_SMS=0110)，同时连接至另一个设置为触发从模式 (SMCR_SMS=0110) 的定时器，可以实现多个定时器同步触发启动，从而对齐多个定时器的开启时机。该场景下主模式定时器还需将 SMCR_MSM 设为 1。

将主模式定时器的 TRGO 设置为比较输出 (CR2_MMS=100)，连接至另一个设置为门控从模式 (SMCR_SMS=0101) 的定时器，可以实现门控 PWM 输出。主模式定时器可以对从模式定时器输出的 PWM 载波进行调制输出。

9.3.3.16 通知机制

ATIM 能够产生中断、DMA 请求、PTC 触发等多种通知机制。能够触发通知的事件主要包括更新事件、触发事件、比较器匹配、输入捕获等。DIER 寄存器可以控制各种事件是否产生中断和 DMA 请求。各事件状态可在 SR 寄存器中查询。

9.3.4 GPTIM 寄存器

表 9-3: GPTIM 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00			**CR1**	TIM control register 1
[31:12]			RSVD	
[11]	rw	1'h0	UIFREMAP	UIF status bit remapping 0: No remapping. UIF status bit is not copied to CNT register bit 31 1: Remapping enabled. UIF status bit is copied to CNT register bit 31
[10:8]			RSVD	
[7]	rw	1'h0	ARPE	Auto-reload preload enable 0: ARR register is not buffered 1: ARR register is buffered

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表 9-3: GPTIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[6:5]	rw	2'h0	CMS	Center-aligned mode selection 00: Edge-aligned mode. The counter counts up or down depending on the direction bit (DIR). 01: Center-aligned mode 1. The counter counts up and down alternatively. Output compare interrupt flags of channels configured in output (CCxS=00 in CCMRx register) are set only when the counter is counting down. 10: Center-aligned mode 2. The counter counts up and down alternatively. Output compare interrupt flags of channels configured in output (CCxS=00 in CCMRx register) are set only when the counter is counting up. 11: Center-aligned mode 3. The counter counts up and down alternatively. Output compare interrupt flags of channels configured in output (CCxS=00 in CCMRx register) are set both when the counter is counting up or down.
[4]	rw	1'h0	DIR	Direction 0: Counter used as upcounter 1: Counter used as downcounter
[3]	rw	1'h0	OPM	One-pulse mode 0: Counter is not stopped at update event 1: Counter stops counting at the next update event (clearing the bit CEN)
[2]	rw	1'h0	URS	Update request source This bit is set and cleared by software to select the UEV event sources. 0: Any of the following events generate an update interrupt or DMA request if enabled. These events can be: Counter overflow/underflow Setting the UG bit Update generation through the slave mode controller 1: Only counter overflow/underflow generates an update interrupt or DMA request if enabled.
[1]	rw	1'h0	UDIS	Update disable This bit is set and cleared by software to enable/disable UEV event generation. 0: UEV enabled. The Update (UEV) event is generated by one of the following events: Counter overflow/underflow Setting the UG bit Update generation through the slave mode controller Buffered registers are then loaded with their preload values. 1: UEV disabled. The Update event is not generated, shadow registers keep their value (ARR, PSC, CCRx). However the counter and the prescaler are reinitialized if the UG bit is set or if a hardware reset is received from the slave mode controller.
[0]	rw	1'h0	CEN	Counter enable 0: Counter disabled 1: Counter enabled Note: External clock, gated mode and encoder mode can work only if the CEN bit has been previously set by software. However trigger mode can set the CEN bit automatically by hardware. CEN is cleared automatically in one-pulse mode, when an update event occurs.
0x04			**CR2**	TIM control register 2
[31:8]			RSVD	

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表 9-3: GPTIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[7]	rw	1'h0	TI1S	TI1 selection 0: The CH1 pin is connected to TI1 input 1: The CH1, CH2 and CH3 pins are connected to the TI1 input (XOR combination)
[6:4]	rw	3'h0	MMS	Master mode selection These bits allow to select the information to be sent in master mode to slave timers for synchronization (TRGO). The combination is as follows: 000: Reset - the UG bit from the EGR register is used as trigger output (TRGO). If the reset is generated by the trigger input (slave mode controller configured in reset mode) then the signal on TRGO is delayed compared to the actual reset. 001: Enable - the Counter enable signal is used as trigger output (TRGO). It is useful to start several timers at the same time or to control a window in which a slave timer is enabled. The Counter Enable signal is generated by a logic OR between CEN control bit and the trigger input when configured in gated mode. When the Counter Enable signal is controlled by the trigger input, there is a delay on TRGO, except if the master/slave mode is selected. 010: Update - The update event is selected as trigger output (TRGO). For instance a master timer can then be used as a prescaler for a slave timer. 011: Compare Pulse - The trigger output send a positive pulse when the CC1IF flag is to be set (even if it was already high), as soon as a capture or a compare match occurred. (TRGO) 100: Compare - OC1REF signal is used as trigger output (TRGO) 101: Compare - OC2REF signal is used as trigger output (TRGO) 110: Compare - OC3REF signal is used as trigger output (TRGO) 111: Compare - OC4REF signal is used as trigger output (TRGO)
[3]	rw	1'h0	CCDS	Capture/compare DMA selection 0: CCx DMA request sent when CCx event occurs 1: CCx DMA requests sent when update event occurs
[2:0]			RSVD	
0x08			**SMCR**	TIM slave mode control register
[31:20]			RSVD	

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表 9-3: GPTIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[19:16]	rw	4'h0	SMS	Slave mode selection When external signals are selected the active edge of the trigger signal (TRGI) is linked to the polarity selected on the external input. 0000: Slave mode disabled. 0001: Encoder mode 1 - Counter counts up/down on TI1FP1 edge depending on TI2FP2 level. 0010: Encoder mode 2 - Counter counts up/down on TI2FP2 edge depending on TI1FP1 level. 0011: Encoder mode 3 - Counter counts up/down on both TI1FP1 and TI2FP2 edges depending on the level of the other input. 0100: Reset Mode - Rising edge of the selected trigger input (TRGI) reinitializes the counter and generates an update of the registers. 0101: Gated Mode - The counter clock is enabled when the trigger input (TRGI) is high. The counter stops (but is not reset) as soon as the trigger becomes low. Both start and stop of the counter are controlled. 0110: Trigger Mode - The counter starts at a rising edge of the trigger TRGI (but it is not reset). Only the start of the counter is controlled. 0111: External Clock Mode 1 - Rising edges of the selected trigger (TRGI) clock the counter. 1000: Combined reset + trigger mode - Rising edge of the selected trigger input (TRGI) reinitializes the counter, generates an update of the registers and starts the counter.
[15]	rw	1'h0	ETP	External trigger polarity 0: ETR is non-inverted, active at high level or rising edge 1: ETR is inverted, active at low level or falling edge
[14]	rw	1'h0	ECE	External clock enable This bit enables External clock mode 2. 0: External clock mode 2 disabled 1: External clock mode 2 enabled. The counter is clocked by any active edge on the ETRF signal.
[13:12]	rw	2'h0	ETPS	External trigger prescaler External trigger signal ETRP frequency must be at most 1/4 of CK_INT frequency. A prescaler can be enabled to reduce ETRP frequency. It is useful when inputting fast external clocks. 00: Prescaler OFF 01: ETRP frequency divided by 2 10: ETRP frequency divided by 4 11: ETRP frequency divided by 8

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表 9-3: GPTIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[11:8]	rw	4'h0	ETF	External trigger filter This bit-field then defines the frequency used to sample ETRP signal and the length of the digital filter applied to ETRP. The digital filter is made of an event counter in which N consecutive events are needed to validate a transition on the output: 0000: No filter 0001: fSAMPLING=fCLK, N=2 0010: fSAMPLING=fCLK, N=4 0011: fSAMPLING=fCLK, N=8 0100: fSAMPLING=fCLK/2, N=6 0101: fSAMPLING=fCLK/2, N=8 0110: fSAMPLING=fCLK/4, N=6 0111: fSAMPLING=fCLK/4, N=8 1000: fSAMPLING=fCLK/8, N=6 1001: fSAMPLING=fCLK/8, N=8 1010: fSAMPLING=fCLK/16, N=5 1011: fSAMPLING=fCLK/16, N=6 1100: fSAMPLING=fCLK/16, N=8 1101: fSAMPLING=fCLK/32, N=5 1110: fSAMPLING=fCLK/32, N=6 1111: fSAMPLING=fCLK/32, N=8
[7]	rw	1'h0	MSM	Master/Slave mode 0: No action 1: The effect of an event on the trigger input (TRGI) is delayed to allow a perfect synchronization between the current timer and its slaves (through TRGO). It is useful if we want to synchronize several timers on a single external event.
[6:4]	rw	3'h0	TS	Trigger selection This bit-field selects the trigger input to be used to synchronize the counter. 000: Internal Trigger 0 (ITR0) 001: Internal Trigger 1 (ITR1) 010: Internal Trigger 2 (ITR2) 011: Internal Trigger 3 (ITR3) 100: TI1 Edge Detector (TI1F_ED) 101: Filtered Timer Input 1 (TI1FP1) 110: Filtered Timer Input 2 (TI2FP2) 111: External Trigger input (ETRF)
[3:0]			RSVD	
0x0C			**DIER**	TIM DMA/Interrupt enable register
[31:15]			RSVD	
[14]	rw	1'h0	TDE	Trigger DMA request enable 0: Trigger DMA request disabled. 1: Trigger DMA request enabled.
[13]			RSVD	
[12]	rw	1'h0	CC4DE	Capture/Compare 4 DMA request enable 0: CC4 DMA request disabled. 1: CC4 DMA request enabled
[11]	rw	1'h0	CC3DE	Capture/Compare 3 DMA request enable 0: CC3 DMA request disabled. 1: CC3 DMA request enabled.

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表 9-3: GPTIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[10]	rw	1'h0	CC2DE	Capture/Compare 2 DMA request enable 0: CC2 DMA request disabled. 1: CC2 DMA request enabled.
[9]	rw	1'h0	CC1DE	Capture/Compare 1 DMA request enable 0: CC1 DMA request disabled. 1: CC1 DMA request enabled.
[8]	rw	1'h0	UDE	Update DMA request enable 0: Update DMA request disabled. 1: Update DMA request enabled
[7]			RSVD	
[6]	rw	1'h0	TIE	Trigger interrupt enable 0: Trigger interrupt disabled. 1: Trigger interrupt enabled
[5]			RSVD	
[4]	rw	1'h0	CC4IE	Capture/Compare 4 interrupt enable 0: CC4 interrupt disabled. 1: CC4 interrupt enabled
[3]	rw	1'h0	CC3IE	Capture/Compare 3 interrupt enable 0: CC3 interrupt disabled. 1: CC3 interrupt enabled
[2]	rw	1'h0	CC2IE	Capture/Compare 2 interrupt enable 0: CC2 interrupt disabled. 1: CC2 interrupt enabled.
[1]	rw	1'h0	CC1IE	Capture/Compare 1 interrupt enable 0: CC1 interrupt disabled. 1: CC1 interrupt enabled
[0]	rw	1'h0	UIE	Update interrupt enable 0: Update interrupt disabled. 1: Update interrupt enabled
0x10			**SR**	TIM status register
[31:13]			RSVD	
[12]	rw0c	1'h0	CC4OF	Capture/Compare 4 overcapture flag
[11]	rw0c	1'h0	CC3OF	Capture/Compare 3 overcapture flag
[10]	rw0c	1'h0	CC2OF	Capture/Compare 2 overcapture flag
[9]	rw0c	1'h0	CC1OF	Capture/Compare 1 overcapture flag This flag is set by hardware only when the corresponding channel is configured in input capture mode. It is cleared by software by writing it to '0'. 0: No overcapture has been detected. 1: The counter value has been captured in CCR1 register while CC1IF flag was already set
[8:7]			RSVD	
[6]	rw0c	1'h0	TIF	Trigger interrupt flag This flag is set by hardware on trigger event (active edge detected on TRGI input when the slave mode controller is enabled in all modes but gated mode). It is set when the counter starts or stops when gated mode is selected. It is cleared by software. 0: No trigger event occurred. 1: Trigger interrupt pending.
[5]			RSVD	

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表 9-3: GPTIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[4]	rw0c	1'h0	CC4IF	Capture/Compare 4 interrupt flag
[3]	rw0c	1'h0	CC3IF	Capture/Compare 3 interrupt flag
[2]	rw0c	1'h0	CC2IF	Capture/Compare 2 interrupt flag
[1]	rw0c	1'h0	CC1IF	Capture/Compare 1 interrupt flag If channel CC1 is configured as output: This flag is set by hardware when the counter matches the compare value. It is cleared by software. 0: No match. 1: The content of the counter CNT has matched the content of the CCR1 register. If channel CC1 is configured as input: This bit is set by hardware on a capture. It is cleared by software or by reading the CCR1 register. 0: No input capture occurred. 1: The counter value has been captured in CCR1 register (An edge has been detected on IC1 which matches the selected polarity).
[0]	rw0c	1'h0	UIF	Update interrupt flag This bit is set by hardware on an update event. It is cleared by software. 0: No update occurred 1: Update interrupt pending. This bit is set by hardware when the registers are updated: At overflow or underflow and if UDIS=0 in the CR1 register. When CNT is reinitialized by software using the UG bit in EGR register, if URS=0 and UDIS=0 in the CR1 register. When CNT is reinitialized by a trigger event, if URS=0 and UDIS=0 in the CR1 register.
0x14			**EGR**	Event generation register
[31:7]			RSVD	
[6]	w	1'h0	TG	Trigger generation This bit is set by software in order to generate an event, it is automatically cleared by hardware. 0: No action 1: The TIF flag is set in SR register. Related interrupt or DMA transfer can occur if enabled.
[5]			RSVD	
[4]	w	1'h0	CC4G	Capture/compare 4 generation
[3]	w	1'h0	CC3G	Capture/compare 3 generation
[2]	w	1'h0	CC2G	Capture/compare 2 generation
[1]	w	1'h0	CC1G	Capture/compare 1 generation This bit is set by software in order to generate an event, it is automatically cleared by hardware. 0: No action 1: A capture/compare event is generated on channel 1: If channel CC1 is configured as output: CC1IF flag is set, Corresponding interrupt or DMA request is sent if enabled. If channel CC1 is configured as input: The current value of the counter is captured in CCR1 register. The CC1IF flag is set, the corresponding interrupt or DMA request is sent if enabled. The CC1OF flag is set if the CC1IF flag was already high.

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表 9-3: GPTIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[0]	w	1'h0	UG	Update generation This bit can be set by software, it is automatically cleared by hardware. 0: No action 1: Re-initialize the counter and generates an update of the registers. Note that the prescaler counter is cleared too (anyway the prescaler ratio is not affected). The counter is cleared if the center-aligned mode is selected or if DIR=0 (upcounting), else it takes the auto-reload value (ARR) if DIR=1 (downcounting).
0x18			**CCMR1**	TIM capture/compare mode register 1
[31:28]	rw	4'h0	OC2M	Output compare 2 mode
[27]	rw	1'h0	OC2PE	Output compare 2 preload enable
[26:25]			RSVD	
[24]	rw	1'h0	OC2CE	Output compare 2 clear enable

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表 9-3: GPTIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[23:20]	rw	4'h0	OC1M	Output compare 1 mode These bits define the behavior of the output reference signal OC1REF from which OC1 and OC1N are derived. OC1REF is active high whereas OC1 and OC1N active level depends on CC1P and CC1NP bits. 0000: Frozen - The comparison between the output compare register CCR1 and the counter CNT has no effect on the outputs.(this mode is used to generate a timing base). 0001: Set channel 1 to active level on match. OC1REF signal is forced high when the counter CNT matches the capture/compare register 1 (CCR1). 0010: Set channel 1 to inactive level on match. OC1REF signal is forced low when the counter CNT matches the capture/compare register 1 (CCR1). 0011: Toggle - OC1REF toggles when CNT=CCR1. 0100: Force inactive level - OC1REF is forced low. 0101: Force active level - OC1REF is forced high. 0110: PWM mode 1 - In upcounting, channel 1 is active as long as CNT<CCR1 else inactive. In downcounting, channel 1 is inactive (OC1REF='0) as long as CNT>CCR1 else active (OC1REF=1). 0111: PWM mode 2 - In upcounting, channel 1 is inactive as long as CNT<CCR1 else active. In downcounting, channel 1 is active as long as CNT>CCR1 else inactive. 1000: Retriggerable OPM mode 1 - In up-counting mode, the channel is active until a trigger event is detected (on TRGI signal). Then, a comparison is performed as in PWM mode 1 and the channels becomes inactive again at the next update. In down-counting mode, the channel is inactive until a trigger event is detected (on TRGI signal). Then, a comparison is performed as in PWM mode 1 and the channels becomes inactive again at the next update. 1001: Retriggerable OPM mode 2 - In up-counting mode, the channel is inactive until a trigger event is detected (on TRGI signal). Then, a comparison is performed as in PWM mode 2 and the channels becomes inactive again at the next update. In down-counting mode, the channel is active until a trigger event is detected (on TRGI signal). Then, a comparison is performed as in PWM mode 1 and the channels becomes active again at the next update. 1010: Reserved, 1011: Reserved, 1100: Combined PWM mode 1 - OC1REF has the same behavior as in PWM mode 1. OC1REFC is the logical OR between OC1REF and OC2REF. 1101: Combined PWM mode 2 - OC1REF has the same behavior as in PWM mode 2. OC1REFC is the logical AND between OC1REF and OC2REF. 1110: Asymmetric PWM mode 1 - OC1REF has the same behavior as in PWM mode 1. OC1REFC outputs OC1REF when the counter is counting up, OC2REF when it is counting down. 1111: Asymmetric PWM mode 2 - OC1REF has the same behavior as in PWM mode 2. OC1REFC outputs OC1REF when the counter is counting up, OC2REF when it is counting down.
[19]	rw	1'h0	OC1PE	Output compare 1 preload enable 0: Preload register on CCR1 disabled. CCR1 can be written at anytime, the new value is taken in account immediately. 1: Preload register on CCR1 enabled. Read/Write operations access the preload register. CCR1 preload value is loaded in the active register at each update event.

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表 9-3: GPTIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[18:17]			RSVD	
[16]	rw	1'h0	OC1CE	Output compare 1 clear enable 0: OC1Ref is not affected by the ETRF input 1: OC1Ref is cleared as soon as a High level is detected on ETRF input
[15:12]	rw	4'h0	IC2F	Input capture 2 filter
[11:10]	rw	2'h0	IC2PSC	Input capture 2 prescaler
[9:8]	rw	2'h0	CC2S	Capture/Compare 2 selection This bit-field defines the direction of the channel (input/output) as well as the used input. 00: CC2 channel is configured as output 01: CC2 channel is configured as input, IC2 is mapped on TI2 10: CC2 channel is configured as input, IC2 is mapped on TI1 11: CC2 channel is configured as input, IC2 is mapped on TRC. This mode is working only if an internal trigger input is selected through the TS bit (SMCR register)
[7:4]	rw	4'h0	IC1F	Input capture 1 filter This bit-field defines the frequency used to sample TI1 input and the length of the digital filter applied to TI1. The digital filter is made of an event counter in which N consecutive events are needed to validate a transition on the output: 0000: No filter, sampling is done at fCLK 0001: fSAMPLING=fCLK, N=2 0010: fSAMPLING=fCLK, N=4 0011: fSAMPLING=fCLK, N=8 0100: fSAMPLING=fCLK/2, N=6 0101: fSAMPLING=fCLK/2, N=8 0110: fSAMPLING=fCLK/4, N=6 0111: fSAMPLING=fCLK/4, N=8 1000: fSAMPLING=fCLK/8, N=6 1001: fSAMPLING=fCLK/8, N=8 1010: fSAMPLING=fCLK/16, N=5 1011: fSAMPLING=fCLK/16, N=6 1100: fSAMPLING=fCLK/16, N=8 1101: fSAMPLING=fCLK/32, N=5 1110: fSAMPLING=fCLK/32, N=6 1111: fSAMPLING=fCLK/32, N=8
[3:2]	rw	2'h0	IC1PSC	Input capture 1 prescaler This bit-field defines the ratio of the prescaler acting on CC1 input (IC1). The prescaler is reset as soon as CC1E=0. 00: no prescaler, capture is done each time an edge is detected on the capture input 01: capture is done once every 2 events 10: capture is done once every 4 events 11: capture is done once every 8 events

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表 9-3: GPTIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[1:0]	rw	2'h0	CC1S	Capture/Compare 1 selection This bit-field defines the direction of the channel (input/output) as well as the used input. 00: CC1 channel is configured as output 01: CC1 channel is configured as input, IC1 is mapped on TI1 10: CC1 channel is configured as input, IC1 is mapped on TI2 11: CC1 channel is configured as input, IC1 is mapped on TRC. This mode is working only if an internal trigger input is selected through TS bit (SMCR register)
0x1C			**CCMR2**	TIM capture/compare mode register 2
[31:28]	rw	4'h0	OC4M	Output compare 4 mode
[27]	rw	1'h0	OC4PE	Output compare 4 preload enable
[26:25]			RSVD	
[24]	rw	1'h0	OC4CE	Output compare 4 clear enable
[23:20]	rw	4'h0	OC3M	Output compare 3 mode
[19]	rw	1'h0	OC3PE	Output compare 3 preload enable
[18:17]			RSVD	
[16]	rw	1'h0	OC3CE	Output compare 3 clear enable
[15:12]	rw	4'h0	IC4F	Input capture 4 filter
[11:10]	rw	2'h0	IC4PSC	Input capture 4 prescaler
[9:8]	rw	2'h0	CC4S	Capture/Compare 4 selection This bit-field defines the direction of the channel (input/output) as well as the used input. 00: CC4 channel is configured as output 01: CC4 channel is configured as input, IC4 is mapped on TI4 10: CC4 channel is configured as input, IC4 is mapped on TI3 11: CC4 channel is configured as input, IC4 is mapped on TRC. This mode is working only if an internal trigger input is selected through TS bit (SMCR register)
[7:4]	rw	4'h0	IC3F	Input capture 3 filter
[3:2]	rw	2'h0	IC3PSC	Input capture 3 prescaler
[1:0]	rw	2'h0	CC3S	Capture/Compare 3 selection This bit-field defines the direction of the channel (input/output) as well as the used input. 00: CC3 channel is configured as output 01: CC3 channel is configured as input, IC3 is mapped on TI3 10: CC3 channel is configured as input, IC3 is mapped on TI4 11: CC3 channel is configured as input, IC3 is mapped on TRC. This mode is working only if an internal trigger input is selected through TS bit (SMCR register)
0x20			**CCER**	Capture/Compare enable register
[31:16]			RSVD	
[15]	rw	1'h0	CC4NP	Capture/Compare 4 output Polarity.
[14]			RSVD	
[13]	rw	1'h0	CC4P	Capture/Compare 4 output Polarity.
[12]	rw	1'h0	CC4E	Capture/Compare 4 output enable.
[11]	rw	1'h0	CC3NP	Capture/Compare 3 output Polarity.
[10]			RSVD	
[9]	rw	1'h0	CC3P	Capture/Compare 3 output Polarity.

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表 9-3: GPTIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[8]	rw	1'h0	CC3E	Capture/Compare 3 output enable.
[7]	rw	1'h0	CC2NP	Capture/Compare 2 output Polarity.
[6]			RSVD	
[5]	rw	1'h0	CC2P	Capture/Compare 2 output Polarity.
[4]	rw	1'h0	CC2E	Capture/Compare 2 output enable.
[3]	rw	1'h0	CC1NP	Capture/Compare 1 output Polarity. CC1 channel configured as output: CC1NP must be kept cleared in this case. CC1 channel configured as input: This bit is used in conjunction with CC1P to define TI1FP1/TI2FP1 polarity. refer to CC1P description.
[2]			RSVD	
[1]	rw	1'h0	CC1P	Capture/Compare 1 output Polarity. CC1 channel configured as output: 0: OC1 active high 1: OC1 active low CC1 channel configured as input: CC1NP/CC1P bits select TI1FP1 and TI2FP1 polarity for trigger or capture operations. 00: noninverted/rising edge Circuit is sensitive to TIxFP1 rising edge (capture, trigger in reset, external clock or trigger mode), TIxFP1 is not inverted (trigger in gated mode, encoder mode). 01: inverted/falling edge Circuit is sensitive to TIxFP1 falling edge (capture, trigger in reset, external clock or trigger mode), TIxFP1 is inverted (trigger in gated mode, encoder mode). 10: reserved, do not use this configuration. 11: noninverted/both edges Circuit is sensitive to both TIxFP1 rising and falling edges (capture, trigger in reset, external clock or trigger mode), TIxFP1 is not inverted (trigger in gated mode). This configuration must not be used for encoder mode.
[0]	rw	1'h0	CC1E	Capture/Compare 1 output enable. CC1 channel configured as output: 0: Off - OC1 is not active 1: On - OC1 signal is output on the corresponding output pin CC1 channel configured as input: This bit determines if a capture of the counter value can actually be done into the input capture/compare register 1 (CCR1) or not. 0: Capture disabled 1: Capture enabled
0x24			**CNT**	Counter
[31]	r	1'h0	UIFCPY	Value depends on IUFREMAP in CR1. If UIFREMAP = 1 UIFCPY: UIF Copy This bit is a read-only copy of the UIF bit of the ISR register
[30:16]			RSVD	
[15:0]	rw	16'h0	CNT	counter value
0x28			**PSC**	Prescaler
[31:16]			RSVD	

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表 9-3: GPTIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[15:0]	rw	16'h0	PSC	Prescaler value The counter clock frequency is equal to fCLK / (PSC[15:0] + 1). PSC contains the value to be loaded in the active prescaler register at each update event (including when the counter is cleared through UG bit of EGR register or through trigger controller when configured in 'reset mode').
0x2C			**ARR**	Auto-reload register
[31:16]			RSVD	
[15:0]	rw	16'h0	ARR	Auto-reload value ARR is the value to be loaded in the actual auto-reload register.
0x30			**RCR**	Repetition counter register
[31:8]			RSVD	
[7:0]	rw	8'h0	REP	Repetition counter value These bits allow the user to set-up the update rate of the compare registers (i.e. periodic transfers from preload to active registers) when preload registers are enable, as well as the update interrupt generation rate, if this interrupt is enable. Each time the REP_CNT related downcounter reaches zero, an update event is generated and it restarts counting from REP value. As REP_CNT is reloaded with REP value only at the repetition update event, any write to the RCR register is not taken in account until the next repetition update event. It means in PWM mode (REP+1) corresponds to the number of PWM periods in edge-aligned mode.
0x34			**CCR1**	Capture/Compare register 1
[31:16]			RSVD	
[15:0]	rw	16'h0	CCR1	Capture/Compare 1 value If channel CC1 is configured as output: CCR1 is the value to be loaded in the actual capture/compare 1 register (preload value).It is loaded permanently if the preload feature is not selected in the CCMR1 register (bit OC1PE). Else the preload value is copied in the active capture/compare 1 register when an update event occurs. The active capture/compare register contains the value to be compared to the counter CNT and signaled on OC1 output. If channel CC1is configured as input: CCR1 is the counter value transferred by the last input capture 1 event (IC1). The CCR1 register is read-only and cannot be programmed.
0x38			**CCR2**	Capture/Compare register 2
[31:16]			RSVD	
[15:0]	rw	16'h0	CCR2	Capture/Compare 2 value If channel CC2 is configured as output: CCR2 is the value to be loaded in the actual capture/compare 2 register (preload value).It is loaded permanently if the preload feature is not selected in the CCMR1 register (bit OC2PE). Else the preload value is copied in the active capture/compare 2 register when an update event occurs. The active capture/compare register contains the value to be compared to the counter CNT and signalled on OC2 output. If channel CC2 is configured as input: CCR2 is the counter value transferred by the last input capture 2 event (IC2). The CCR2 register is read-only and cannot be programmed.
0x3C			**CCR3**	Capture/Compare register 3
[31:16]			RSVD	

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表 9-3: GPTIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[15:0]	rw	16'h0	CCR3	Capture/Compare value If channel CC3 is configured as output: CCR3 is the value to be loaded in the actual capture/compare 3 register (preload value).It is loaded permanently if the preload feature is not selected in the CCMR2 register (bit OC3PE). Else the preload value is copied in the active capture/compare 3 register when an update event occurs. The active capture/compare register contains the value to be compared to the counter CNT and signalled on OC3 output. If channel CC3is configured as input: CCR3 is the counter value transferred by the last input capture 3 event (IC3). The CCR3 register is read-only and cannot be programmed.
0x40			**CCR4**	Capture/Compare register 4
[31:16]			RSVD	
[15:0]	rw	16'h0	CCR4	Capture/Compare value 1. if CC4 channel is configured as output: CCR4 is the value to be loaded in the actual capture/compare 4 register (preload value).It is loaded permanently if the preload feature is not selected in the CCMR2 register (bit OC4PE). Else the preload value is copied in the active capture/compare 4 register when an update event occurs. The active capture/compare register contains the value to be compared to the counter CNT and signalled on OC4 output. 2. if CC4 channel is configured as input: CCR4 is the counter value transferred by the last input capture 4 event (IC4). The CCR4 register is read-only and cannot be programmed.

9.3.5 定时器级联

表 9-4: 定时器级联

下级定时器	级联端口	上级定时器
ATIM1	ITR0	BTIM2
	ITR1	GPTIM2
	ITR2	GPTIM1
	ITR3	BTIM1
GPTIM1	ITR0	GPTIM2
	ITR1	BTIM2
	ITR2	ATIM1
	ITR3	BTIM1
GPTIM2	ITR0	GPTIM1
	ITR1	ATIM1
	ITR2	BTIM1
	ITR3	BTIM2
BTIM1	ITR0	BTIM2
	ITR1	/
	ITR2	ATIM1
	ITR3	GPTIM2

续表下页...

表 9-4: 定时器级联（续）

下级定时器	级联端口	上级定时器
BTIM2	ITR0	GPTIM1
	ITR1	BTIM1
	ITR2	/
	ITR3	ATIM1
GPTIM3	ITR0	BTIM3
	ITR1	BTIM4
	ITR2	GPTIM4
	ITR3	GPTIM5
GPTIM4	ITR0	GPTIM3
	ITR1	GPTIM5
	ITR2	BTIM3
	ITR3	BTIM4
GPTIM5	ITR0	GPTIM3
	ITR1	GPTIM4
	ITR2	BTIM3
	ITR3	BTIM4
BTIM3	ITR0	GPTIM3
	ITR1	GPTIM4
	ITR2	GPTIM5
	ITR3	BTIM4
BTIM4	ITR0	/
	ITR1	/
	ITR2	GPTIM4
	ITR3	BTIM3

9.4 LPTIM

芯片共有 3 个 LPTIM，其中 LPTIM 1 位于 HPSYS_AON，在 HPSYS 进入低功耗模式时 (除 hibernate 外) 能够保持工作，输入输出连接至 IO(PA)；LPTIM2 和 LPTIM3 位于 LPSYS_AON，在 LPSYS 进入低功耗模式时 (除 hibernate 外) 能够保持工作，输入输出连接至 IO(PB) 与 IO(PBR)。

9.4.1 简介

LPTIM (Low Power Timer) 基于一个 24 比特递增计数器，可实现计时、产生输出波形 (输出比较和 PWM) 和唤醒系统等功能。计数时钟可以为系统时钟，低功耗时钟，IO 输入信号或比较器输出，并可进行最多 128 倍的预分频以及最多 256 次的循环计数。根据计数结果可以产生 PWM 输出，并可产生中断，或产生唤醒信号将系统从低功耗模式唤醒。当用 IO 输入信号作为计数时钟时，支持不依赖于内部时钟进行计数并产生唤醒信号。

9.4.2 主要特性

- 24 位向上自动重装载计数器，最大计数 16777215(2^{24}-1)
- 计数时钟选择

  - 内部时钟，PCLK2 或低功耗时钟
  - 可选边沿的 IO 输入信号或比较器输出，可利用内部时钟进行防抖动，也可不依赖内部时钟独立计数
- 8 档预分频，计数时钟分频系数为 2 的 0~7 次方
- 1~256 循环次数
- 计数模式
  - 连续计数模式
  - 单笔计数模式，循环次数完成后计数结束
- 可配极性的输出模式
  - PWM 输出，可配脉宽，周期
  - 单次翻转输出
  - 单脉冲或指定个数脉冲输出
- 触发模式
  - 软件触发
  - IO 输入信号边沿触发，支持防抖动滤波
- 超时检测，每次外部触发时计数器复位
- 如下事件发生时产生中断或唤醒信号：
  - 更新
  - 计数器溢出
  - 输出比较
  - 外部触发

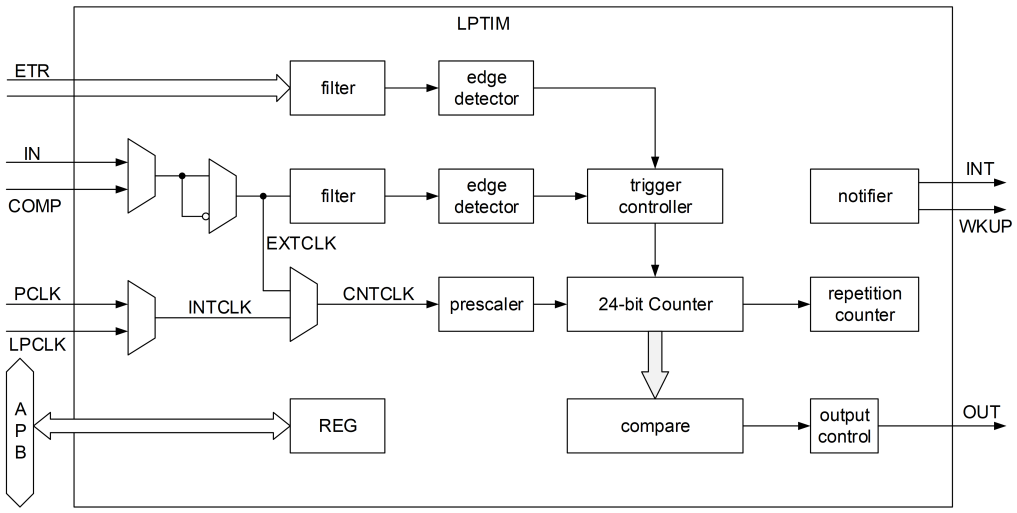

图 9-13: LPTIM 结构图

9.4.3 LPTIM 功能描述

9.4.3.1 计数器

LPTIM 的各项功能均基于一个 24 比特的计数器。计数器基于事件计数，包括时钟翻转、外部输入翻转、比较器结果翻转等。

计数事件经过预分频处理才会真正进入计数器。预分频的次数介于 1 到 128 之间 $(2^{CFGR\_PRESCPSC})$，即仅当发生了 $(2^{CFGR\_PRESCPSC})$ 次计数事件，计数器的值才真正改变一次。

计数器固定为递增计数模式，计数器从 0 计数到自动重载值 ARR，然后重新从 0 开始计数并产生计数器上溢事件。

计数值可以通过 CNT 读出。由于计数时钟与 APB 时钟异步，需要连续两次读取的数值相同才能认为是一次有效数据读取。

9.4.3.2 计数时钟

LPTIM 计数器的计数时钟 CNTCLK 可以在多个来源中选择。最常用的默认模式是选择内部低功耗时钟 LPCLK，此时 LPTIM 可以在芯片进入低功耗睡眠模式以后继续保持工作。当不处于低功耗睡眠模式时，LPTIM 也可以选择内部 PCLK 做时钟。LPTIM 还能够不依赖于内部时钟，直接用外部信号 IN 或者比较器输出信号 COMP 做时钟进行计数。时钟选择相关的寄存器包括 CFGR_EXTCKSEL/INTCKSEL/CKSEL。外部时钟的极性可以用 CFGR_CKPOL 选择。

当选择内部时钟时，还可以对外部信号 IN 或者比较器输出信号 COMP 翻转的事件进行计数，并能够进行预滤波和边沿选择处理。这种模式下应保证内部时钟的翻转频率至少为外部信号 IN 或者比较器输出信号 COMP 翻转频率的五倍。

9.4.3.3 更新事件 (UEV)

更新事件用于标志一个计数单元的结束。最基本的更新事件产生于每次计数器上溢时 (未开启重复计数时)。更新事件可以产生中断和唤醒信号，是定时器最基本的一项通知功能。

9.4.3.4 重复计数

如果配置了重复计数器 (RCR>0)，每次计数器上溢时重复计数器会递减，并仅当重复计数器为 0 时才产生更新事件。

重复计数器的当前值可以通过 RCR 读出。由于计数时钟与 APB 时钟异步，需要连续两次读取的数值相同才能认为是一次有效数据读取。

9.4.3.5 计数器触发

计数器可配置为一级触发模式 (CFGR_TRIGEN=00) 或两级触发模式 (CFGR_TRIGEN!=00)。

一级触发模式为软件触发，包括单次触发和连续触发两种。触发前，需先将 CR_ENABLE 置 1 使能计数器。随后将 CR_SNGSTRT 置 1 启动单次触发，计数器即刻启动，并在更新事件后停止；或将 CR_CNTSTRT 置 1 启动连续触发，计数器即刻启动持续计数直到计数器关闭使能或复位。

两级触发模式在软件触发基础上增加硬件触发机制，仅当经过滤波的 ETR 可选边沿到来时才真正启动计数器。

9.4.3.6 超时监测

在两级触发模式下，如果将 CFGR_TIMOUT 置 1，则每次硬件触发时均会复位计数器并重新启动计数。该功能可用于监测两个连续触发信号之间的间隔，当间隔超出预期时产生比较或更新事件。

9.4.3.7 PWM 输出

LPTIM 可以产生周期、占空比可控的单路 PWM 输出至 OUT 端口。PWM 输出的周期由 ARR 决定，占空比由 CMP 决定。计数器值 CNT 与 CMP 进行比较，生成 PWM，极性通过 CFGR_WAVEPOL 配置。单次触发模式下，根据 RCR 的值可生成单个或多个脉冲。连续触发模式下可生成持续的 PWM。如果 CFGR_WAVE 为 1，可以生成单次置 1 波形。

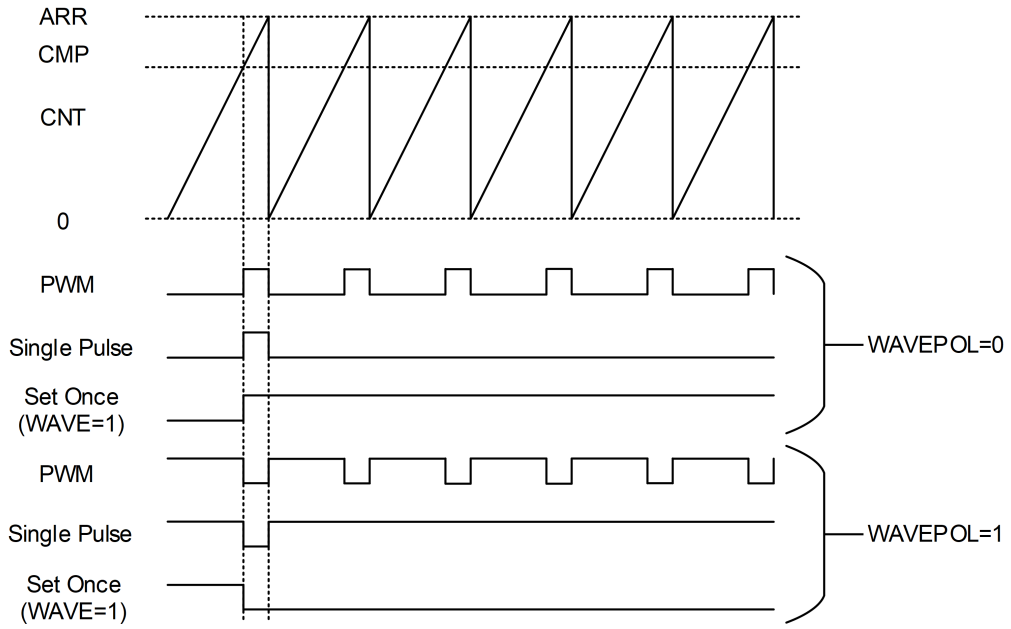

图 9-14: PWM 输出

9.4.3.8 通知机制

LPTIM 能够产生中断和唤醒等通知。中断仅在系统处于非低功耗睡眠状态时产生。唤醒信号无论系统是否处于低功耗睡眠状态均可产生，并能够将系统唤醒。能够触发通知的事件主要包括上溢事件、更新事件、触发事件、比较器匹配等。IER 寄存器可以控制各种事件是否产生中断和唤醒。各事件状态可在 ISR 寄存器中查询。

9.4.4 LPTIM 寄存器

表 9-5: LPTIM 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00			**ISR**	LPTIM interrupt and status register
[31:11]			RSVD	
[10]	r	1'h0	OCWKUP	Indicates output compare wakeup occurred The OCWKUP bit is set by hardware when LPTIM_CNT register value reached the LPTIM_CMP register's value. To clear OCWKUP, first write 0 to the OCWE bit in the LPTIM_IER register to disable, then write 1 to the WKUPCLR bit in the LPTIM_ICR register.

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表 9-5: LPTIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[9]	r	1'h0	OFWKUP	Indicates overflow wakeup occurred OFWKUP is set by hardware when LPTIM_CNT register's value reached the LPTIM_ARR register's value and count from zero again. To clear OFWKUP, first write 0 to the OFWE bit in the LPTIM_IER register to disable, then write 1 to the WKUPCLR bit in the LPTIM_ICR register.
[8]	r	1'h0	UEWKUP	Indicates update event wakeup occurred UEWKUP is set by hardware when an update event was generated (overflow occurred while repetition counter reached zero). To clear UEWKUP, first write 0 to the UEWE bit in the LPTIM_IER register to disable, then write 1 to the WKUPCLR bit in the LPTIM_ICR register.
[7:4]			RSVD	
[3]	r	1'h0	ET	External trigger edge event ET is set by hardware to inform application that a valid edge on the selected external trigger input has occurred. If the trigger is ignored because the timer has already started, then this flag is not set. ET flag can be cleared by writing 1 to the ETCLR bit in the LPTIM_ICR register.
[2]	r	1'h0	OC	Output compare match The OC bit is set by hardware to inform application that LPTIM_CNT register value reached the LPTIM_CMP register's value. OC flag can be cleared by writing 1 to the OCCLR bit in the LPTIM_ICR register.
[1]	r	1'h0	OF	Overflow occurred OF is set by hardware to inform application that LPTIM_CNT register's value reached the LPTIM_ARR register's value and count from zero again. OF flag can be cleared by writing 1 to the OFCLR bit in the LPTIM_ICR register.
[0]	r	1'h0	UE	LPTIM update event occurred UE is set by hardware to inform application that an update event was generated when overflow occurred while repetition counter reached zero. UE flag can be cleared by writing 1 to the UECLR bit in the LPTIM_ICR register.
0x04			**ICR**	LPTIM interrupt and status clear register
[31:9]			RSVD	
[8]	w	1'h0	WKUPCLR	wakeup status clear flag Writing 1 to this bit clears all wakeup status flags in the LPTIM_ISR register.
[7:4]			RSVD	
[3]	w	1'h0	ETCLR	External trigger valid edge clear flag Writing 1 to this bit clears the ET flag in the LPTIM_ISR register
[2]	w	1'h0	OCCLR	Output compare clear flag Writing 1 to this bit clears the OC flag in the LPTIM_ISR register
[1]	w	1'h0	OFCLR	Overflow clear flag Writing 1 to this bit clears the OF flag in the LPTIM_ISR register
[0]	w	1'h0	UECLR	Update event clear flag Writing 1 to this bit clear the UE flag in the LPTIM_ISR register.
0x08			**IER**	LPTIM interrupt and wakeup enable register
[31:11]			RSVD	
[10]	rw	1'h0	OCWE	Output compare Wakeup Enable 0: Output compare wakeup disabled 1: Output compare wakeup enabled
[9]	rw	1'h0	OFWE	Overflow Wakeup Enable 0: Overflow Wakeup disabled 1: Overflow Wakeup enabled

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表 9-5: LPTIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[8]	rw	1'h0	UEWE	Update event Wakeup enable 0: Update event Wakeup disabled 1: Update event Wakeup enabled
[7:4]			RSVD	
[3]	rw	1'h0	ETIE	External trigger valid edge Interrupt Enable 0: External trigger interrupt disabled 1: External trigger interrupt enabled
[2]	rw	1'h0	OCIE	Output compare Interrupt Enable 0: Output compare interrupt disabled 1: Output compare interrupt enabled
[1]	rw	1'h0	OFIE	Overflow Interrupt Enable 0: Overflow interrupt disabled 1: Overflow interrupt enabled
[0]	rw	1'h0	UEIE	Update event interrupt enable 0: Update event interrupt disabled 1: Update event interrupt enabled
0x0C			**CFGR**	LPTIM configuration register
[31:24]			RSVD	
[23]	rw	1'h0	COUNTMODE	counter mode in internal clock source mode (CKSEL=0). If CKSEL=1, this bit has no effect. 0: the counter is incremented following each internal clock pulse 1: the counter is incremented following each valid pulse on the external clock
[22]			RSVD	
[21]	rw	1'h0	WAVPOL	Waveform shape polarity The WAVEPOL bit controls the output polarity 0: The LPTIM output reflects the compare results between LPTIM_ARR and LPTIM_CMP registers 1: The LPTIM output reflects the inverse of the compare results between LPTIM_ARR and LPTIM_CMP registers
[20]	rw	1'h0	WAVE	Waveform shape The WAVE bit controls the output shape 0: Deactivate Set-once mode 1: Activate the Set-once mode
[19]	rw	1'h0	TIMOUT	Timeout enable The TIMOUT bit controls the Timeout feature 0: A trigger event arriving when the timer is already started will be ignored 1: A trigger event arriving when the timer is already started will reset and restart the LPTIM counter and the repetition counter
[18:17]	rw	2'h0	TRIGEN	Trigger enable and polarity The TRIGEN bits controls whether the LPTIM counter is started by an external trigger or not. If the external trigger option is selected, three configurations are possible for the trigger active edge: 00: software trigger (counting start is initiated by software) 01: rising edge is the active edge 10: falling edge is the active edge 11: both edges are active edges
[16]			RSVD	

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表 9-5: LPTIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[15:13]	rw	3'h0	TRIGSEL	Trigger selector The TRIGSEL bits select the trigger source that will serve as a trigger event for the LPTIM among the below 8 available sources: 000: lptim_ext0 001: lptim_ext1 010: lptim_ext2 011: lptim_ext3 100: lptim_ext4 101: lptim_ext5 110: lptim_ext6 111: lptim_ext7
[12]			RSVD	
[11:9]	rw	3'h0	PRESC	Clock prescaler The PRESC bits configure the prescaler division factor. It can be one among the following division factors: 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128
[8]	rw	1'h0	EXTCKSEL	External clock source selector 0: external clock source is from lptim_in 1: external clock source is from LPCOMP (if LPCOMP integrated)
[7:6]	rw	2'h0	TRGFLT	Configurable digital filter for trigger The TRGFLT value sets the number of consecutive equal samples that should be detected when a level change occurs on an internal trigger before it is considered as a valid level transition. An internal clock source must be present to use this feature 00: any trigger active level change is considered as a valid trigger 01: trigger active level change must be stable for at least 2 clock periods before it is considered as valid trigger. 10: trigger active level change must be stable for at least 4 clock periods before it is considered as valid trigger. 11: trigger active level change must be stable for at least 8 clock periods before it is considered as valid trigger.
[5]	rw	1'h0	INTCKSEL	Internal clock source selector 0: internal clock source is clk_lp 1: internal clock source is pclk2

续表下页...

表 9-5: LPTIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[4:3]	rw	2'h0	CKFLT	Configurable digital filter for external clock The CKFLT value sets the number of consecutive equal samples that should be detected when a level change occurs on an external clock signal before it is considered as a valid level transition. An internal clock source must be present to use this feature 00: any external clock signal level change is considered as a valid transition 01: external clock signal level change must be stable for at least 2 clock periods before it is considered as valid transition. 10: external clock signal level change must be stable for at least 4 clock periods before it is considered as valid transition. 11: external clock signal level change must be stable for at least 8 clock periods before it is considered as valid transition.
[2:1]	rw	2'h0	CKPOL	Clock Polarity If LPTIM is clocked by an external clock source, CKPOL bits is used to configure the active edge or edges used by the counter: 00: the rising edge is the active edge used for counting 01: the falling edge is the active edge used for counting 10: both edges are active edges. When both external clock signal edges are considered active ones, the LPTIM must also be clocked by an internal clock source with a frequency equal to at least four time the external clock frequency. 11: not allowed
[0]	rw	1'h0	CKSEL	Clock selector The CKSEL bit selects which clock source the LPTIM will use: 0: LPTIM is clocked by internal clock source, according to INTCKSEL 1: LPTIM is clocked by external clock source, according to EXTCKSEL
0x10			**CR**	LPTIM control register
[31:4]			RSVD	
[3]	rw	1'h0	COUNTRST	Counter reset This bit is set by software and cleared by hardware. When set to 1 this bit will trigger a synchronous reset of the CNT register. Due to the synchronous nature of this reset, it only takes place after a synchronization delay. COUNTRST must never be set to 1 by software before it is already cleared to 0 by hardware. Software should consequently check that COUNTRST bit is already cleared to 0 before attempting to set it to 1.
[2]	w	1'h0	CNTSTRT	Timer start in Continuous mode This bit is set by software and cleared by hardware. In case of software start (TRIGEN[1:0] = 00), setting this bit starts the LPTIM in Continuous mode. If the software start is disabled (TRIGEN[1:0] different than 00), setting this bit starts the timer in Continuous mode as soon as an external trigger is detected. If this bit is set when a single pulse mode counting is ongoing, then the timer will not stop at the next match between ARR and CNT registers and the LPTIM counter keeps counting in Continuous mode.

续表下页...

表 9-5: LPTIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[1]	w	1'h0	SNGSTRT	LPTIM start in Single mode This bit is set by software and cleared by hardware. In case of software start (TRIGEN[1:0] = 00), setting this bit starts the LPTIM in single pulse mode. If the software start is disabled (TRIGEN[1:0] different than 00), setting this bit starts the LPTIM in single pulse mode as soon as an external trigger is detected. If this bit is set when the LPTIM is in continuous counting mode, then the LPTIM will stop at the following match between ARR and CNT registers. If this bit is set simultaneously with CNTSTRT, then LPTIM will be in continuous counting mode.
[0]	rw	1'h0	ENABLE	LPTIM enable The ENABLE bit is set and cleared by software. 0:LPTIM is disabled 1:LPTIM is enabled
0x14			**CMP**	LPTIM compare register
[31:24]			RSVD	
[23:0]	rw	24'h0	CMP	Compare value CMP is the compare value used by the LPTIM.
0x18			**ARR**	LPTIM autoreload register
[31:24]			RSVD	
[23:0]	rw	24'h0	ARR	Auto reload value ARR is the autoreload value for the LPTIM. This value must be strictly greater than the CMP[15:0] value.
0x1C			**CNT**	LPTIM counter register
[31:24]			RSVD	
[23:0]	r	24'h0	CNT	Counter value When the LPTIM is running with an asynchronous clock, reading the CNT register may return unreliable values. So in this case it is necessary to perform two consecutive read accesses and verify that the two returned values are identical.
0x20			**RCR**	LPTIM repetition register
[31:8]			RSVD	
[7:0]	rw	8'h0	REP	Repetition register value REP is the repetition value for the LPTIM. Read REP will return left repetition times. It should be noted that for a reliable REP register read access, two consecutive read accesses must be performed and compared. A read access can be considered reliable when the values of the two consecutive read accesses are equal.

9.5 WDT

芯片共有 3 个 WDT，其中 WDT1 位于 HPSYS，当 HPSYS 进入 deepsleep，standby 或 hibernate 模式后停止工作；WDT2 位于 LPSYS，当 LPSYS 进入 deepsleep，standby 或 hibernate 模式后停止工作；IWDT 位于 AON，当芯片进入低功耗模式以后仍能保持工作。具体每个 WDT 的复位作用域可参考时钟与复位章节。

9.5.1 简介

看门狗计时器作为一种计数器主要是用于在到达设定好的时间之后重置系统，以防止软件挂死。

看门狗计时器基本功能：

- 支持两种工作模式：
  - mode0
    - wdt 不会产生中断，在到达设定的时间之后会直接重置系统。
    - 最高支持 24bit 的计数器
  - mode1
    - 分为两段计数，在到达第一段设定的时间之后，会产生中断，在到达第二段设定的时间之后，再重置系统。
    - 每个时间段最高支持 24bit 的计数器
- 支持写保护，以防止软件对 wdt 进行误操作

9.5.2 WDT 的工作方式

wdt 根据需求有两种 reset 产生模式：

模式 1：只计数一轮，计数结束直接产生 reset 的信号。

模式 2：计数两轮，第一轮计数结束产生中断，第二轮计数结束产生 reset 信号。

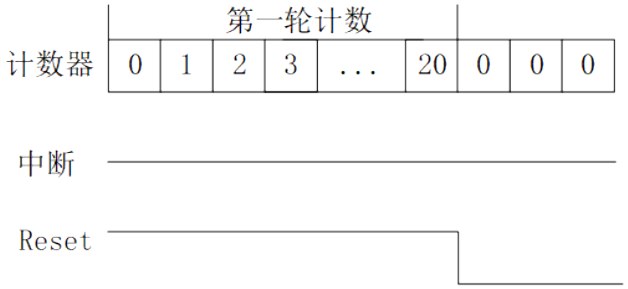


图 9-15: 模式 1 的中断以及 reset 信号产生与计数器的关系（假定超时值为 20，reset 低有效）

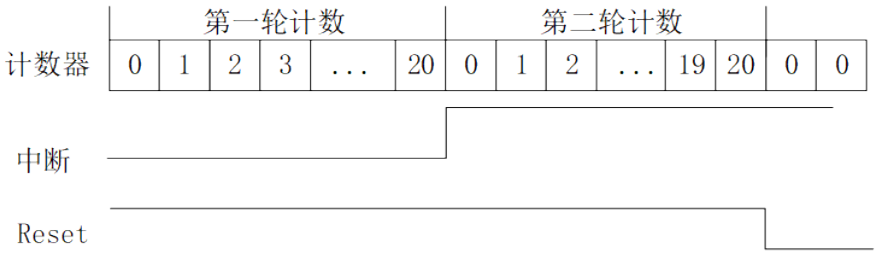


图 9-16: 模式 2 的中断以及 reset 信号产生与计数器的关系（假定超时值为 20，reset 低有效）

两种模式下的“喂狗”行为：

在模式 1 下，第一轮计数结束之前“喂狗”，则计数器从零开始重新计数；

在模式 2 下，第一轮计数结束之前“喂狗”，则计数器从零开始重新计数；如果第一轮计数器结束之前没有“喂狗”行为，则 wdt 进入第二轮计数，此时通过清除中断，或者“喂狗”的行为都可以让 wdt 重新进入第一轮开始计数。

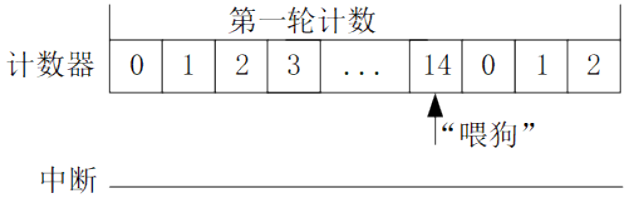


图 9-17: 模式 1“喂狗”行为对计数器的影响（假定超时值为 20）

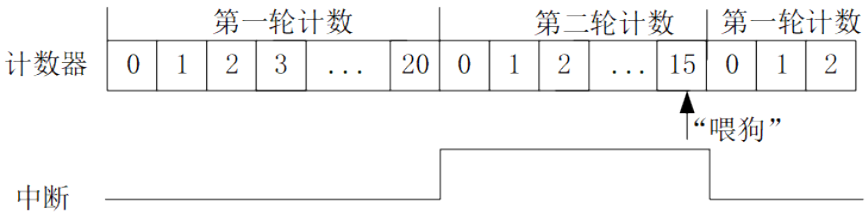


图 9-18: 模式 2 在第二轮计数时“喂狗“操作对计数器的影响，第一轮计数时的影响和模式 1 相同（假定超时值为 20）

两种模式下停止 wdt 的方式：

在模式 1 下，在计数结束之前配置寄存器 0x0C(counter_control)=0x34，wdt 则会停止；

在模式 2 下，在第一轮计数结束之前配置寄存器 0x0C(counter_control)=0x34，wdt 则会停止；如果在第二轮计数阶段则需要清除中断或者进行“喂狗”的操作让 wdt 回到第一轮计数才能进行配置寄存器 0x0C(counter_control)=0x34，让 wdt 停止。

清除中断的方法：

在模式 2 下，wdt 在第一轮计数完成之后会产生中断 0x14 WDT_SR 中 int_assert 为 1，此时可以通过配置 0x10 的 WDT_IDR 的 int_clr 来清除或者通过配置 0xc WDT_CCR 中 counter_control 为 0x76 即喂狗来清除。

9.5.2.1 WDT 寄存器配置流程

1. 根据需要选择 wdt 的工作模式。配置 0x08 中 response_mode 寄存器，配置 0x0 选择模式 1，配置 0x1 选择模式 2
2. 根据 wdt 触发 reset 时间配置 0x00 中 count_value_0 寄存器（两种模式下第一轮计数的超时值）以及 0x04 中的 count_value_1（模式 2 下第二轮计数器的超时值）
3. 根据需求配置 0x08 中 reset length 的长度
4. 配置 0x0c 中 counter_control 寄存器（=0x76）触发 wdt 开始工作
   1~3 的顺序没有要求，只要在 4 之前完成即可。

9.5.2.2 注意事项

1. wdt 提供了 write protect 写保护功能以防止 wdt 中的配置被意外改写，使用方法如下：
   配置 0x18 中 wrpt 寄存器为 0x58ab99fc，当 0x18 寄存器中 wrpt_st 为 1 说明写保护使能，此状态下 wdt 中的所有寄存器无法被改写但不影响读操作，如要取消写保护则配置 0x18 中 wrpt 寄存器为 0x51ff8621。

2. wdt 中 0x1c 的 sync_fg 寄存器为 1 表示 start，stop，irq clear，reset flag clear 的操作已经从 pclk 同步到 wdt clk 中即已经生效。
3. rst_fg 为 1 表示此 wdt 发生了 reset，此寄存器只有 iwdt 才有效。
4. 如果 0xc 中的 counter_control 写不进去，先 check 对应 sys rcc 里面的 wdt 时钟 enable 寄存器有没有配置为 1。

9.5.3 WDT 寄存器

表 9-6: WDT 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00			**WDT_CVR0**	WatchDog Counter Value 0
[31:24]			RSVD	
[23:0]	rw	24'hffffff	count_value_0	Count Value for 1st TimeOut
0x04			**WDT_CVR1**	WatchDog Counter Value 1
[31:24]			RSVD	
[23:0]	rw	24'hffffff	count_value_1	Count Value for 2nd TimeOut
0x08			**WDT_CR**	WatchDog Control Register
[31:5]			RSVD	
[4]	rw	1'b1	response_mode	0:reset only, 1:interrupt and reset
[3]			RSVD	
[2:0]	rw	3'b000	reset_length	reset pulse length in number of wdt clock cycles
0x0C			**WDT_CCR**	WatchDog Counter Control Register
[31:8]			RSVD	
[7:0]	rw	8'h0	counter_control	SinglePulse /Write 8'h76 to restart, write8'h34 to stop, else do nothing
0x10			**WDT_ICR**	WatchDog Interrupt Clear Register
[31:1]			RSVD	
[0]	w1c	1'b0	int_clr	SinglePulse /A pulse to clear interrupt
0x14			**WDT_SR**	WatchDog Status Register
[31:2]			RSVD	
[1]	r	1'b0	wdt_active	Watchdog runs when 1, else 0
[0]	r	1'b0	int_assert	Interrupt assert when 1
0x18			**WDT_WP**	WatchDog Write Protect Register
[31]	r	1'b0	wrpt_st	1 indicates write protect is active
[30:0]	w	31'h0	wrpt	write 0x58ab99fc generate write_protect, write 0x51ff8621 to release
0x1C			**WDT_FG**	WatchDog Flag Register
[31:4]			RSVD	
[3]	r	1'b0	sync_fg	1 indicates one transition from system clk to wdt clk has complicated
[2]	w1c	1'b0	sync_fg_clr	SinglePulse/A pulse to clear sync flag
[1]	r	1'b0	rst_fg	1 indicates wdt has already reset system
[0]	w1c	1'b0	rst_fg_clr	SinglePulse/A pulse to clear reset flag

10 图形

10.1 ePicasso™ 高性能 2.5D 图形引擎

ePicasso 位于 HPSYS。

在 2.5D 图像处理中，有许多常见的图像运算会耗费大量的 CPU 计算资源。ePicasso™ 则是专为 2.5D 图像运算设计的加速引擎，能够对 2.5D 图像运算中常见图层叠加、缩放、旋转等功能提供指数级的速度提升。除此以外，ePicasso™ 能够兼容各种常见的 RGB 图像格式，简化了系统中不同格式的图像格式转换。

10.1.1 图层叠加

ePicasso™ 最多支持四个前景图层，一个专用的掩膜图层，和一个单色背景图层叠加，输入和输出格式包括常用 RGB565、RGB888、ARGB8565、ARGB8888、L8、A8、A4。每个前景图层有独立的叠加模式和叠加区域，掩膜图层主要是提取图像中特定的形状。除此以外，每个图层还提供了单独的 filter 配置选项，可以使图层滤除某一特定的颜色，该功能可用于简单的图像捕获。

10.1.2 图形缩放

ePicasso™ 有一个图层称为功能图层，除了支持叠加的功能外，这个功能图层还能够实现图形的缩放。缩放最大比例可以到达 1024 倍，精度则可以达到 1/65536。在 X 和 Y 方向上，缩放的比例可以分别配置，以此适应各种不同的需求。

10.1.3 图形旋转

ePicasso™ 的功能图层除了可以支持缩放的功能以外，还能够支持图像的高精度旋转。用户可以自定义旋转角的 sin/cos 值，来满足任意角度的旋转需求。旋转和缩放的功能可以同时启用，一次性完成图像的两种操作，提高了图像处理的性能。

10.2 LCDC

LCDC 位于 HPSYS。

10.2.1 简介

LCDC 全称 LCD Controller，其主要功能是从内存空间读取图像数据，然后根据不同屏幕接口，将数据发送至对应的屏幕。LCDC 支持非常丰富的屏幕接口，包括：

- DPI/RGB 接口：用于高分辨率，不带 GRAM 的显示屏
- DBI/8080 接口：用于中低分辨率，带 GRAM 的显示屏
- SPI/DSPI/QSPI 接口：用于带 GRAM 的 IOT 小尺寸中低分辨率屏幕
- JDI Serial/Parallel 接口：用于 JDI 厂商专用反射型显示屏

除了丰富的接口，LCDC 对图像数据的格式支持也比较丰富，可以支持 RGB565，RGB888 以及 ARGB8888 等格式。在最基础的功能基础上，LCDC 也能够支持简单的图层混叠，可以进行最基础的图像处理加速。

10.2.2 架构介绍

如下图所示是 LCDC 的基本架构框图：

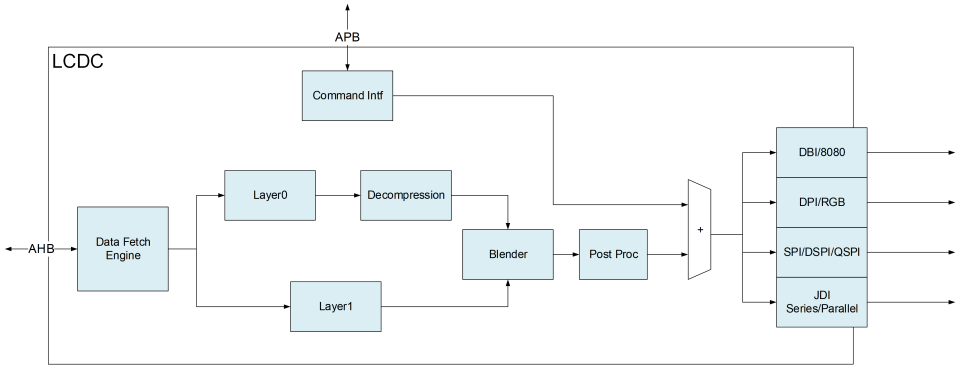


图 10-1: LCDC 架构图

图中有两条主要的数据通路。

1. 配置通路：上层通过 APB 总线发送屏幕配置指令，LCDC 接收到指令后，将对应的数据通过 Command Intf 模块发送到对应的屏幕接口上。该通路速率较低，主要用于屏幕初始化配置，以及基础功能验证。
2. 图像传输通路：LCDC 的 Data Fetch Engine 通过 AHB 总线，从内存空间读取图像数据，按配置发送到 Layer0/Layer1，其中 Layer0 有独立的解压缩模块，该模块会将收到的压缩数据解压缩为图像数据。当两个 layer 数据准备完成后，Blender 将图像数据混叠后送到对应的屏幕接口。该通路是 LCDC 向屏幕发送图像数据的主要通路。还有一点需要注意，Layer0 和 Layer1 均可以单独使能，即使两者均不使能，Blender 可以配置成向屏幕发送单色数据。

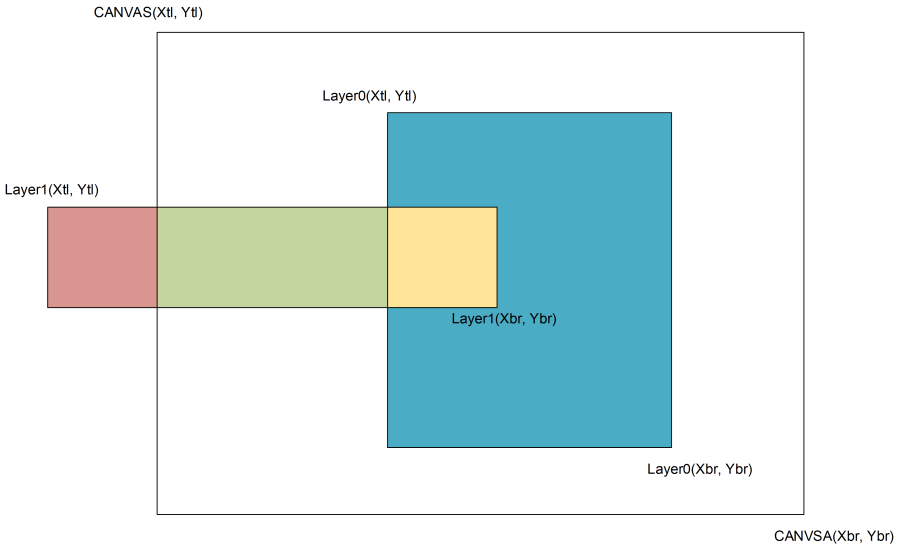
10.2.3 配置流程

LCDC 的配置主要分为两部分，第一部分是图层配置，针对的是两个 Layer 以及 Blender 的配置，第二部分是接口配置，针对的是不同接口对应的参数配置。

10.2.3.1 图层配置

图层配置包括 Layer0/Layer1 的配置和 Blender 的配置，用户可以配置 Layer0_CONFIG 和 Layer1_CONFIG 寄存器，对 Layer0 和 Layer1 进行使能，并配置其色彩格式和混叠系数。由于 Layer0 还支持压缩模式的图像，当 Layer0 的 Decompression 模块使能后，其原本的色彩格式配置将不再有效，解压后的色彩格式统一为 RGB888。

当图层数据被送入 Blender 后，Blender 会根据用户配置的图层坐标和画布坐标进行混叠操作，每一个图层有自己独立的矩形区域，画布也有其自己的矩形区域，Blender 只对重叠部分的图像进行计算。具体可以参考下图：



图中 CANVAS，Layer0，Layer1 各自有两组坐标代表各自的矩形区域，(Xtl, Ytl) 表示矩形左上角坐标，(Xbr, Ybr) 表示矩形右下角坐标。可以看到，Layer0 完全在 CANVAS 内部，所以其整个区域都会参与混叠计算，Layer1 由三部分组成，红色部分在 CANVAS 外，所以不会参与计算，黄色区域与 CANVAS 和 Layer0 都重叠，所以 Blender 会将这两个图层与 CANVAS 一同计算，最后绿色区域只与 CANVAS 重叠，所以会与 CANVAS 进行混叠计算。剩下白色的 CANVAS 区域因为没有与任何图层重叠，所以会直接输出 CANVAS 的背景色。

大部分场景下，LCDC 如果仅将图像帧缓存 (FrameBuffer) 输出到屏幕，那么只需要将图层的坐标与 CANVAS 坐标配置成一致即可。

Blender 输出之后还会经过 Post Processing 模块，该模块的 Dithering 在原有图像中加入一定的抖动，使图像在观感上更加平滑，除此以外该模块也支持对图像进行水平镜像。

10.2.3.2 接口配置

因为不同接口传输协议差别很大，所以对应的配置参数也不尽相同，以下根据不同接口列出了不同的配置参数。

DPI/RGB 接口：

DPI/RGB 是由 Pixel 时钟驱动的同步并行接口，其主要配置参数可以参考如下表格：

参数名	描述	配置
Freq(pclk)	Pixel 时钟速率	PCLK_DIV，Pixel 时钟分频比，源时钟为系统时钟
Hsync Width	Hsync 信号有效周期数	HSW，周期对应 Pixel 时钟
Vsync Height	Vsync 信号有效行数	VSH
Horizontal Active Width	行有效宽度	HAW，每一行的有效 Pixel 数
Vertical Active Height	有效行数	VAH，含有有效 Pixel 的行数
Horizontal Back Porch	HBP 参数	HBP，对应 DPI 接口的 HBP 参数
Vertical Back Porch	VBP 参数	VBP，对应 DPI 接口的 VBP 参数
Horizontal Front Porch	HFP 参数	HFP，对应 DPI 接口的 HFP 参数
Vertical Front Porch	VFP 参数	VFP，对应 DPI 接口的 VFP 参数

配置完这些参数后，用户还需要根据实际屏幕特点配置，配置 Hsync，Vsync，DE，Pclk 等信号的相位信息。默认情况下，这些信号都是高有效。

最后要注意，在配置完成 DPI 接口后，配置 DPI_EN 信号，即可使能 DPI 接口。使能后，只有配置 DPI_EN 为 0，才能停止 LCDC 的数据发送，否则 LCDC 会不断将当前配置地址的 Framebuffer 数据发送到屏幕端。

DBI/8080 接口:

DBI/8080 接口用于驱动带有 GRAM 的屏幕，根据 MIPI 协议，DBI 并行接口本身还分为 TypeA 和 TypeB 两类，两者信号上略有不同，但逻辑上可以互相转换。在选择 LCDC 接口时也可以选择对应的 TypeA 和 TypeB。

DBI 接口的主要参数配置参考下表：

参数名	描述	配置
PWH	WRX/RDX 信号 inactive 状态周期数	周期对应时钟为系统时钟
PWL	WRX/RDX 信号 active 状态周期数	周期对应时钟为系统时钟
TAH	WRX/RDX 信号 inactive 后到 CSX 信号 inactive 延迟周期数	周期对应时钟为系统时钟
TAS	CSX 信号 active 后到 WRX/RDX 信号 active 延迟周期数	周期对应时钟为系统时钟

以上参数是 DBI 接口配置的主要参数，其中 PWH 和 PWL 决定了 DBI 接口的速率，其两者之和为单笔数据传输的周期数。

另一点需要注意，DBI 接口所有信号默认为低有效，如果需要调整有效相位，可以通过配置对应信号的 POL 寄存器，实现相位的反转。

除了图像传输通路，DBI 接口也支持配置通路。在设置完成 DBI 接口后，用户可以先将要写的值配置到 LCD_WR 寄存器，通过 WR_TRIG 和 RD_TRIG 寄存器触发读写操作，在通过 LCD_RD 寄存器获得读取的值。

SPI/DSPI/QSPI 接口:

SPI，DSPI 和 QSPI 都属于 SPI 类型的屏幕接口，区别在于数据线的数量。SPI 通常只有单根的数据线，DSPI 有两根，QSPI 有四根。除了数据线数量区别，SPI 接口还会基于 D/C(Data/Command 选择) 信号传输方式分为 3-wire SPI 和 4-wire SPI。3-wire SPI 的 D/C 作为一个数据 bit，通过 SDO 进行传输，4-wire SPI 的 D/C 则有一根单独的线来标识，所以相对来说 3-wire SPI 比 4-wire SPI 有效带宽略微低一些。

SPI 接口的主要参数配置参考下表：

参数名	描述	配置
CLK_DIV	SPI 时钟分频比	源时钟为系统时钟
LINE	SPI 模式	不同模式包含 3-wire/4-wire 以及对应的单数据线，双数据线和死数据线模式
SPI_CS_AUTO_DIS	SPI CS 自动停止	在数据传输阶段，如果由于总线繁忙，LCDC 没有即使获取数据送往屏幕，则会自动控制 SPI 接口的 CS 信号，使其处于非使能状态
SPI_CLK_AUTO_DIS	SPI 时钟自动停止	在数据传输阶段，如果由于总线繁忙，LCDC 没有即使获取数据送往屏幕，则会自动停止 SPI 接口的时钟信号

除了以上这些主要参数，其他还有一些参数主要用于 SPI 接口的读操作，以及 SPI 信号的相位等，具体可以参考寄存器表内的描述。

与 DBI 接口一样，SPI 接口也支持配置通路。在选择了 SPI 接口后，与 DBI 一样，用户可以通过 WR_TRIG 和 RD_TRIG 寄存器触发读写操作。对于 SPI，用户还需要配置 WR_LEN 和 RD_LEN，这两个寄存器决定了 SPI 接口的配置通路单次读写数据的字节数。0 表示 1 个字节，最高 4 个字节。

JDI Serial/Parallel 接口:

JDI Serial 和 JDI Parallel 接口是 JDI 的反射屏专用的接口，JDI Serial 为串行接口，支持相对分辨率更小的屏幕，JDI Parallel 作为并行接口，可以支持分辨率更高的屏幕。JDI Serial 接口配置相对简单，配置参数如下：

参数名	描述	配置
CLK_DIV	JDI Serial 时钟分频比	源时钟为系统时钟
JDI_SER_FORMAT	JDI Serial 色彩格式	JDI Serial 可以支持 1bit，3bit，4bit 的色彩格式
JDI_WR_CMD	JDI 发送指令	JDI Serial 接口在发送实际数据前会先发送一段指令，这里可以对指令内容进行配置

以上就是 JDI Serial 接口的主要参数配置。JDI Serial 接口也支持配置通路，用户需要配置 JDI Serial 的 WR_LEN 寄存器，定义 JDI Serial 接口单次传输的 bit 位宽，在通过 WR_TRIG 发送数据。

JDI Parallel 接口可以适配相对更大分辨率的屏幕，色彩也会更丰富一些。其配置参数也更多，具体需要参照 JDI Parallel 接口协议，对相应参数进行配置。配置参数如下：

参数名	描述	配置
MAX_LINE	最大行数	\
MAX_COL	最大列数	\
ST_LINE	起始行数	第一行有效数据行数
END_LINE	结束行数	最后一行有效数据行数
ST_COL	起始列数	第一列有效数据列数
END_COL	结束列数	最后一列有效数据列数
HCK_WIDTH	HCK 信号宽度	基于系统时钟周期数
HST_WIDTH	HST 信号宽度	基于系统时钟周期数
VCK_WIDTH	VCK 信号宽度	基于系统时钟周期数
VST_WIDTH	VST 信号宽度	基于系统时钟周期数
VCK_DLY	VST 到 VCK 信号的延迟	基于系统时钟周期数
HST_DLY	VCK 到 HST 信号的延迟	基于系统时钟周期数
HCK_DLY	HST 到 HCK 信号的延迟	基于系统时钟周期数
ENB_ST_COL	ENB 信号起始列数	ENB 信号有效的第一列列数
ENB_END_COL	ENB 信号结束列数	ENB 信号有效的最后一列列数
ENB_ST_LINE	ENB 信号起始行数	ENB 信号有效的第一行行数
ENB_END_LINE	ENB 信号结束列数	ENB 信号有效的最后一行行数
DP_MODE	DP 模式	支持大小双像素模式

JDI Parallel 接口配置参数较多，需要结合 JDI Parallel 接口文档才能比较准确的进行参数的配置。JDI Parallel 接口同 DPI 接口类似，使能后会循环不停从 FrameBuffer 地址读取数据送到屏幕上。只有当使能关闭后，JDI Parallel 接口才会在当前帧数据发送结束后停止。

10.2.4 LCDC 寄存器

表 10-1: LCDC 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00			**COMMAND**	
[31:2]			RSVD	
[1]	rw	1'h0	reset	1: reset the whole graphics 0: release the reset
[0]	w1t	1'h0	start	write 1 to trigger the lcd interface block
0x04			**STATUS**	
[31:3]			RSVD	
[2]	r	1'h0	JDI_PAR_RUN	JDI parallel interface is running
[1]	r	1'h0	DPI_RUN	DPI interface is running
[0]	r	1'h0	LCD_BUSY	LCS controll busy flag
0x08			**IRQ**	
[31:23]			RSVD	
[22]	rw1c	1'h0	LINE_DONE_RAW_STAT	raw_status of line process done interrupt
[21]	rw1c	1'h0	JDI_PAR_UDR_RAW_STAT	raw_status of jdi parallel interface under run interrupt
[20]	rw1c	1'h0	JDI_PARL_INTR_RAW_STAT	raw_status of jdi parallel interface line interrupt
[19]	rw1c	1'h0	DPI_UDR_RAW_STAT	raw status of dpi under run interrupt

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表 10-1: LCDC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[18]	rw1c	1'h0	DPIL_INTR_RAW_STAT	raw status of dpi line interrupt
[17]	rw1c	1'h0	ICB_OF_RAW_STAT	raw status of icb overflow interrupt
[16]	rw1c	1'h0	EOF_RAW_STAT	raw status of end of frame interrupt
[15:7]			RSVD	
[6]	rw1c	1'h0	LINE_DONE_STAT	line process done interrupt, masked by mask register
[5]	rw1c	1'h0	JDI_PAR_UDR_STAT	jdi parallel interface under run interrupt, masked by mask register
[4]	rw1c	1'h0	JDI_PARL_INTR_STAT	jdi parallel interface line interrupt, masked by mask register
[3]	rw1c	1'h0	DPI_UDR_STAT	dpi under run interrupt, masked by mask register
[2]	rw1c	1'h0	DPIL_INTR_STAT	dpi line interrupt, masked by mask register
[1]	rw1c	1'h0	ICB_OF_STAT	icb overflow interrupt, masked by mask register
[0]	rw1c	1'h0	EOF_STAT	end of frame interrupt, masked by mask register
0x0C			**SETTING**	
[31:27]			RSVD	
[26:16]	rw	11'h1ff	LINE_DONE_NUM	line number of line process done interrupt
[15:9]			RSVD	
[8]	rw	1'h1	AUTO_GATE_EN	auto clock gating enable
[7]			RSVD	
[6]	rw	1'h0	LINE_DONE_MASK	line process done interrupt, 0: mask the interrupt
[5]	rw	1'h0	JDI_PAR_UDR_MASK	jdi parallel interface under run interrupt mask, 0: mask the interrupt
[4]	rw	1'h0	JDI_PARL_INTR_MASK	jdi parallel interface line interrupt, 0: mask the interrupt
[3]	rw	1'h0	DPI_UDR_MASK	dpi under run interrupt mask, 0: mask the interrupt
[2]	rw	1'h0	DPIL_INTR_MASK	dpi line interrupt, 0: mask the interrupt
[1]	rw	1'h0	ICB_OF_MASK	icb overflow interrupt mask, 0: mask the interrupt
[0]	rw	1'h0	EOF_MASK	end of frame interrupt mask, 0: mask the interrupt
0x10			**CANVAS_TL_POS**	
[31:27]			RSVD	
[26:16]	rw	11'h0	Y0	
[15:11]			RSVD	
[10:0]	rw	11'h0	X0	
0x14			**CANVAS_BR_POS**	
[31:27]			RSVD	
[26:16]	rw	11'h0	Y1	
[15:11]			RSVD	
[10:0]	rw	11'h0	X1	
0x18			**CANVAS_BG**	
[31:28]			RSVD	
[27]	rw	1'h0	H_MIRROR	set 1 to do horizontal mirror for output image
[26]	rw	1'h0	LB_BYPASS	line buffer bypass. Set 1 to bypass line buffer.
[25]	rw	1'h0	ALL_BLENDING_BYPASS	if this bit is set, lcdc is in pure dma mode. No blending operation.
[24]	rw	1'h0	BG_BLENDING_BYPASS	if this bit is set, the layer is not blending with background. The alpha value will be reserved to output.
[23:16]	rw	8'h0	RED	Red color
[15:8]	rw	8'h0	GREEN	green color
[7:0]	rw	8'h0	BLUE	blue color
0x1C			**LAYER0_CONFIG**	
[31]			RSVD	
[30]	rw	1'h0	V_MIRROR	set 1 to do vertical mirror for the layer

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表 10-1: LCDC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[29]	rw	1'h0	ALPHA_BLEND	set 1 to enable alpha blending mode. Use layer alpha as blending factor for image with Alpha. Alpha_out = Layer_alpha * Image_alpha
[28]	rw	1'h0	ACTIVE	layer active flag
[27]	rw	1'h0	LINE_FETCH_MODE	line fetch mode 0: address skip every single line 1: address skip every two line
[26]	rw	1'h0	PREFETCH_EN	preload 64 bytes extra data when reading pixel from memory
[25:13]	rw	13'h0	WIDTH	source image width(including padding), unit is bytes
[12]	rw	1'h0	FILTER_EN	layer color filter enable
[11:4]	rw	8'h0	ALPHA	layer alpha value
[3]	rw	1'h0	ALPHA_SEL	alpha selection 1'b0: select alpha according to image format 1'b1: select layer alpha
[2:0]	rw	3'h0	FORMAT	overlay layer input format 3'h0: RGB565 3'h1: RGB888 3'h2: ARGB8888 3'h3: ARGB8565 3'h4: RGB332 3'h5: A8 3'h6: L8 others: reserved
0x20			**LAYER0_TL_POS**	
[31:27]			RSVD	
[26:16]	rw	11'h0	Y0	Coordingate Y-value
[15:11]			RSVD	
[10:0]	rw	11'h0	X0	Coordinate X-value
0x24			**LAYER0_BR_POS**	
[31:27]			RSVD	
[26:16]	rw	11'h0	Y1	Coordingate Y-value
[15:11]			RSVD	
[10:0]	rw	11'h0	X1	Coordinate X-value
0x28			**LAYER0_FILTER**	
[31:24]	rw	8'h0	FILTER_MASK	layer color filter mask
[23:16]	rw	8'h0	FILTER_R	filter r color
[15:8]	rw	8'h0	FILTER_G	filter g color
[7:0]	rw	8'h0	FILTER_B	filter b color
0x2C			**LAYER0_SRC**	
[31:0]	rw	32'h0	ADDR	source image RGB data address[31:0]. For RGB565 format, address should be aligned to halfword. For ARGB8888 format, address should be aligned to word.
0x30			**LAYER0_FILL**	
[31:26]			RSVD	
[25]	rw	1'h0	ENDIAN	input 565 data format endian 0: R[4:0], G[5:3], G[2:0], B[4:0] 1: G[2:0], R[4:0], B[4:0], G[5:3]
[24]	rw	1'h0	BG_MODE	not used
[23:16]	rw	8'h0	BG_R	background r color

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表 10-1: LCDC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[15:8]	rw	8'h0	BG_G	background g color
[7:0]	rw	8'h0	BG_B	background b color
0x34			**LAYER0_DECOMP**	
[31:24]			RSVD	
[23:13]	rw	11'h0	col_size	number of colums in a line of original image, max column size is 1024
[12:1]	rw	12'h0	target_words	size of a single channel data before decompression. Unit is half word. Each line has 3 channels. So for each line, the compressed data size is target_words * 3 * 2 bytes.
[0]	rw	1'h0	enable	decompression enable
0x38			**LAYER0_DECOMP_CFG0**	
[31:20]	rw	12'h10	cfg0_reserved	
[19:16]	rw	4'h5	lossless_qidx2	condition to decrease qidx
[15:12]	rw	4'h5	lossless_qidx1	up level for adjusted qidx value for low quality block
[11:8]	rw	4'h9	use_lossless_qidx	condition to increase qidx
[7:4]	rw	4'h8	extra_threshold	the threshold to distinguish high/low quality block
[3:0]	rw	4'h2	extra_high	extra bit for high quality bit
0x3C			**LAYER0_DECOMP_CFG1**	
[31:28]	rw	4'h8	extra_low	extra bit for low quality block
[27:24]	rw	4'h0	block_min_qidx	minimum qidx for block mode
[23:20]	rw	4'h0	line_min_qidx	minimum qidx for line mode
[19:16]	rw	4'h2	failover_bits_b	failover compression mode target bits(Blue)
[15:12]	rw	4'h3	failover_bits_g	failover compression mode target bits(Green)
[11:8]	rw	4'h3	failover_bits_r	failover compression mode target bits(Red)
[7:2]	rw	6'h1	cfg1_reserved	
[1]	rw	1'b1	dither	dithering function 0: off 1: on
[0]	rw	1'b1	block_width	block_size in pixel unit. 0: 16 pixels 1: 32 pixels Small block size will cause more blocks and more bits to store block information.
0x40			**LAYER0_DECOMP_STAT**	
[31:7]			RSVD	
[6:0]	r	7'h0	buf_max_depth	buf max usage
0x60			**LAYER1_CONFIG**	
[31]			RSVD	
[30]	rw	1'h0	V_MIRROR	set 1 to do vertical mirror for the layer
[29]	rw	1'h0	ALPHA_BLEND	set 1 to enable alpha blending mode. Use layer alpha as blending factor for image with Alpha. Alpha_out = Layer_alpha * Image_alpha
[28]	rw	1'h0	ACTIVE	layer active flag
[27]	rw	1'h0	LINE_FETCH_MODE	line fetch mode 0: address skip every single line 1: address skip every two line
[26]	rw	1'h0	PREFETCH_EN	preload 64 bytes extra data when reading pixel from memory
[25:13]	rw	13'h0	WIDTH	source image width(including padding), unit is bytes
[12]	rw	1'h0	FILTER_EN	layer color filter enable
[11:4]	rw	8'h0	ALPHA	layer alpha value

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表 10-1: LCDC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[3]	rw	1'h0	ALPHA_SEL	alpha selection 1'b0: select alpha according to image format 1'b1: select layer alpha
[2:0]	rw	3'h0	FORMAT	overlay layer input format 3'h0: RGB565 3'h1: RGB888 3'h2: ARGB8888 3'h3: ARGB8565 3'h4: RGB332 3'h5: A8 3'h6: L8 others: reserved
0x64			**LAYER1_TL_POS**	
[31:27]			RSVD	
[26:16]	rw	11'h0	Y0	Coordingate Y-value
[15:11]			RSVD	
[10:0]	rw	11'h0	X0	Coordinate X-value
0x68			**LAYER1_BR_POS**	
[31:27]			RSVD	
[26:16]	rw	11'h0	Y1	Coordingate Y-value
[15:11]			RSVD	
[10:0]	rw	11'h0	X1	Coordinate X-value
0x6C			**LAYER1_FILTER**	
[31:24]	rw	8'h0	FILTER_MASK	layer color filter mask
[23:16]	rw	8'h0	FILTER_R	filter r color
[15:8]	rw	8'h0	FILTER_G	filter g color
[7:0]	rw	8'h0	FILTER_B	filter b color
0x70			**LAYER1_SRC**	
[31:0]	rw	32'h0	ADDR	source image RGB data address[31:0]. For RGB565 format, address should be aligned to halfword. For ARGB8888 format, address should be aligned to word.
0x74			**LAYER1_FILL**	
[31:26]			RSVD	
[25]	rw	1'h0	ENDIAN	input 565 data format endian 0: R[4:0], G[5:3], G[2:0], B[4:0] 1: G[2:0], R[4:0], B[4:0], G[5:3]
[24]	rw	1'h0	BG_MODE	not used
[23:16]	rw	8'h0	BG_R	background r color
[15:8]	rw	8'h0	BG_G	background g color
[7:0]	rw	8'h0	BG_B	background b color
0x78			**DITHER_CONF**	
[31:13]			RSVD	
[12]	w1t	1'h0	lfsr_load	load lfsr init value
[11:10]	rw	2'h0	lfsr_load_sel	select lfsr 0: none 1: red 2: green 3: blue
[9:7]	rw	3'h0	w_r	red dither width

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表 10-1: LCDC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[6:4]	rw	3'h0	w_g	green dither width
[3:1]	rw	3'h0	w_b	blue dither width
[0]	rw	1'h0	en	dither enable
0x7C			**DITHER_LFSR**	
[31:0]	rw	32'h0	init_val	lfsr init load value
0x80			**LCD_CONF**	
[31:19]			RSVD	
[18]	rw	1'h0	ENDIAN	LCD 565 data format endian, this bit would affect SPI, DPI, DBI and AHB interface 565 format 0: R[4:0], G[5:3], G[2:0], B[4:0] 1: G[2:0], R[4:0], B[4:0], G[5:3]
[17]	rw	1'h0	DIRECT_INTF_EN	when the target LCD is AHB LCD, this bit enable the direct interface to DSI module. Direct interface has higher bandwidth and speed than AHB interface.
[16:15]	rw	2'h0	JDI_SER_FORMAT	JDI serial format 2'b00: 3-bit mode 2'b01: 4-bit mode 2'b10: 1-bit mode 2'b11: reserved
[14:12]	rw	3'h0	DPI_LCD_FORMAT	DPI LCD format 3'b000: 16-bit conf1 3'b001: 16-bit conf2 3'b010: 16-bit conf3 3'b011: 18-bit conf1 3'b100: 18-bit conf2 3'b101: 24-bit others: Reserved
[11:10]	rw	2'h0	SPI_LCD_FORMAT	SPI LCD format 2'b00: 8-bit RGB 3:3:2 2'b01: 16-bit RGB 5:6:5 2'b10: 24-bit RGB 8:8:8 2'b11: Reserved
[9:8]	rw	2'h0	AHB_FORMAT	AHB LCD/RAM output format: 0: RGB565 1: RGB888 2: ARGB8888 3: RGB332
[7:5]	rw	3'h0	LCD_FORMAT	LCD output format: 3'b000: 8-bit RGB 3:3:2 3'b001: 16-bit RGB 5:6:5 over 8-bit bus, 2 cycles/pixel 3'b010: 12-bit RGB 4:4:4 3'b011: 16-bit RGB 5:6:5 3'b100: 18-bit RGB 6:6:6 3'b101: 24-bit RGB 8:8:8 3'b110: 24-bit RGB 8:8:8 over 16-bit bus, 1.5 cycles/pixel 3'b111: 24-bit RGB 8:8:8 over 8-bit bus, 3cycles/pixel others: Reserved

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表 10-1: LCDC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[4:2]	rw	3'h0	LCD_INTF_SEL	3'b000: 8080 DBI Type B 3'b001: SPI interface 3'b010: DBI to DSI interface 3'b011: DPI interface 3'b100: JDI serial interface 3'b101: JDI parallel interface 3'b110: 8080 DBI Type A 3'b111: DPI to DSI interface
[1:0]	rw	2'h0	TARGET_LCD	The Data can be sent to four destinations: 2'b00: LCD panel 0 2'b01: LCD panel 1 2'b10: AHB LCD 2'b11: AHB RAM
0x84			**LCD_IF_CONF**	
[31:26]			RSVD	
[25]	rw	1'h0	CTRL_DLY_SET	if this bit is set to 1, LCD control output will be delayed for 1 lcdc clock cycle
[24]	rw	1'h0	DO_DLY_SET	if this bit is set to 1, LCD data output will be delayed for 1 lcdc clock cycle
[23]	rw	1'h0	LCD_RSTB	LCD RSTB pin, direct to output
[22]	rw	1'h0	RD_POL	LCD RD pin polarity. RD is 0 for write operation, 1 for idle if polarity bit is set as 0. RD bit definition is opposite if polarity bit is set as 1.
[21]	rw	1'h0	WR_POL	LCD WR pin polarity. WR is 0 for write operation, 1 for idle if polarity bit is set as 0. WR bit definition is opposite if polarity bit is set as 1.
[20]	rw	1'h0	RS_POL	LCD RS pin polarity. RS is 1 for data access, 0 for command access if polarity bit is set as 0. RS bit definition is opposite if polarity bit is set as 1.
[19]	rw	1'h0	CS1_POL	LCD0 CS pin polarity. CS is 0 for LCD chip select if polarity bit is set as 0. CS bit definition is opposite if polarity bit is set as 1.
[18]	rw	1'h0	CS0_POL	LCD1 CS pin polarity. CS is 0 for LCD chip select if polarity bit is set as 0. CS bit definition is opposite if polarity bit is set as 1.
[17:12]	rw	6'h0	PWH	inactive cycles of LCD_WR/LCD_RD for consecutive write/read operation
[11:6]	rw	6'h0	PWL	active cycles of LCD_WR/LCD_RD
[5:3]	rw	3'h0	TAH	hold cycles, delay from LCD_WR/LCD_RD inactive to LCD_CS inactive
[2:0]	rw	3'h0	TAS	setup cycles, delay from LCD_CS active to LCD_WR/LCD_RD active
0x88			**LCD_MEM**	
[31:0]	rw	32'h0	ADDR	address for AHB LCD/AHB RAM
0x8C			**LCD_O_WIDTH**	
[31:16]			RSVD	
[15:0]	rw	16'h0	OFFSET	AHB RAM address offset for each line
0x90			**LCD_SINGLE**	
[31:4]			RSVD	
[3]	r	1'h0	LCD_BUSY	LCD/SPI LCD interface is busy for single access
[2]	w1t	1'h0	RD_TRIG	Single read operation trigger
[1]	w1t	1'h0	WR_TRIG	Single write operation trigger
[0]	rw	1'h0	TYPE	LCD access type, this bit could affect all LCD interface including SPI, parellel and AHB 1'b0: command 1'b1: data
0x94			**LCD_WR**	
[31:0]	rw	32'h0	DATA	LCD write data
0x98			**LCD_RD**	

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表 10-1: LCDC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:0]	r	32'h0	DATA	LCD read data
0x9C			**SPI_IF_CONF**	
[31]			RSVD	
[30]	rw	1'h0	SPI_CLK_INIT	SPI CLK idle state value 1'h0: high 1'h1: low
[29]	rw	1'h0	SPI_CLK_POL	SPI CLK polarity 1'h0: normal 1'h1: inverted
[28]	rw	1'h0	SPI_CS_POL	SPI CS polarity 0: low active 1: high active
[27]	rw	1'h1	SPI_CS_AUTO_DIS	1: SPI CS is automatically disabled after data transaction 0: SPI CS is not disabled after data transaction
[26]	rw	1'h0	SPI_CS_NO_IDLE	1: SPI CS is always active during data transaction 0: SPI CS is IDLE in wait state during data transaction
[25]	rw	1'h0	SPI_CLK_AUTO_DIS	1: SPI clock auto disable in wait state during data transaction 0: SPI clock is always on in wait state during data transaction
[24]	rw	1'h0	SPI_RD_MODE	SPI read mode: 1'b0: normal read. Send write request before read. 1'b1: direct read. Read data without write request.
[23:22]	rw	2'h0	WR_LEN	SPI write data length(single access)
[21:20]	rw	2'h0	RD_LEN	SPI read data length(single access)
[19:17]	rw	3'h0	LINE	SPI line mode 0: 4-line 1: 4-line with 2 data line(support RGB565 and RGB888) 2: 4-line with 4 data line(support RGB565 and RGB888) 3: reserved 4: 3-line 5: 3-line with 2 data line(support RGB565 and RGB888) 6: 3-line with 4 data line(support RGB565 and RGB888) 7: reserved
[16:14]	rw	3'h0	DUMMY_CYCLE	SPI transaction dummy cycle
[13:6]	rw	8'ha	CLK_DIV	SPI clock divider
[5:0]	rw	6'h0	WAIT_CYCLE	SPI line wait cycle, wait cycle is after each line and is according to SPI clock. 0 refers to no wait cycle.
0xA0			**TE_CONF**	
[31:21]			RSVD	
[20]	rw	1'h0	FMARK_SOURCE	TE signal source 1: use TE signal from DSI 0: use TE signal from external pin
[19]	rw	1'h0	FMARK_MODE	TE signal trigger mode 1: edge trigger 0: pulse trigger
[18:3]	rw	16'h0	VSYNC_DET_CNT	vsync signal detect counter, used for mode 1 to detect vsync signal
[2]	rw	1'h0	MODE	0: vsync only TE mode 1: vsync+hsync TE mode
[1]	rw	1'h0	FMARK_POL	TE signal polarity
[0]	rw	1'h0	ENABLE	TE enable

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表 10-1: LCDC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
0xA4			**TE_CONF2**	
[31:0]	rw	32'h0	DLY_CNT	TE delay counter
0xA8			**DPI_IF_CONF1**	
[31:27]			RSVD	
[26:16]	rw	11'h0	HSW	dpi hsync width
[15:11]			RSVD	
[10:0]	rw	11'h0	VSH	dpi vsync height
0xAC			**DPI_IF_CONF2**	
[31:27]			RSVD	
[26:16]	rw	11'h0	HBP	horizontal back porch
[15:11]			RSVD	
[10:0]	rw	11'h0	VBP	vertical back porch
0xB0			**DPI_IF_CONF3**	
[31:27]			RSVD	
[26:16]	rw	11'h0	HFP	horizontal front porch
[15:11]			RSVD	
[10:0]	rw	11'h0	VFP	vertical front porch
0xB4			**DPI_IF_CONF4**	
[31:27]			RSVD	
[26:16]	rw	11'h0	HAW	horizontal active width
[15:11]			RSVD	
[10:0]	rw	11'h0	VAH	vertical active height
0xB8			**DPI_IF_CONF5**	
[31:24]			RSVD	
[23]	rw	1'h0	clk_force_on	1: force DPI clock on 0: DPI clock is controlled by hardware
[22:12]	rw	11'h7ff	INT_LINE_NUM	DPI interrupt line number
[11]	rw	1'h0	HSPOL	hsync polarity
[10]	rw	1'h0	VSPOL	vsync polarity
[9]	rw	1'h0	DEPOL	de polarity
[8]	rw	1'h0	PCLKPOL	pixel clock polarity
[7:0]	rw	8'h1	PCLK_DIV	pixel clock divider
0xBC			**DPI_CTRL**	
[31:4]			RSVD	
[3]	rw	1'h0	DPI_UC	dpi update config
[2]	rw	1'h0	DPI_SD	dpi shutdown
[1]	rw	1'h0	DPI_CM	dpi color mode
[0]	rw	1'h0	DPI_EN	dpi interface enable
0xC0			**DPI_STAT**	
[31:16]	r	16'h1	VPOS	dpi vertical position
[15:14]			RSVD	

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表 10-1: LCDC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[13:11]	r	3'h0	HSTAT	horizontal status 0: idle 1: prep 2: hsync 3: hbp 4: hact 5: hfp 6: wait
[10:0]	r	11'h1	HPOS	dpi horizontal position
0xC4			**JDI_SER_CONF1**	
[31:16]			RSVD	
[15:8]	rw	8'h2	CLK_DIV	jdi serial clock divider
[7:5]			RSVD	
[4:0]	rw	5'd1	WR_LEN	jdi single write bit length
0xC8			**JDI_SER_CONF2**	
[31:16]	rw	16'h0	INIT_LINE_CNT	jdi serial init line counter
[15:0]	rw	16'h0	WR_CMD	jdi serial data transfer write command
0xCC			**JDI_SER_CTRL**	
[31:2]			RSVD	
[1]	rw	1'h0	EXTCOMIN	jdi serial interface extcomin control
[0]	rw	1'h0	DISP	jdi serial interface disp control
0xD0			**JDI_PAR_CONF1**	
[31:16]	rw	16'h0	MAX_LINE	jdi parallel interface max line, line number start from 0
[15:0]	rw	16'h0	MAX_COL	jdi parallel interface max column, column number start from 0
0xD4			**JDI_PAR_CONF2**	
[31:16]	rw	16'h0	ST_LINE	jdi parallel interface start line, line number start from 0
[15:0]	rw	16'h0	END_LINE	jdi parallel interface end line, line number start from 0
0xD8			**JDI_PAR_CONF3**	
[31:16]	rw	16'h0	ST_COL	jdi parallel interface start column, column number start from 0
[15:0]	rw	16'h0	END_COL	jdi parallel interface end column, column number start from 0
0xDC			**JDI_PAR_CONF4**	
[31:16]	rw	16'h0	HCK_WIDTH	jdi parallel interface HCK width, HSK width = lcd_ck_cycle * HCK_WIDTH
[15:0]	rw	16'h0	HST_WIDTH	jdi parallel interface HST width, HST width = lcd_ck_cycle * HST_WIDTH
0xE0			**JDI_PAR_CONF5**	
[31:16]	rw	16'h0	VCK_WIDTH	jdi parallel interface VCK width, VCK width = lcd_ck_cycle * VCK_WIDTH
[15:0]	rw	16'h0	VST_WIDTH	jdi parallel interface VST width, VST width = lcd_ck_cycle * VST_WIDTH
0xE4			**JDI_PAR_CONF6**	
[31:16]	rw	16'h0	VCK_DLY	jdi parallel interface VST to VCK delay, VST2VCK delay = lcd_ck_cycle * VCK_DLY
[15:0]	rw	16'h0	HST_DLY	jdi parallel interface VCK to HST delay, VCK2HST delay = lcd_ck_cycle * HST_DLY
0xE8			**JDI_PAR_CONF7**	
[31:17]			RSVD	
[16]	rw	1'h0	DP_MODE	double pixel mode. Some jdi parallel screens use large pixel+small pixel structure. Set this bit to 1 to support this structure.
[15:0]	rw	16'h0	HCK_DLY	jdi parallel interface HST to HCK delay
0xEC			**JDI_PAR_CTRL**	
[31:16]	rw	16'hffff	INT_LINE_NUM	jdi parallel interface interrupt line number, line number start from 0.

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表 10-1: LCDC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[15:10]			RSVD	
[9]	rw	1'h0	VSTPOL	jdi parallel vst polarity
[8]	rw	1'h0	VCKPOL	jdi parallel vck polarity
[7]	rw	1'h0	HSTPOL	jdi parallel hst polarity
[6]	rw	1'h0	HCKPOL	jdi parallel hck polarity
[5]	rw	1'h0	ENBPOL	jdi parallel enb polarity
[4]	rw	1'h0	XRST	jdi parallel interface XRST
[3:1]			RSVD	
[0]	rw	1'h0	ENABLE	jdi parallel interface enable
0xF0			**JDI_PAR_STAT**	
[31:16]	r	16'h0	VPOS	jdi parallel vertical position
[15:0]	r	16'h0	HPOS	jdi parallel horizontal position
0xF4			**JDI_PAR_EX_CTRL**	
[31]	r	1'h0	VCOM	VCOM value
[30]	r	1'h0	FRP	FRP value
[29]	r	1'h0	XFRP	XFRP value
[28]	rw	1'h0	CNT_EN	VCOM/FRP/XFRP counter enable
[27:24]			RSVD	
[23:0]	rw	24'h0	MAX_CNT	VCOM/FRP/XFRP max counter
0xF8			**JDI_PAR_CONF8**	
[31:16]	rw	16'h0	ENB_ST_COL	jdi parallel interface enb start column, column number start from 0
[15:0]	rw	16'h0	ENB_END_COL	jdi parallel interface enb end column, column number start from 0
0xFC			**JDI_PAR_CONF9**	
[31:16]	rw	16'h0	ENB_ST_LINE	jdi parallel interface enb start line, line number start from 0
[15:0]	rw	16'h0	ENB_END_LINE	jdi parallel interface enb end line, line number start from 0
0x100			**JDI_PAR_CONF10**	
[31:16]	rw	16'h0	HC_ST_LINE	jdi parallel interface horizontal control start line, line number start from 0
[15:0]	rw	16'h0	HC_END_LINE	jdi parallel interface horizontal control end line, line number start from 0
0x110			**CANVAS_STAT0**	
[31:27]			RSVD	
[26:16]	r	11'h0	y_cor	canvas y cordinate
[15:11]			RSVD	
[10:0]	r	11'h0	x_cor	canvas x cordinate
0x114			**CANVAS_STAT1**	
[31:12]			RSVD	
[11:9]	r	3'h0	fetch_stat	fetch status
[8:6]	r	3'h0	prec_stat	prec status
[5:3]	r	3'h0	postc_stat	postc_status
[2:0]	r	3'h0	fifo_cnt	pre calc fifo count
0x118			**OL0_STAT**	
[31:24]			RSVD	
[23:22]	r	2'h0	sc_lb0	
[21:20]	r	2'h0	sc_lb1	
[19:16]	r	4'h0	sc_fe	
[15:13]	r	3'h0	sc_be	
[12:11]	r	2'h0	sc_out	
[10:8]	r	3'h0	pf_pr	
[7:6]	r	2'h0	pf_df	

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表 10-1: LCDC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[5:4]	r	2'h0	data_conv	
[3:2]	r	2'h0	prefetch_read	
[1]	r	1'h0	prefetch_out	
[0]	r	1'h0	done_req	
0x11C			**OL1_STAT**	
[31:11]			RSVD	
[10:8]	r	3'h0	pf_pr	
[7:6]	r	2'h0	pf_df	
[5:4]	r	2'h0	data_conv	
[3:2]	r	2'h0	prefetch_read	
[1]	r	1'h0	prefetch_out	
[0]	r	1'h0	done_req	
0x120			**MEM_IF_STAT**	
[31:10]			RSVD	
[9:7]	r	3'h0	arb_main	
[6:4]	r	3'h0	arb_read_port	
[3:0]	r	4'h0	ahb	
0x124			**PERF_CNT**	
[31:0]	rw	32'h0	VAL	lcdc performance counter

10.3 eZip™ 无损压缩解码器

eZip 位于 HPSYS。

eZip™ 解码器是基于自有算法的实时无损解压缩模块，压缩率与 Zip 格式相当。它可以用于将通用数据解码后保存，以此加快数据的实时加载能力。如果数据是从芯片外部传输，压缩后的传输有助于缩短传输时间，减少传输功耗。

此外，eZip™ 还支持专有格式的图片压缩，压缩率与 PNG 格式相当，并支持独立 DMA 操作或与 ePicasso™ 联动读取。当独立操作时，eZip™ 可通过 DMA 机制，可以灵活地将存储在 Flash 或 RAM 的压缩图片解压缩并搬运至目标缓存中。在联动模式下，ePicasso™ 通过 eZip™ 模块，实时从存储中读取图片并实时解压缩，然后按照一般的图形流程进行所需要的 2.5D 计算，从而省去了暂存解压缩图片的缓存。

通过以上机制，eZip™ 可以有效地降低图像素材对存储容量的需求，在有限的存储中最大化素材的丰富度，减小对片外存储的带宽要求，从而提高大大系统的整体运行效率。

eZip™ 模块是将 eZip™ 压缩图片进行解码输出的模块。该模块通过 AHB 总线读入压缩数据，解码后的图像数据可配置通过 AHB 总线输出或直接送给 epic 模块进行后续处理。

该模块具有以下特点：

- 通过 AHB 总线输入\输出的数据地址可配
- 输出图片数据可直接送给 epic 模块
- 可输出一个指定区域的图片数据
- 支持解码参数 cache 功能，cache 命中的情况下可缩短解码时间

11 音频

11.1 PDM

芯片共有 2 个 PDM，均位于 HPSYS，输入输出连接至 IO(PA)，可向 DMAC1 发送请求。

11.1.1 简介

PDM (Pulse Density Modulation) 脉冲密度调制接口主要是用于将 PDM 麦克风采集到的 PDM 音频信号转化为 PCM（Pulse Code Modulation）脉冲编码调制信号以供后续的音频处理。

主要功能：

- 同时支持左右两路立体声信号，也可以单独采集单声道信号
- 可提供的 PDM 麦克风时钟速率：3.072MHz、1.536MHz、0.768MHz、1.024MHz、2.4MHz、1.6MHz、0.8MHz 等
- 支持 PCM 数据的速率：48kHz、32kHz、24kHz、16kHz、12kHz、8kHz 等
- 支持 32bit、24bit、16bit、8bit 的 PCM 信号
- 支持分辨率为 0.5dB 并且从-15dB 到 45dB 增益可调

11.1.2 使用说明

PDM(脉冲密度调制) 模块旨在支持数字麦克风。

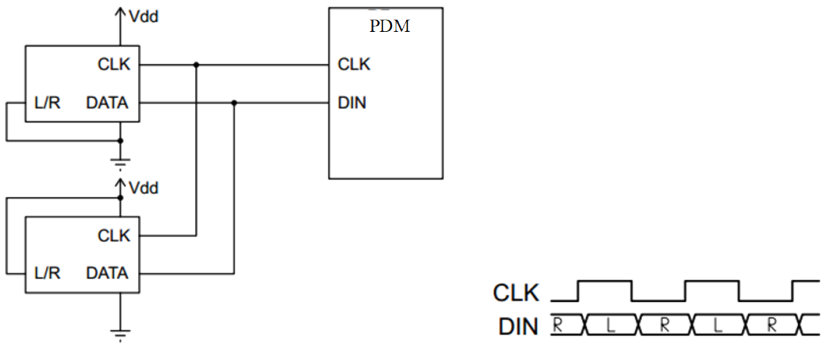

图 11-1: 数字麦克风通过 PDM 模块的典型连接

上图所示为一对数字麦克风通过 PDM 模块的典型连接，两个麦克风共用同一比特流时钟和数据线。借助麦克风的配置引脚 (L/R)，其中一个麦克风可在 CLK 上升沿提供有效数据，而另一个麦克风则在 CLK 下降沿提供有效数据。

11.1.2.1 PDM 模块的整体结构

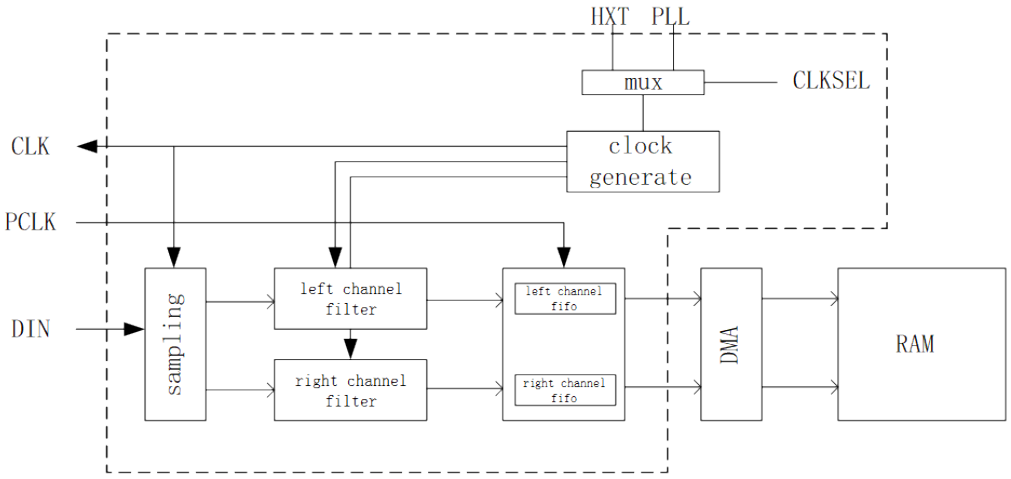

图 11-2: PDM 模块的整体结构

11.1.2.2 PDM 模块的时钟结构

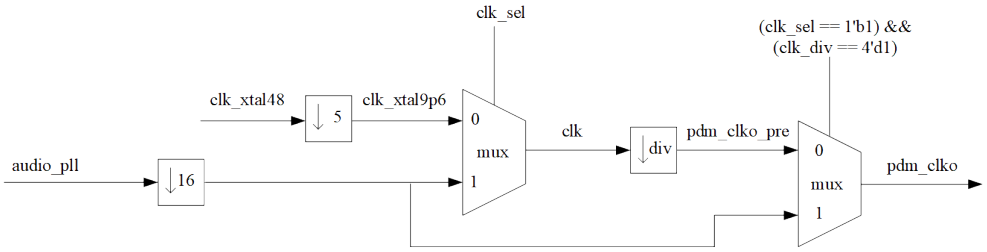

图 11-3: PDM 模块的时钟结构

PDM 模块的时钟源有两个，一个是系统的 48mHz 晶振，一个是系统的音频 PLL 经过 16 倍分频的时钟。而 48mHz 晶振在 PDM 模块内部先经过一个 5 倍的分频器得到一个 9.6mHz 的时钟，此时钟和音频 PLL 的时钟进行二选一，在经过可以配置的分频器得到最终送给数字麦克风的时钟 pdm_clko。pdm 模块最终的输出数据速率为 pdm_clko/(sinc_rate×lpf_downsample)。其中 sinc_rate 和 lpf_downsample 根据如下表格对寄存器 sinc_rate 以及 lpf_ds 进行配置得到最终的数据。

表 11-1: PDM 麦克风时钟源以及对应输出数据速率的配置关系表

PDM_CLK(MHz)	Fs (PCM 输出 Rate, KHz)	OSR（过采样率）	SINC RATE(CIC 下采样率)	LPF 后下采样率	SINC ORDER
3.072	48	64	32	2	3
3.072	32	96	48	2	3
3.072	24	128	64	2	3
3.072	16	192	96	2	3
3.072	12	256	64	4	3
3.072	8	384	96	4	3
1.536	48	32	16	2	4
1.536	32	48	24	2	4
1.536	24	64	32	2	3

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表 11-1: PDM 麦克风时钟源以及对应输出数据速率的配置关系表（续）

PDM_CLK(MHz)	Fs (PCM 输出 Rate, KHz)	OSR（过采样率）	SINC RATE(CIC 下采样率)	LPF 后下采样率	SINC ORDER
1.536	16	96	48	2	3
1.536	12	128	64	2	3
1.536	8	192	96	2	3
0.768	24	32	16	2	4
0.768	16	48	24	2	4
0.768	12	64	32	2	3
0.768	8	96	24	4	4
1.024	32	32	16	2	4
1.024	16	64	32	2	3
1.024	8	128	64	2	3
2.4	48	50	25	2	4
2.4	24	100	50	2	3
2.4	16	150	75	2	3
2.4	12	200	100	2	3
2.4	8	300	75	4	3
1.6	32	50	25	2	4
1.6	16	100	50	2	3
1.6	8	200	100	2	3
0.8	16	50	25	2	4
0.8	8	100	50	2	3
2.4	32	75	75	LPF bypass	3
1.2	48	25	25	LPF bypass	4
1.2	24	50	25	2	4
1.2	16	75	75	LPF bypass	3
1.2	12	100	50	2	3
1.2	8	150	75	2	
2.8224	44.1	64	32	2	3
2.8224	22.05	128	64	2	3
2.8224	11.025	256	64	4	3
1.4112	44.14	32	16	2	4
1.4112	22.05	64	32	2	3
1.4112	11.025	128	64	2	3
0.7056	22.05	32	16	2	4
0.7056	11.025	64	32	2	3

以表中第一行的配置为例对 PDM 模块的寄存器配置进行说明。输出时钟 3.072mHz，输出数据速率 48kHz。输出数据位宽 16 比特，双声道打开。

PDM 寄存器的配置流程：

1. 根据表格选择输出的速率。根据表中的 PDM_CLK 选择时钟源，配置 0x00 中 clk_sel 寄存器，0x0 表示 pdm 模块的输入时钟为 9.6mHz，0x1 表示 pdm 模块的输入时钟为音频 PLL 的十六分频时钟。此例 clk_sel 的配置为 1。（音频时钟的配置不在此处讨论）
2. 根据表格中 SINC RATE 以及 SINC ORDER 配置 0x08 中 sinc_rate 以及 sinc_order_sel 寄存器，其中 sinc_order_sel 为 1 对应表格中 SINC ORDER 为 4，0 对应 3。根据 LPF 后下采样率配置 0x34 中 lpf_ds 寄存器以及 lpf_bypass 寄存器，配置 lpf_ds 寄存器 1 表示对应 excel 中 lpf 下采样 4，配置 lpf_ds 寄存器 0 表示对应 excel 中 lpf 下采样 2，配置 lpf_bypass 为 1 对应表格中的 LPF BYPASS。此例 0x08 sinc_rate=64，sinc_order_sel=0，0x34

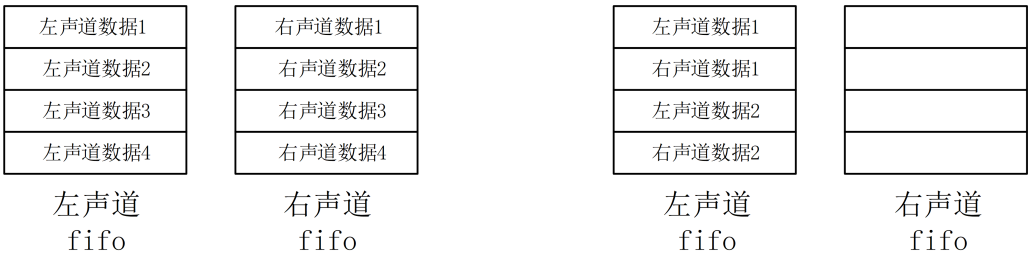
lpf_ds=0。

3. 根据声道配置打开对应的使能信号：

		双声道		左声道	右声道
寄存器 0x0 CFG0	left_en	1	0	1	0
	right_en	1	0	0	1
	stereo_en	0	1	0	0

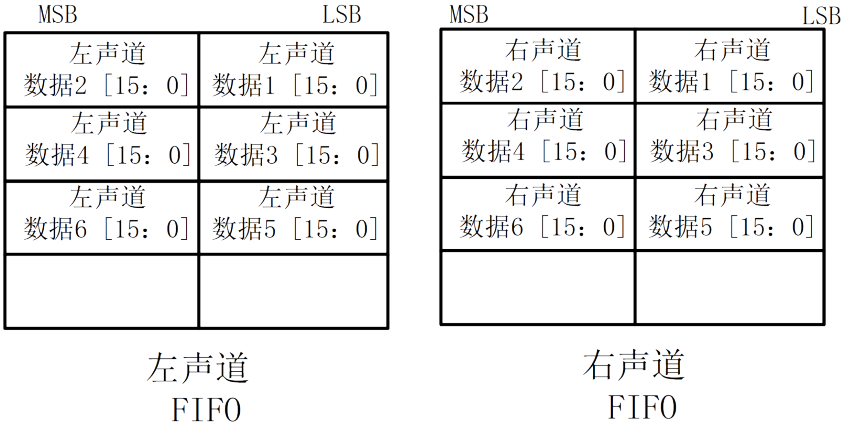
在 0x0 的 swap_en 寄存器为 0 时，pdm 模块认为的右声道采集的是 pdm mic 上升沿输出的数据，左声道采集的是 pdm mic 下降沿输出的数据；在 0x0 的 swap_en 寄存器为 1 时则正好相反，pdm 模块认为的右声道采集的时 pdm mic 下降沿输出的数据，左声道采集的时 pdm mic 上升沿输出的数据。根据需求进行配置。此例 0x0 stereo_en=1 left_en=0 rignt_en=0 或者 stereo_en=0 left_en=1 rignt_en=1。

4. 根据 pdm 模块的输出数据格式进行配置，输出数据的位宽不同对 0x38 的 byte_trunc 寄存器进行配置，配置 0 对应 24bits 输出，配置 1 对应 16bits 输出，配置 2 对应 8bits 输出，配置 3 对应 32bits 输出。此例 0x38 byte_trunc 为 1。
5. 根据左右声道数据是否需要混合到一起配置 0x38 的 byte_con 寄存器，配置 0 左右两个声道的数据各自存到各自的 fifo 中，配置 1 则左右两个声道的数据都存在左声道的 fifo 中。不同 byte_con 寄存器配置对应的输出数据的存储区别示意图。



不满 32 比特的数据会自动将下一个数据的低位补到上一个数据的高位凑成 32 比特数据，以 24 比特双声道数据，byte_con 为 1 为例如下图所示。

以 16 比特双声道数据，byte_con 为 0 为例如下图所示。



此例中对数据存储格式没有要求，请使用者根据需求自行选择配置。

6. 根据 dma 的使用说明配置 dma 的寄存器用去将 pdm fifo 中的数据一次一个 32 比特数据通过 dma 搬到指定的 ram 地址中。
7. 配置 0x0 中 pdmcoreen 寄存器使能 pdm 模块。

1~6 的顺序不固定，只要在 7 之前完成即可。

11.1.2.3 注意事项

PDM 模块产生的中断都是 fifo 出现溢出产生错误发出的中断。

11.1.3 PDM 寄存器

表 11-2: PDM 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00			**CFG0**	
[31:10]			RSVD	
[9]	rw	1'b0	swap_en	1: Swap right channel and left channel pdm data; 0: Not swap right channel and left channel pdm data
[8]	rw	1'b0	stereo_en	1:Enable double channels pdm data sampling; 0: Disable double channels pdm data sampling
[7]	rw	1'b0	right_en	1: Enable right channel pdm data sampling; 0: Disable right channel pdm data sampling
[6]	rw	1'b0	left_en	1: Enable left channel pdm data sampling; 0: Disable left channel pdm data sampling
[5:2]	rw	4'h4	clk_div	Clock frequency division ratio of 3.072MHz or 9.6MHz according to register clk_sel
[1]	rw	1'b0	clk_sel	1:Clk select dll 3.072MHz; 0: Clk selct xtal 9.6MHz
[0]	rw	1'b0	pdmcoreen	1:Enable pdm module; 0: Disable pdm module
0x04			**CFG1**	
[31:11]			RSVD	
[10:8]	rw	3'h0	sample_dly_r	The number of delay dff before the right data stream in processing
[7:5]	rw	3'h0	sample_dly_l	The number of delay dff before the left data stream in processing
[4:0]			RSVD	
0x08			**SINC_CFG**	

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表 11-2: PDM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:9]			RSVD	
[8]	rw	1'b1	sinc_order_sel	1:select four differentiators in sinc filter; 0:select three differentiators in sinc filter
[7:0]	rw	8'd32	sinc_rate	dowmsampling rate of sinc filter
0x14			**HPF_CFG**	
[31:6]			RSVD	
[5]	rw	1'b1	hpf_rst	1:high-pass filter normal operation ; 0:reset high-pass filter
[4]	rw	1'b0	hpf_bypass	1:bypass-high pass filter ; 0: enable high-pass filter
[3:0]	rw	4'hd	hpf_coeff	coefficient of high-pass filter
0x18			**PGA_CFG**	
[31:14]			RSVD	
[13:7]	rw	7'd0	pga_gain_r	right channel gain control , the range is -15dB~45dB. Resolution is 0.5dB/LSB
[6:0]	rw	7'd0	pga_gain_l	left channel gain control , the range is -15dB~45dB. Resolution is 0.5dB/LSB
0x34			**LPF_CFG6**	
[31:14]			RSVD	
[13]	rw	1'b0	lpf_bypass	1:bypass low-pass filter ; 0: enable low-pass filter
[12]	rw	1'b0	lpf_ds	1:downsampling rate of low pass filter is two;0:No downsampling of low pass filter
[11:0]			RSVD	
0x38			**FIFO_CFG**	
[31:9]			RSVD	
[8]	rw	1'b0	lr_chg	1:exchange storage location of left and right channel; 0: don't exchange storage location of left and right channel
[7]	rw	1'b0	rx_dma_msk_l	1:disable left channel dma request; 0: enable left channel dma request
[6]	rw	1'b0	rx_dma_msk_r	1:disable right channel dma request; 0: enable right channel dma request
[5:3]	rw	3'h0	pdm_shift	the number of data left shift for higher data accuracy
[2:1]	rw	2'b0	byte_trunc	1: 16bits output ; 0: 24bits output ;2: 8bits output ; 3: 32bits output
[0]	rw	1'b0	byte_con	1: combine left channel and right channel; 0: not combine left channel and right channel
0x44			**FIFO_ST**	
[31:8]			RSVD	
[7]	r	1'h0	full_l	1 indicates left channel fifo is full
[6]	r	1'b0	empty_l	1 indicates left channel fifo is empty
[5]	r	1'b0	almost_full_l	1 indicates left channel fifo is less than two full
[4]	r	1'b0	almost_empty_l	1 indicates left channel fifo is less than two datas left
[3]	r	1'h0	full_r	1 indicates right channel fifo is full
[2]	r	1'b0	empty_r	1 indicates right channel fifo is empty
[1]	r	1'b0	almost_full_r	1 indicates right channel fifo is less than two full
[0]	r	1'b0	almost_empty_r	1 indicates right channel fifo is less than two datas left
0x48			**INT_ST**	
[31:2]			RSVD	
[1]	r	1'b0	overflow_l	1 indicates left channel fifo has already overflowed and as irq at same time
[0]	r	1'b0	overflow_r	1 indicates right channel fifo has already overflowed and as irq at same time
0x4c			**INT_MSK**	
[31:2]			RSVD	
[1]	rw	1'b0	int_mask_l	1:disable left channel irq to system; 0: enable left channel irq to system
[0]	rw	1'b0	int_mask_r	1:disable right channel irq to system; 0: enable right channel irq to system
0x50			**INT_CLR**	
[31:2]			RSVD	

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表 11-2: PDM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[1]	w1c	1'b0	int_clr_l	clear left channel irq
[0]	w1c	1'b0	int_clr_r	clear right channel irq

11.2 I2S

芯片有 1 个 I2S，位于 HPSYS，输入输出连接至 IO(PA)，可向 DMAC1 发送请求。

11.2.1 简介

I2S(也叫 IIS，即：Inter IC Sound) 总线, 又称集成电路内置音频总线，是飞利浦公司为数字音频设备之间的音频数据传输而制定的一种总线标准，该总线采用主/从模式，专责于音频设备之间的数据传输，广泛应用于各种多媒体系统。

目前 I2S 有 MSB 对齐（左对齐），LSB 对齐（右对齐）和 I2S 标准模式。

I2S 标准模式如下图所示：

数据在跟随 LRCLK 传输的 BCLK 的第二个上升沿时传输 MSB，其他位一直到 LSB 按顺序传。传输依赖于字长、BCLK 频率和采样率 (BCLK=Fs x 声道数 x 采样位数)，在每个采样的 LSB 和下一个采样的 MSB 之间都应该有未用的 BCLK 周期，LRCLK 为 0 传输左声道数据，LRCLK 为 1 传输右声道数据。

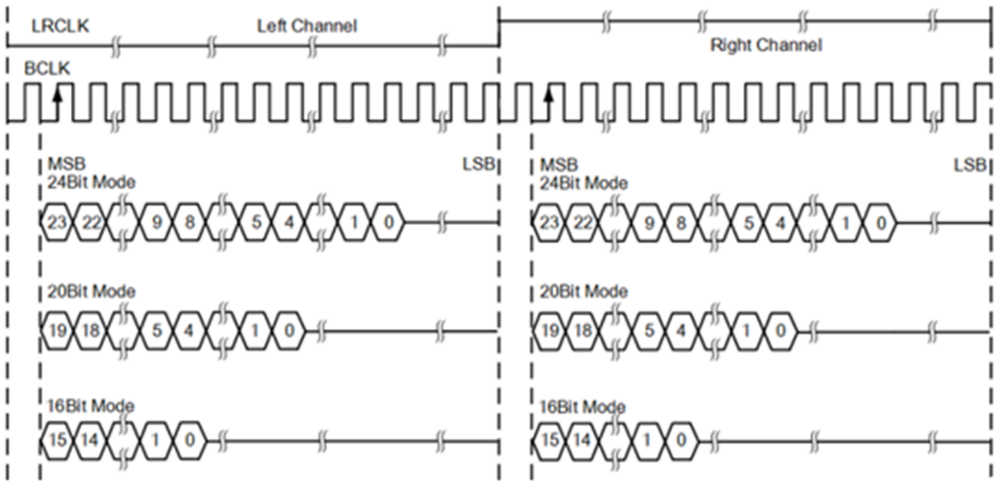

图 11-4: I2S 标准模式

I2S 左对齐如下图所示：

标准左对齐格式的数据的 MSB 没有相对于 BCLK 延迟一个时钟。左对齐格式的左右声道数据的 MSB 在 LRCLK 边沿变化后 BCLK 的第一个上升沿有效。LRCLK 为 1 传输左声道数据，LRCLK 为 0 传输右声道数据。

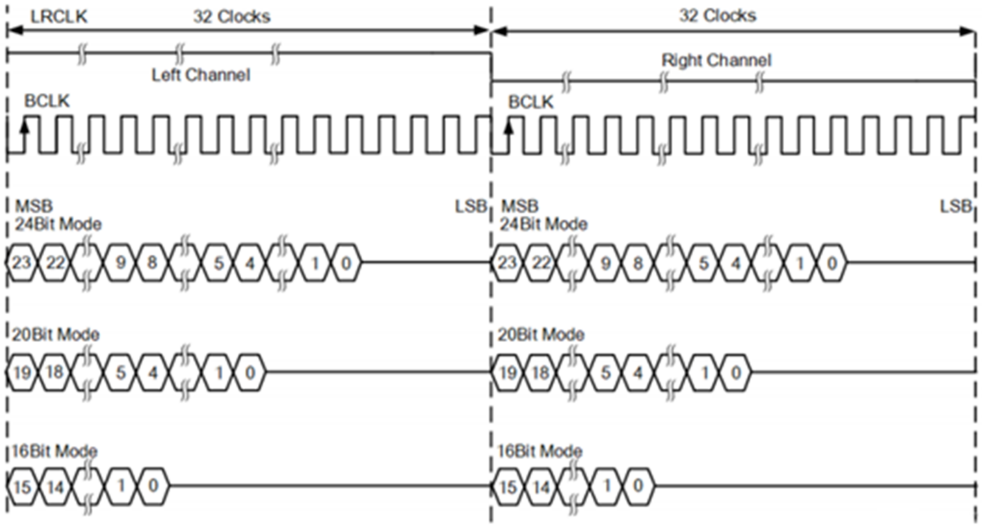

图 11-5: I2S 左对齐

I2S 右对齐如下图所示：

声音数据 LSB 传输完成的同时，LRCLK 完成第二次翻转，LRCLK 为 1 传输左声道数据，LRCLK 为 0 传输右声道数据。

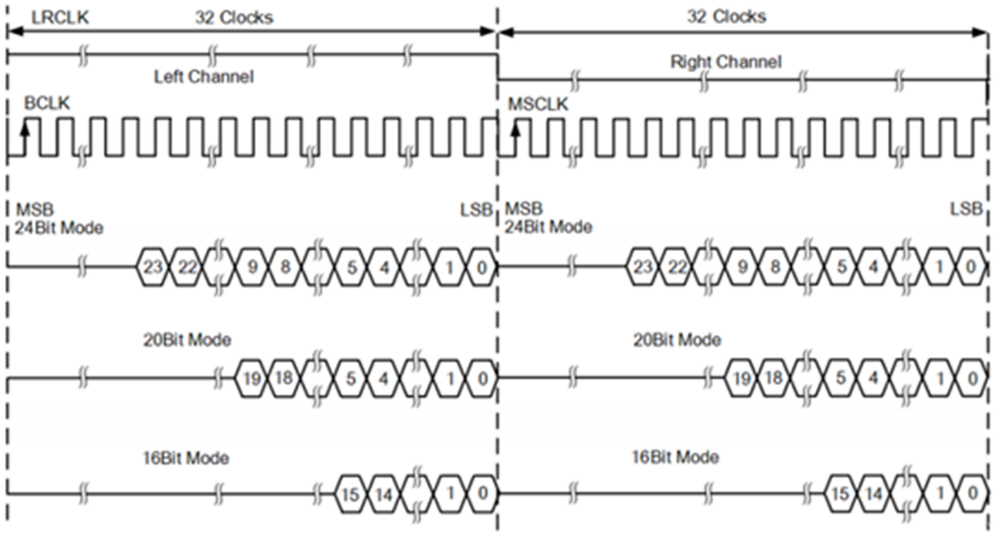

图 11-6: I2S 右对齐

11.2.2 I2S 功能描述

I2S 模块可以支持主从两种模式。主模式时，MCU 可以提供采样时钟 LRCK 和 bit 时钟 BCLK。从模式时，BCLK 和 LRCK 由外部提供，MCU 负责 I2S 的数据收发。

I2S 模块共支持左对齐和右对齐三种数据格式。在主模式下，用户可以根据需求定义 BCLK 和 LRCK 的比例关系。

当前版本的 I2S 模块还额外提供了 MCLK 的输出，MCLK 是与 BCLK 和 LRCK 同步的更高频率的时钟，可以提

供给 I2S 外设更高的工作频率，用户也可以根据需求定义 MCLK 的频率。除此以外，I2S 时钟源增加了 PLL 的选项，这样提高了 I2S 时钟的灵活性。

11.2.3 I2S 寄存器

表 11-3: I2S 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x10			**TX_PCM_FORMAT**	
[31:6]			RSVD	
[5]	rw	1'h0	track_flag	0: stereo 1: mono
[4:0]	rw	5'h10	dw	tx source pcm data width N(N>=8) common value is 8,13,14,16,18,20,22,24 This data width indicate the tx fifo output data width. When writing to tx fifo, please refer to following format: Mono 8 bit: fifo_data[31:0] = L3,L2,L1,L0, each word contains 4 samples, so four samples need read one word Stereo 8 bit: fifo_data[31:0] = R1,L1,R0,L0 , each word contains 2 samples, so two samples need read one word Mono 13/14/16 bit: fifo_data[31:0] = L1,L0, each word contains 2 samples, so two samples need read one word Stereo 13/14/16 bit: fifo_data[31:0] = R0,L0, each word contains 1 samples, so each sample need read one word Mono 18/20/22/24 bit: fifo_data[31:0] = L0, each word contains 1 samples, so each sample need read one word Stereo 18/20/22/24 bit: fifo_data[31:0][0] = L0, fifo_data[31:0][1]=R0, each 2 words contain 1 samples, so each sample need read two word
0x20			**TX_PCM_SAMPLE_CLK**	
[31:13]			RSVD	
[12:0]	rw	13'd250	fs_duty	source PCM sample clock duty cycle(with GCLK=12MHz): 250 for 48K FS 272 for 44.1K FS 375 for 32K FS 500 for 24K FS 544 for 22.05K FS 750 for 16K FS 1000 for 12K FS 1088 for 11.025K FS 1500 for 8K FS
0x30			**TX_RS_SMOOTH**	
[31:1]			RSVD	
[0]	rw	1'h0	en	0: Disable TX re-sample smooth filter 1: Enable TX re-sample smooth filter This function is not implemented.
0x40			**TX_PCM_CH_SEL**	
[31:4]			RSVD	

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表 11-3: I2S 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[3:2]	rw	2'h0	left_channel_sel	TX re-sampling module setting: 00: TX left = source left 01: TX left = source right 10,11: TX left = (source left + source right)/2
[1:0]	rw	2'h0	right_channel_sel	TX re-sampling module setting: 00: TX right = source right 01: TX right = source left 10,11: TX right = (source left + source right)/2
0x50			**TX_VOL_CTRL**	
[31:4]			RSVD	
[3:0]	rw	4'hf	vol	volume control: 0000: +6dB, 0001: +4.5dB, 0010: +3dB, 0011: +1.5dB, 0100: 0dB, 0101: -1.5dB, 0110: -3.0dB, 0111: -4.5dB, 1000: -6.0dB, 1001: -7.5dB, 1010: -9dB, 1011: -10.5dB, 1100: -12dB, 1101: -13.5dB, 1110: -15dB, 1111: mute Note: 1) +1.5db = 20log(1+1/4-1/16+1/1024) 2) -1.5dB = 20log(1-1/8-1/32-1/512-1/2048)
0x60			**TX_LR_BAL_CTRL**	
[31:6]			RSVD	
[5:4]	rw	2'h0	en	LR balance enable: 00: both left and right in full volume 10: left channel balance volume adjustment enable 01: right channel balance volume adjustment enable 11: reserved, still kepp left and right in full volume
[3:0]	rw	4'h0	bal_vol	Balance volume control: 0000: Reserved, 0001: -1.5dB, 0010: -3.0dB, 0011: -4.5dB, 0100: -6.0dB, 0101: -7.5dB, 0110: -9.0dB, 0111: -10.5dB, 1000: -12dB, 1001: -13.5dB, 1010: -15dB, 1011: -16.5dB, 1100: -18dB, 1101: -19.5dB, 1110: -21dB, 1111: mute Note: 1) bit[5:0] = 101111 for left mute 2) bit[5:0] = 011111 for right mute 3) bit[5:4] = 00 or 11, bit[3:0] is don't care 4) +1.5db = 20log(1+1/4-1/16+1/1024) 5) -1.5dB = 20log(1-1/8-1/32-1/512-1/2048)
0x70			**AUDIO_TX_LRCK_DIV**	
[31:28]			RSVD	

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表 11-3: I2S 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[27:16]	rw	12'd125	duty_high	TX LRCK duty cycle high: 125 for 48K FS 136 for 44.1K FS 185 for 32K FS 250 for 24K FS 272 for 22.05K FS 375 for 16K FS 500 for 12K FS 544 for 11.025K FS 750 for 8K FS
[15:12]			RSVD	
[11:0]	rw	12'd125	duty_low	TX LRCK duty cycle low: 125 for 48K FS 136 for 44.1K FS 190 for 32K FS 250 for 24K FS 272 for 22.05K FS 375 for 16K FS 500 for 12K FS 544 for 11.025K FS 750 for 8K FS Note: 1)duty_cycle = 12M/FS
0x80			**AUDIO_TX_BCLK_DIV**	
[31:6]			RSVD	
[5:0]	rw	6'h5	duty	TX serial bit clock duty cycle 5 for 48K FS 4 for 44.1K FS 5 for 32KFS 10 for 24K FS 8 for 22.05K FS 15 for 16K FS 20 for 12K FS 16 for 11.025K FS 30 for 8KFs
0x90			**AUDIO_TX_FORMAT**	
[31:5]			RSVD	
[4:0]	rw	5'h10	pcm_data_width	I2S out pcm data width M >= 16, common value: 16, 18, 20, 22, 24
0xa0			**AUDIO_SERIAL_TIMING**	
[31:4]			RSVD	
[3]	rw	1'h0	lrck_pol	TX LRCK polarity control. 0: disable TX_LRCK inventor 1: enable TX_LRCK inventor for standard I2S, set tx_lrck_pol to low for Left/Right Justified, set tx_lrck_pol to hgih
[2]	rw	1'h0	slave_en	audio code transmit mode select. 0: master mode, 1: slave mode

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表 11-3: I2S 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[1:0]	rw	2'h0	timing	00: I2S mode 01: Left justified 10: right justified 11: reserved
0xb0			**AUDIO_TX_FUNC_EN**	
[31:2]			RSVD	
[1]	rw	1'h0	tx_intf_sel	1: select external tx interface 0: select internal apb tx interface
[0]	rw	1'h0	tx_en	1: enable 0:disable
0xc0			**AUDIO_TX_PAUSE**	
[31:1]			RSVD	
[0]	rw	1'h0	tx_pause	TX pause control when tx_enable = 1. 1: pause 0: TX work
0xc8			**AUDIO_I2S_SL_MERGE**	
[31:1]			RSVD	
[0]	rw	1'h0	slave_timing_merge	when work as an I2S slave, and external I2S master TX/RX share an only BCLK/LRCK, we need set this bit high. 0: I2S slave use separated timing control port. TX_BCLK_IN/TX_LRCK_IN and RX_BCLK/RX_LRCK_IN are separated. 1: I2S slave use the same BCLK/LRCK, the TX_BCLK_IN/TX_LRCK also is used for RX controller.
0x100			**AUDIO_RX_FUNC_EN**	
[31:2]			RSVD	
[1]	rw	1'h0	rx_intf_sel	1: select external rx interface 0: select internal apb rx interface
[0]	rw	1'h0	rx_en	1: enable 0: disable
0x110			**AUDIO_RX_PAUSE**	
[31:1]			RSVD	
[0]	rw	1'h0	rx_pause	RX pause control when rx_enable = 1. 1: pause 0: RX work
0x120			**AUDIO_RX_SERIAL_TIMING**	
[31:4]			RSVD	
[3]	rw	1'h0	lrck_pol	RX LRCK polarity control. 0: disable RX_LRCK inventor 1: enable RX_LRCK inventor for standard I2S, set tx_lrck_pol to low for Left/Right Justified, set tx_lrck_pol to hgih
[2]	rw	1'h0	slave_en	audio code receiver mode select. 0: master mode, 1: slave mode
[1:0]	rw	2'h0	timing	00: I2S 01: Left justified 10: right justified 11: reserved
0x130			**AUDIO_RX_PCM_DW**	
[31:5]			RSVD	
[4:0]	rw	5'h10	pcm_data_width	For I2S and left justified mode, M can be 8,13,14,16 For right justified mode, M can be 8, 13, 14, 16, 18, 20, 22, 24
0x140			**AUDIO_RX_LRCK_DIV**	

续表下页...

表 11-3: I2S 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:28]			RSVD	
[27:16]	rw	12'd125	duty_high	RX LRCK duty cycle high: 125 for 48K FS 136 for 44.1K FS 185 for 32K FS 250 for 24K FS 272 for 22.05K FS 375 for 16K FS 500 for 12K FS 544 for 11.025K FS 750 for 8K FS
[15:12]			RSVD	
[11:0]	rw	12'd125	duty_low	RX LRCK duty cycle low: 125 for 48K FS 136 for 44.1K FS 190 for 32K FS 250 for 24K FS 272 for 22.05K FS 375 for 16K FS 500 for 12K FS 544 for 11.025K FS 750 for 8K FS Note: 1)duty_cycle = 12M/FS
0x150			**AUDIO_RX_BCLK_DIV**	
[31:10]			RSVD	
[9:0]	rw	10'h5	duty	RX serial bit clock duty cycle 5 for 48K FS 4 for 44.1K FS 5 for 32KFS 10 for 24K FS 8 for 22.05K FS 15 for 16K FS 20 for 12K FS 16 for 11.025K FS 30 for 8KFs
0x160			**RECORD_DATA_SEL**	
[31:1]			RSVD	
[0]	rw	1'h0	rs_data_sel	0: I2S audio recording 1: BT recording
0x170			**RX_RE_SAMPLE_CLK_DIV**	
[31:13]			RSVD	

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表 11-3: I2S 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[12:0]	rw	13'd250	rs_duty	source PCM sample clock duty cycle: 250 for 48K FS 272 for 44.1K FS 375 for 32K FS 500 for 24K FS 544 for 22.05K FS 750 for 16K FS 1000 for 12K FS 1088 for 11.025K FS 1500 for 8K FS Note: 1)duty_cycle = 12M/FS
0x180			**RX_RE_SAMPLE**	
[31:1]			RSVD	
[0]	rw	1'h0	smooth_en	0: Disable RX re-sample smooth filter 1: Enable RX re-sample smooth filter
0x190			**RECORD_FORMAT**	
[31:2]			RSVD	
[1]	rw	1'h0	track	1: mono recording, 0: stereo recording
[0]	rw	1'h0	dw	0: 8bit 1: 16bit RX fifo data format: Mono 8 bit (unsigned): RX FIFO_DIN[31:0] = L3,L2,L1,L0, each four samples need one FIFO write operation Stereo 8 bit (unsigned): RX_FIFO_DIN[31:0] = R1,L1,R0,L0, each tow samples need one FIFO write operation Mono 16 bit (Signed 2's complement): RX_FIFO_DIN[31:0] = L1,L0, each two samples need one FIFO write operation Stereo 16 bit (Signed 2's complement): RX_FIFO_DIN[31:0] = R0,L0, each sample need one FIFO write operation
0x1a0			**RX_CH_SEL**	
[31:4]			RSVD	
[3:2]	rw	2'h0	left_channel_sel	RX re-sampling module setting: 00: RD left = RX left 01: RD left = RX right 10,11: RD left = (RX left + RX right)/2
[1:0]	rw	2'h0	right_channel_sel	RX re-sampling module setting: 00: RD right = RX right 01: RD right = RX left 10,11: RD right = (RX left + RX right)/2
0x200			**BT_PHONE_CTRL**	
[31:6]			RSVD	
[5]	rw	1'h0	bb_i2s_bps_to_cdc	bypass baseband I2S interface to audio codec i2s interface 0: no bypass, 1: bypass
[4]	rw	1'h0	bt_pcm_if_bps	bypass baseband PCM signals to BT VCI master: 0: no bypass, 1: bypass
[3]	rw	1'h0	bt_path_sel	BT path select 0: digital path, 1: analog path
[2]	rw	1'h0	bt_mix_smooth_filter_en	0: disable the smooth filter for background mixer 1: enable the smooth filer for background mixer

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表 11-3: I2S 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[1]	rw	1'h0	bt_back_mix_en	background mixer enable 0: disable, 1: enable
[0]	rw	1'h0	bt_ph_en	BT phone enable 0: disable, 1: enable
0x210			**BB_PCM_FORMAT**	
[31:11]			RSVD	
[10]	rw	1'h0	pcm_clk_pol	input BB pcm clock polarity: 0: rising edge for data transmitting, falling edge for data receiving 1: rising edge for data receiving, falling edge for data transmitting
[9]	rw	1'h0	i2s_lrck_pol	0: no bb_i2s_lrck input inventor 1: enable bb_i2s_lrck input inventor for standard I2S, set tx_lrck_pol to low for Left/Right Justified, set tx_lrck_pol to high
[8]	rw	1'h0	pcm_lsb_flag	Serial PCM data bit sequence. 0: MSB first, 1: LSB first
[7]	rw	1'h0	pcm_sync_flag	0: short sync, 1: long sync
[6:5]	rw	2'h0	pcm_tim_sel	00: I2S timing, 01: Left Justified 10: Right Justified, 11: PCM timing
[4:0]	rw	5'h8	pcm_dw	Baseband Master PCM data width (>=8) Common value: 8, 13,14, 16, 18, 20, 22, 24. for I2S/Left Justified/Right Kistified timing, bb_pcm_dw >=16 For PCM timing, only 8, 13, 14, 16 configure value is available.
0x220			**BT_PCM_DW**	
[31:5]			RSVD	
[4:0]	rw	5'h10	dw	BT PCM master data width (>= 8), common value: 8, 13,14, 16
0x230			**BT_PCM_TIMING**	
[31:3]			RSVD	
[2]	rw	1'h0	clk_pol	BT PCM master output pcm clock polarity: 0: rising edge for data transmitting, falling edge for data receiving 1: rising edge for data receiving, falling edge for data transmitting
[1]	rw	1'h0	sync_flag	0: short sync, 1: long sync
[0]	rw	1'h0	lsb_flag	Serial PCM data bit sequence. 0: MSB first, 1: LSB first
0x240			**BT_PCM_CLK_DUTY**	
[31:10]			RSVD	
[9:0]	rw	10'h0	clk_duty	BT_PCM_CLK duty cycle <= (GCLK/(bt_pcm_sync*bt_pcm_dw))
0x250			**BT_PCM_SYNC_DUTY**	
[31:6]			RSVD	
[5:0]	rw	6'h0	sync_duty	PCM_SYNC duty cycle (bt_pcm_sync frequency = bt_pclk_clk/bt_pcm_sync_duty)
0x260			**BT_VOL_CTRL**	
[31:4]			RSVD	
[3]	rw	1'h0	vol_adj_en	BT volume adjust enable
[2:0]	rw	3'h0	vol	BT master volume
0x300			**INT_MASK**	
[31:2]			RSVD	

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表 11-3: I2S 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[1]	rw	1'h1	tx_fifo_int_mask	Interrupt mask for TX FIFO pop underflow, high active
[0]	rw	1'h1	rx_fifo_int_mask	Interrupt mask for RX FIFO push overflow, high active
0x310			**INT_STATUS**	
[31:2]			RSVD	
[1]	rw	1'h0	tx_fifo_underflow	TX FIFO pop underflow
[0]	rw	1'h0	rx_fifo_overflow	RX FIFO push overflow
0x400			**TX_DMA_ENTRY**	
[31:0]	w	32'h0	tx_dma_entry	TX DMA entry
0x440			**RX_DMA_ENTRY**	
[31:0]	r	32'h0	rx_dma_entry	RX DMA entry
0x480			**DMA_MASK**	
[31:2]			RSVD	
[1]	rw	1'h1	tx_dma_mask	TX DMA mask enable:1: mask0: do not mask
[0]	rw	1'h1	rx_dma_mask	RX DMA mask enable:1: mask0: do not mask
0x500			**DEBUG_LOOP**	
[31:24]			RSVD	
[23:16]	rw	8'h2	sp_clk_div	sp clock divider value
[15:9]			RSVD	
[8]	w1c	1'h0	sp_clk_div_update	update sp clock divider
[7:3]			RSVD	
[2]	rw	1'h0	sp_clk_sel	clock select 0: xtal clock 1: pll clock
[1]	rw	1'h0	ad2da_loop_back	RX–>TX Loop debug control: 0: disable 1: enable, internally connect RX Resampled PCM to TX Resample PCM input
[0]	rw	1'h0	da2ad_loop_back	TX–>RX Loop debug control: 0: disable 1: enable, internally connect TX SDTO to RX SDTI
0x600			**FIFO_STATUS**	
[31:8]			RSVD	
[7:0]	rw	8'h0	fifo_status_out	FIFO Status output: Bit [7:0] = tx_full,tx_empty,tx_almost_full,tx_almost_empty,rx_full,rx_empty,rx_almost_f
0x700			**TX_EQUALIZER_EN**	
[31:1]			RSVD	
[0]	rw	1'h0	tx_equalizer_en	0: Disable TX equalizer 1: Enable TX equalizer equalizer is not implemented
0x710			**TX_EQUALIZER_GAIN1**	
[31:30]			RSVD	
[29:25]	rw	5'h0	band6_gain	
[24:20]	rw	5'h0	band5_gain	
[19:15]	rw	5'h0	band4_gain	
[14:10]	rw	5'h0	band3_gain	
[9:5]	rw	5'h0	band2_gain	
[4:0]	rw	5'h0	band1_gain	
0x720			**TX_EQUALIZER_GAIN2**	

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表 11-3: I2S 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:20]			RSVD	
[19:15]	rw	5'h0	band10_gain	
[14:10]	rw	5'h0	band9_gain	
[9:5]	rw	5'h0	band8_gain	
[4:0]	rw	5'h0	band7_gain	

11.3 Audprc

Audprc 位于 HPSYS。

11.3.1 简介

Audprc 模块全称 Audio Process Controller，其主要功能是对采集和播放音频数据进行处理后，并将处理后的数据送到指定的模块。Audprc 内对音频的处理功能有增益调节，混音，均衡调节，采样率转换，用户可以根据需要对这些功能进行单独配置。

11.3.2 系统架构

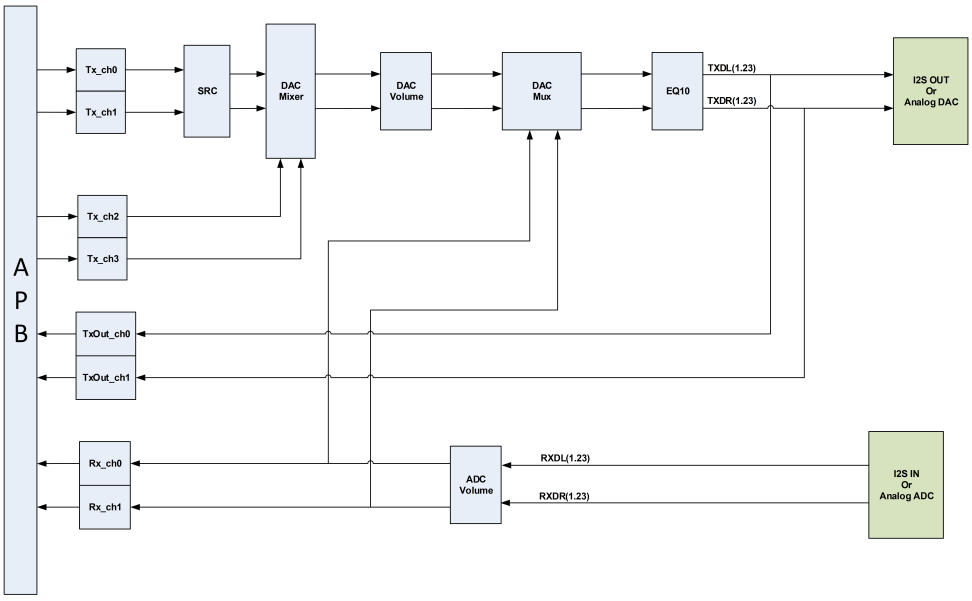

图 11-7: Audprc 结构图

Audprc 主要由两部分通路组成，输出的 TX 通路和接受的 RX 通路。TX 通路将数据从内存空间送至 I2S 输出端或者模拟的 DAC。RX 通路则从 I2S 输入端或者模拟的 ADC 接受数据，并存储到内存空间。

11.3.3 功能描述

11.3.3.1 采样率转换模块

采样率转换模块 SRC 可以根据需求改变音频数据的采样率，转换的范围是 1/16~16。采样率转换模块由多级 Half-band 滤波器和 Sinc 滤波器组成，用户需要根据输入输出的采样率，对采样率转换模块的参数进行配置，达到需要的转换比例。

采样率转换模块内部共有三级 Half-band 滤波器，以及一级 Sinc 滤波器。每一级 Half-band 滤波器可以实现 2 倍的上采样或者下采样，Sinc 滤波器可以实现 0.5~2 以内的高精度采样率转换。总的采样率转换比例：

$$Ratio = Ratio(hb1) * Ratio(hb2) * Ratio(hb3) * Ratio(sinc)$$

三级 Half-band 滤波器结构相同，配置方法也相同。如果需要实现 2 倍上采样，则配置 Hbf enable 为 1，同时 mode 设置为 0。如果需要实现 2 倍下采样，则配置 Hbf enable 为 1，同时 mode 设置为 0。默认情况下 Hbf 的 enable 为 0，表示该级 Half-band 滤波器不工作，不会改变采样率。三级 Half-band 滤波器的配置，要尽可能逼近最终的目标采样率转换比例。

最后一级 Sinc 滤波器有两个配置参数，是能 enable 和采样率转换比例 Sinc_ratio。Sinc_ratio 为 31bit 定点无符号数，包含 1 位整数位和 30 位小数位，对应的精度为 $1/2^{30}$。

以下将以 16KHz 转 44.1KHz 为例，对 SRC 进行配置。

16KHz 转 44.1KHz 有两种比较简单的方式：

- 方案一：16KHz->32KHz->44.1KHz
- 方案二：16KHz->32KHz->64KHz->44.1KHz

这两种情况理论上都可以，方案一中，采用一级 Half-band 滤波器进行 2 倍上采样，然后使用 Sinc 滤波器 Ratio 为 1.378 倍。方案二中，采样两级 Half-band 滤波器进行共 4 倍上采样，然后 Sinc 滤波器 Ratio 为 0.689 倍。两种方案相比较，方案二中 Sinc 滤波器的 Ratio 更接近 1，滤波器性能上会更好一些，所以选择方案二。

11.3.3.2 混音模块

混音模块 (DAC Mixer,DAC Mux) 是在 DAC 通路上，将不同源头的音频源混合在一起。

DAC Mixer 的输入是四路 TX 数据，四路音频经过重新组合，变成两路音频输出。输出的每一路都由两路音频数据相加而得，这两路音频数据可以来自与 TX 的四路数据，也可以选择静音。具体可以参考寄存器 mixlsrc0，mixlsrc1，mixrsrc0，mixrsrc1。

DAC Mux 的输入是 DAC 的两路数据，和 ADC 的两路数据。Mux 的混音方式与 Mixer 相同，也是将四路输入混合成两路输出，每一路的音频源可以任意配置。具体可以参考寄存器 muxlsrc0，muxlsrc1，muxrsrc0，muxrsrc1。

11.3.3.3 增益调节模块

DAC 和 ADC 通路由独立的增益调节模块 Volume，左右两路音频调节各自独立。范围是-18~13dB，步进是 0.5dB。

11.3.3.4 均衡器模块

均衡器模块 EQ 最多支持 10 级独立调节，用户需要配置 eq_stage 来使能需要的级数。每一级有 5 个参数，共 50 个参数可以配置。用户可以使用工具产生想要的均衡器效果，然后将参数配置入 Audprc。均衡器在使用前需要先使能 eq_clr，等到 eq_clr_done 为 1 后，清除 eq_clr 即可，这一步骤是为了清除内部临时数据残留。如果不进

行清除，均衡器模块收敛时间会长一点，且有可能开启时会有瞬时噪声。

11.3.4 配置流程

11.3.4.1 配置 Tx 和 Rx 通道

Audprc 的 Tx 通道可以支持单声道 16bit/24bit 和立体声 16bit 的音频数据格式，最多支持 4 路音频（立体声占用两路）。每个 Tx 通道可以通过配置 format 寄存器，支持单路 16bit/24bit 的音频。对于立体声 16bit 的音频源 (每 32bit 数据包含左右声道各 16bit 的数据)，仅有 Tx 通道 0 和通道 2 可以支持，可以通过 Mode 寄存器进行模式配置。当 Tx 通道 0 配置为立体声 16bit 模式时，Tx 通道 1 就会被占用，无法再使用。同样当 Tx 通道 2 配置为立体声 16bit 模式时，Tx 通道 3 也会被占用，无法再使用。

Audprc 的 Rx 通道可以支持单声道 16bit/24bit 的音频数据格式，最多支持 2 路音频。每个 Rx 通道可以通过配置 format 寄存器，支持单路 16bit/24bit 的音频。

配置完 Tx 和 Rx 的音频数据结构之后，还需要配置对应的 DMA，对 Tx 和 Rx 通道数据收发处理。

11.3.4.2 配置 DAC 通路

DAC 通路配置包含前文提到的各个模块，如 SRC，EQ，Mixer，Mux，Volume。需要注意的是，SRC 和 EQ 均支持输入端两个通道单独使能，配置是只需要使能有音频数据的输入通道即可。另外在配置 Mux 的时候，如果选择 Rx 通道的数据与 Tx 通道的数据混合，需要保证两者的采样率相同，否则会出现混音不同步的问题。

配置完成 DAC 内部模块后，可以通过寄存器 dst_sel 配置 DAC 的输出目标模块。如果 dst_sel 为 0，则 DAC 数据会被送到 Codec 模块，该通路最高支持 24bit 立体声，经过 Codec 模块后，音频数据会被转化成音频模拟信号输出。如果 dst_sel 为 1，则 DAC 数据会被送到 I2S 模块，该通路最高支持 16bit 立体声，数据最后会通过数字 I2S 接口输出。如果 dst_sel 为 2，则 DAC 数据会被送至 Audprc Tx_out 通道，该通道最高支持 24bit 立体声，用户可以配置 DMA 将数据从 Tx_out 通道读取并存储到内存空间。

除此以外，DAC 通路还需要配置采样时钟源和采样分频比。时钟源可以选择芯片内置的音频 PLL 或者 48MHz 晶振，这里需要保证 DAC 通路使用的时钟源与输出目标模块一致，且经过分频后的时钟与输出模块的采样率一致。如果输出模块为 Tx_out 通道，则没有该要求。

11.3.4.3 配置 ADC 通路

ADC 通路配置一个 Volume 模块。配置完 Volume 后可以通过寄存器 src_sel 配置 ADC 的音频源。如果 src_sel 为 0，则 ADC 数据来源为 Codec 模块，该通路最高支持 24bit 立体声，Codec 数据来源于 ADC 采集的外部音频模拟信号。如果 src_sel 为 1，则 ADC 数据来源为 I2S 模块，该通路最高支持 16bit 立体声，音频数据来源于外部 I2S 数字接口。

与 DAC 通路一样，ADC 通路需要配置采样时钟源和分频比，时钟源需要与音频源一致，经过分频后的时钟需要与音频采样率一致。

当 ADC 数据通过 Mux 送到 DAC 通路时，ADC 数据到 Rx 通道的通路不会受到影响，用户可以同时从使能 Rx 通道采集 ADC 的数据。

11.3.5 Audprc 寄存器

表 11-4: Audprc 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00			**id**	
[31:0]	rw	32'hA0000	rev	revision id
0x04			**cfg**	
[31:21]			RSVD	
[20]	w1c	1'h0	audclk_div_update	audprc clock divider update, write 1 to update
[19:16]	rw	4'h2	audclk_div	audprc clock divider, 0 and 1 means divide by 1
[15:10]			RSVD	
[9]	rw	1'h0	stb_clk_sel	audio strobe clock select 0: use xtal clock to generate strobe 1: use pll clock to generate strobe
[8]	rw	1'h0	auto_gate_en	auto clock gating enable, high active
[7]	rw	1'h0	adc_path_en	adc path enable
[6]	rw	1'h0	dac_path_en	dac path enable
[5]	rw	1'h0	adc_path_sreset	adc path software reset, high active
[4]	rw	1'h0	dac_path_sreset	dac path software reset, high active
[3]	rw	1'h0	adc_path_flush	adc path fifo flush, high active
[2]	rw	1'h0	dac_path_flush	dac path fifo flush, high active
[1]	rw	1'h0	sreset	audprc software reset, high active
[0]	rw	1'h0	enable	audprc enable
0x08			**stb**	
[31:16]	rw	16'h1	adc_div	adc strobe divider
[15:0]	rw	16'h1	dac_div	dac strobe divider
0x0C			**irq**	
[31:26]			RSVD	
[25]	rw	1'h0	tx_out1_fifo_uf_mask	tx_out channel 1 fifo underflow mask, 0: mask the interrupt
[24]	rw	1'h0	tx_out0_fifo_uf_mask	tx_out channel 0 fifo underflow mask, 0: mask the interrupt
[23]	rw	1'h0	rx_in_fifo_of_mask	rx input fifo overflow mask, 0: mask the interrupt
[22]	rw	1'h0	tx_out_fifo_uf_mask	tx output fifo underflow mask, 0: mask the interrupt
[21]	rw	1'h0	rx1_fifo_uf_mask	rx channel 1 fifo underflow mask, 0: mask the interrupt
[20]	rw	1'h0	rx0_fifo_uf_mask	rx channel 0 fifo underflow mask, 0: mask the interrupt
[19]	rw	1'h0	tx3_fifo_of_mask	tx channel 3 fifo overflow mask, 0: mask the interrupt
[18]	rw	1'h0	tx2_fifo_of_mask	tx channel 2 fifo overflow mask, 0: mask the interrupt
[17]	rw	1'h0	tx1_fifo_of_mask	tx channel 1 fifo overflow mask, 0: mask the interrupt
[16]	rw	1'h0	tx0_fifo_of_mask	tx channel 0 fifo overflow mask, 0: mask the interrupt
[15:10]			RSVD	
[9]	rw1c	1'h0	tx_out1_fifo_uf	tx_out channel 1 fifo underflow, write 1 to clear
[8]	rw1c	1'h0	tx_out0_fifo_uf	tx_out channel 0 fifo underflow, write 1 to clear
[7]	rw1c	1'h0	rx_in_fifo_of	rx input fifo overflow, write 1 to clear
[6]	rw1c	1'h0	tx_out_fifo_uf	tx output fifo underflow, write 1 to clear
[5]	rw1c	1'h0	rx1_fifo_uf	rx channel 1 fifo underflow, write 1 to clear
[4]	rw1c	1'h0	rx0_fifo_uf	rx channel 0 fifo underflow, write 1 to clear
[3]	rw1c	1'h0	tx3_fifo_of	tx channel 3 fifo overflow, write 1 to clear
[2]	rw1c	1'h0	tx2_fifo_of	tx channel 2 fifo overflow, write 1 to clear
[1]	rw1c	1'h0	tx1_fifo_of	tx channel 1 fifo overflow, write 1 to clear
[0]	rw1c	1'h0	tx0_fifo_of	tx channel 0 fifo overflow, write 1 to clear
0x10			**tx_ch0_cfg**	
[31:8]			RSVD	
[7:4]	r	4'h0	fifo_cnt	tx fifo counter

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表 11-4: Audprc 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[3]	rw	1'h0	dma_msk	1: mask the dma request for tx ch0
[2]	rw	1'h0	mode	tx mode 1'h0: mono mode 1'h1: stereo mode This bit is only used for 16-bit mode, in 24-bit mode, channel can only be set in mono mode. In 16-bit stereo mode, tx channel 1 is not working, both left and right audio data comes from channel 0.
[1]	rw	1'h0	format	tx format 0: 16-bit mode 1: 24-bit mode
[0]	rw	1'h0	enable	tx channel 0 enable
0x14			**tx_ch0_entry**	
[31:0]	rw	32'h0	data	tx channel 0 data entry
0x18			**tx_ch1_cfg**	
[31:8]			RSVD	
[7:4]	r	4'h0	fifo_cnt	tx fifo counter
[3]	rw	1'h0	dma_msk	1: mask the dma request for tx ch1
[2]			RSVD	
[1]	rw	1'h0	format	tx format 0: 16-bit mode 1: 24-bit mode
[0]	rw	1'h0	enable	tx channel 0 enable
0x1C			**tx_ch1_entry**	
[31:0]	rw	32'h0	data	tx channel 1 data entry
0x20			**tx_ch2_cfg**	
[31:8]			RSVD	
[7:4]	r	4'h0	fifo_cnt	tx fifo counter
[3]	rw	1'h0	dma_msk	1: mask the dma request for tx ch2
[2]	rw	1'h0	mode	tx mode 1'h0: mono mode 1'h1: stereo mode This bit is only used for 16-bit mode, in 24-bit mode, channel can only be set in mono mode. In 16-bit stereo mode, tx channel 3 is not working, both left and right audio data comes from channel 2.
[1]	rw	1'h0	format	tx format 0: 16-bit mode 1: 24-bit mode
[0]	rw	1'h0	enable	tx channel 0 enable
0x24			**tx_ch2_entry**	
[31:0]	rw	32'h0	data	tx channel 2 data entry
0x28			**tx_ch3_cfg**	
[31:8]			RSVD	
[7:4]	r	4'h0	fifo_cnt	tx fifo counter
[3]	rw	1'h0	dma_msk	1: mask the dma request for tx ch3
[2]			RSVD	

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表 11-4: Audprc 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[1]	rw	1'h0	format	tx format 0: 16-bit mode 1: 24-bit mode
[0]	rw	1'h0	enable	tx channel 0 enable
0x2C			**tx_ch3_entry**	
[31:0]	rw	32'h0	data	tx channel 3 data entry
0x30			**rx_ch0_cfg**	
[31:8]			RSVD	
[7:4]	r	4'h0	fifo_cnt	rx fifo counter
[3]	rw	1'h0	dma_msk	1: mask the dma request for rx ch0
[2]	rw	1'h0	mode	rx mode 1'h0: mono mode 1'h1: stereo mode This bit is only used for 16-bit mode, in 24-bit mode, channel can only be set in mono mode. In 16-bit stereo mode, rx channel 1 is not working, both left and right audio data comes from channel 0.
[1]	rw	1'h0	format	rx format 0: 16-bit mode 1: 24-bit mode
[0]	rw	1'h0	enable	rx channel 0 enable
0x34			**rx_ch0_entry**	
[31:0]	r	32'h0	data	rx channel 0 data entry
0x38			**rx_ch1_cfg**	
[31:8]			RSVD	
[7:4]	r	4'h0	fifo_cnt	rx fifo counter
[3]	rw	1'h0	dma_msk	1: mask the dma request for rx ch1
[2]			RSVD	
[1]	rw	1'h0	format	rx format 0: 16-bit mode 1: 24-bit mode
[0]	rw	1'h0	enable	rx channel 1 enable
0x3C			**rx_ch1_entry**	
[31:0]	r	32'h0	data	rx channel 1 data entry
0x40			**tx_out_ch0_cfg**	
[31:8]			RSVD	
[7:4]	r	4'h0	fifo_cnt	tx out fifo counter
[3]	rw	1'h0	dma_msk	1: mask the dma request for tx out ch0
[2]	rw	1'h0	mode	tx out mode 1'h0: mono mode 1'h1: stereo mode This bit is only used for 16-bit mode, in 24-bit mode, channel can only be set in mono mode. In 16-bit stereo mode, rx channel 1 is not working, both left and right audio data comes from channel 0.
[1]	rw	1'h0	format	tx out format 0: 16-bit mode 1: 24-bit mode
[0]	rw	1'h0	enable	tx out channel 0 enable

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表 11-4: Audprc 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
0x44			**tx_out_ch0_entry**	
[31:0]	r	32'h0	data	tx out channel 0 data entry
0x48			**tx_out_ch1_cfg**	
[31:8]			RSVD	
[7:4]	r	4'h0	fifo_cnt	tx out fifo counter
[3]	rw	1'h0	dma_msk	1: mask the dma request for tx out ch1
[2]			RSVD	
[1]	rw	1'h0	format	tx out format 0: 16-bit mode 1: 24-bit mode
[0]	rw	1'h0	enable	tx out channel 1 enable
0x4C			**tx_out_ch1_entry**	
[31:0]	r	32'h0	data	tx out channel 1 data entry
0x50			**dac_path_cfg0**	
[31:26]			RSVD	
[25:24]	rw	2'h0	dst_sel	dac path destination select 2'h0: select audio codec 2'h1: select external interface 2'h2: select apb interface 2'h3: reserved
[23:21]	rw	3'h3	mixrsrc1	dac mixer right channel input source0 select 3'h0:tx ch0 3'h1:tx ch1 3'h2:tx ch2 3'h3:tx ch3 3'h4:mute other: mute
[20:18]	rw	3'h2	mixrsrc0	dac mixer right channel input source0 select 3'h0:tx ch0 3'h1:tx ch1 3'h2:tx ch2 3'h3:tx ch3 3'h4:mute other: mute
[17:15]	rw	3'h1	mixlsrc1	dac mixer left channel input source1 select 3'h0:tx ch0 3'h1:tx ch1 3'h2:tx ch2 3'h3:tx ch3 3'h4:mute other: mute
[14:12]	rw	3'h0	mixlsrc0	dac mixer left channel input source0 select 3'h0:tx ch0 3'h1:tx ch1 3'h2:tx ch2 3'h3:tx ch3 3'h4:mute other: mute

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表 11-4: Audprc 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[11:6]	rw	6'h3f	vol_r	volume control from -18~13dB, step is 0.5dB 6'h0: -18dB 6'h1: -17.5dB ..... 6'h3e: 13dB 6'h3f: mute
[5:0]	rw	6'h3f	vol_l	volume control from -18~13dB, step is 0.5dB 6'h0: -18dB 6'h1: -17.5dB ..... 6'h3e: 13dB 6'h3f: mute
0x54			**dac_path_cfg1**	
[31:30]	rw	2'h0	src_ch_clr	clear src channal internal data
[29:28]	r	2'h0	src_ch_clr_done	src channel internal data clear done
[27]	rw	1'h0	src_hbf3_mode	3rd stage hbf mode: 0: upsampling 1: downsampling
[26]	rw	1'h0	src_hbf3_en	3rd stage hbf enable
[25]	rw	1'h0	src_hbf2_mode	2nd stage hbf mode: 0: upsampling 1: downsampling
[24]	rw	1'h0	src_hbf2_en	2nd stage hbf enable
[23]	rw	1'h0	src_hbf1_mode	1st stage hbf mode: 0: upsampling 1: downsampling
[22]	rw	1'h0	src_hbf1_en	1st stage hbf enable
[21:20]	rw	2'h0	src_ch_en	source rate converter channel enable
[19]	rw	1'h0	eq_clr	equalizer clear request
[18]	r	1'h0	eq_clr_done	equalizer clear done flag
[17:14]	rw	4'ha	eq_stage	set equalizer stage, max is 10.
[13:12]	rw	2'h0	eq_ch_en	equalizer channel enable 2'b11: enable both channel 2'b10: enable right chanel only 2'b01: enable left channel only 2'b00: bypass equalizer
[11:9]	rw	3'h3	muxrsrc1	dac mux right channel input source0 select 3'h0:tx ch0 3'h1:tx ch1 3'h2:rx ch0 3'h3:rx ch1 3'h4:mute other: mute

续表下页...

表 11-4: Audprc 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[8:6]	rw	3'h2	muxrsrc0	dac mux right channel input source0 select 3'h0:tx ch0 3'h1:tx ch1 3'h2:rx ch0 3'h3:rx ch1 3'h4:mute other: mute
[5:3]	rw	3'h1	muxlsrc1	dac mux left channel input source1 select 3'h0:tx ch0 3'h1:tx ch1 3'h2:rx ch0 3'h3:rx ch1 3'h4:mute other: mute
[2:0]	rw	3'h0	muxlsrc0	dac mux left channel input source0 select 3'h0:tx ch0 3'h1:tx ch1 3'h2:rx ch0 3'h3:rx ch1 3'h4:mute other: mute
0x58			**dac_path_cfg2**	
[31]	rw	1'h0	src_sinc_en	sinc filter enable
[30:0]	rw	31'h0	sinc_ratio	sinc filter ratio, s31.30 format. Range from 0~2
0x5C			**adc_path_cfg0**	
[31:15]			RSVD	
[14]	rw	1'h0	rx2tx_loopback	rx to tx loopback enable
[13]	rw	1'h0	data_swap	swap adc path left and right channel data
[12]	rw	1'h0	src_sel	adc path source select 1'h0: select audio codec 1'h1: select external interface
[11:6]	rw	6'h3f	vol_r	volume control from -18~13dB, step is 0.5dB 6'h0: -18dB 6'h1: -17.5dB ..... 6'h3e: 13dB 6'h3f: mute
[5:0]	rw	6'h3f	vol_l	volume control from -18~13dB, step is 0.5dB 6'h0: -18dB 6'h1: -17.5dB ..... 6'h3e: 13dB 6'h3f: mute
0x70			**dac_eq_cfg0**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0x74			**dac_eq_cfg1**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	

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表 11-4: Audprc 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
0x78			**dac_eq_cfg2**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0x7C			**dac_eq_cfg3**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0x80			**dac_eq_cfg4**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0x84			**dac_eq_cfg5**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0x88			**dac_eq_cfg6**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0x8C			**dac_eq_cfg7**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0x90			**dac_eq_cfg8**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0x94			**dac_eq_cfg9**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0x98			**dac_eq_cfg10**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0x9C			**dac_eq_cfg11**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0xA0			**dac_eq_cfg12**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0xA4			**dac_eq_cfg13**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0xA8			**dac_eq_cfg14**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0xAC			**dac_eq_cfg15**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0xB0			**dac_eq_cfg16**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0xB4			**dac_eq_cfg17**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	

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表 11-4: Audprc 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
0xB8			**dac_eq_cfg18**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0xBC			**dac_eq_cfg19**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0xC0			**dac_eq_cfg20**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0xC4			**dac_eq_cfg21**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0xC8			**dac_eq_cfg22**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0xCC			**dac_eq_cfg23**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0xD0			**dac_eq_cfg24**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0xD4			**dac_eq_cfg25**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0xD8			**dac_eq_cfg26**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0xDC			**dac_eq_cfg27**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0xE0			**dac_eq_cfg28**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0xE4			**dac_eq_cfg29**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0xE8			**dac_eq_cfg30**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0xEC			**dac_eq_cfg31**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0xF0			**dac_eq_cfg32**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0xF4			**dac_eq_cfg33**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	

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表 11-4: Audprc 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
0xF8			**dac_eq_cfg34**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0xFC			**dac_eq_cfg35**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0x100			**dac_eq_cfg36**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0x104			**dac_eq_cfg37**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0x108			**dac_eq_cfg38**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0x10C			**dac_eq_cfg39**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0x110			**dac_eq_cfg40**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0x114			**dac_eq_cfg41**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0x118			**dac_eq_cfg42**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0x11C			**dac_eq_cfg43**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0x120			**dac_eq_cfg44**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0x124			**dac_eq_cfg45**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0x128			**dac_eq_cfg46**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0x12C			**dac_eq_cfg47**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0x130			**dac_eq_cfg48**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0x134			**dac_eq_cfg49**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	

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表 11-4: Audprc 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
0x138			**RESERVED_IN**	
[31:24]			RSVD	
[23:16]	rw	8'hf	CTRL_2	reserved control 2
[15:8]	rw	8'hf	CTRL_1	reserved control 1
[7:0]	rw	8'hf	CTRL_0	reserved control 0
0x13C			**RESERVED_OUT**	
[31:8]			RSVD	
[7:0]	r	8'h0	STAT	reserved status

12 加速器

12.1 神经网络加速器

12.1.1 神经网络矩阵卷积加速器（NNACC）

矩阵卷积加速器旨在满足机器学习计算中对底层矩阵算力的需求，可以广泛适用于各种神经网络框架。加速器访存接口丰富，提供灵活的数据地址配置。支持最大 255×255 的输入矩阵和最大 128 的输入输出通道数。支持 8bit 整数型运算，可以满足大部分边缘端 AI 计算要求，比如语音指令识别、心率、计步、心电图等传感器的计算等场景。

12.1.2 神经网络协处理器（NN Co-Processor）

神经网络协处理器，通过协处理器接口挂在 hpcpu/lpcpu 上。软件通过专门的协处理器指令调用该处理器。协处理器特性为：

- 数据总线位宽为 64Bit
- 支持 8Bit 位宽的 MAC 运算
- 支持单指令 4 次独立 MAC 运算

12.2 FFT 加速器

FFT 运算对算力要求很高，用 FFT 加速器可以减轻 CPU 负载，提升系统性能。HPSYS 中集成有 FFT 加速器，可以在更多场景下满足 FFT 算力要求。

FFT 加速器主要特性如下：

- 支持最大 512 点最小 16 点 FFT
- 支持 24 点、16 点、8 点定点有符号数输入输出，输入输出位宽独立配置
- 支持实数 FFT 运算
- 支持 IFFFT
- 支持加窗 FFT/IFFT
- 支持 DCT/IDCT

12.3 Cordic 协处理器

Cordic 协处理器用于计算三角函数和双曲函数及其推演出的一些算术运算。在 HPSYS/LPSYS 中各集成了一个 Cordic 协处理器。

Cordic 协处理器特性如下：

- 支持 ARM coprocessor 协处理器指令
- 支持 ARM Custom Datapath Extention 指令（只有 HPSYS）

- 支持三角函数类运算：cos、sin、ang、mod、atan、rot
- 支持双曲函数类运算 cosh、sinh、atanh、angh、modh、mul、div、ln、exp、sqrt
- 支持 32 位定点输入输出

12.4 CRC

芯片共有 2 个 CRC，其中 CRC1 位于 HPSYS，CRC2 位于 LPSYS。

12.4.1 简介

CRC(Cyclic Redundancy Check) 可进行特定位宽，任意生成多项式，任意初始值的 CRC 计算。数据可以通过 CPU 或 DMA 输入，最小输入单元为单字节，没有最长字节数限制。单 HCLK 周期即能够完成单字节输入的计算。数据输入全部完成后即时得到校验结果。支持输入数据高低位倒转和输出数据高低位倒转。支持不同有效位宽的输入数据。

12.4.2 主要特性

- 7/8/16/32 比特 CRC 计算
- 任意自定义多项式
- 任意初始值
- 输入数据支持单字节/双字节/三字节/四字节有效位宽
- 输入数据支持字节/双字节/四字节高低位比特倒转
- 输出数据支持高低位比特倒转
- 计算速度为每 HCLK 周期 1 字节

12.4.3 CRC 配置方法

启动 CRC 计算前，需要预先配置相应寄存器，包括多项式宽度，有效数据位宽，输入输出倒转模式，多项式和初始值等。主流的 CRC 格式配置方法见下表。

表 12-1: CRC 配置方法

CRC 算法	多项式公式	POLYSIZE	POL	INIT	REV_IN	REV_OUT	结果异或值
CRC-7/MMC	x^7+x^3+1	3	0x09	0x00	0	0	0x00
CRC-8	x^8+x^2+x+1	2	0x07	0x00	0	0	0x00
CRC-8/ITU	x^8+x^2+x+1	2	0x07	0x00	0	0	0x55
CRC-8/ROHC	x^8+x^2+x+1	2	0x07	0xFF	1	1	0x00
CRC-8/MAXIM	$x^8+x^5+x^4+1$	2	0x31	0x00	1	1	0x00
CRC-16/IBM	$x^{16}+x^5+x^2+1$	1	0x8005	0x0000	1	1	0x0000
CRC-16/MAXIM	$x^{16}+x^5+x^2+1$	1	0x8005	0x0000	1	1	0xFFFF
CRC-16/USB	$x^{16}+x^5+x^2+1$	1	0x8005	0xFFFF	1	1	0xFFFF
CRC-16/ MODBUS	$x^{16}+x^5+x^2+1$	1	0x8005	0xFFFF	1	1	0x0000
CRC-16/CCITT	$x^{16}+x^{12}+x^5+1$	1	0x1021	0x0000	1	1	0x0000
CRC-16/ CCITT-FALSE	$x^{16}+x^{12}+x^5+1$	1	0x1021	0xFFFF	0	0	0x0000
CRC-16/x5	$x^{16}+x^{12}+x^5+1$	1	0x1021	0xFFFF	1	1	0xFFFF

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表 12-1: CRC 配置方法（续）

CRC 算法	多项式公式	POLYSIZE	POL	INIT	REV_IN	REV_OUT	结果异或值
CRC-16/ XMODEM	$x^{16}+x^{12}+x^5+1$	1	0x1021	0x0000	0	0	0x0000
CRC-16/DNP	$x^{16}+x^{13}+x^{12}+x^{11}+x^{10}+x^8+x^6+x^5+x^2+1$	1	0x3D65	0x0000	1	1	0xFFFF
CRC-32	$x^{32}+x^{26}+x^{23}+x^{22}+x^{16}+x^{12}+x^{11}+x^{10}+x^8+x^7+x^5+x^4+x^2+x+1$	0	0x04C11DB7	0xFFFFFFFF	1	1	0xFFFFFFFF
CRC-32/ MPEG-2	$x^{32}+x^{26}+x^{23}+x^{22}+x^{16}+x^{12}+x^{11}+x^{10}+x^8+x^7+x^5+x^4+x^2+x+1$	0	0x04C11DB7	0xFFFFFFFF	0	0	0x00000000

CRC 模块不进行结果异或运算，需要由软件读出结果后进行后处理。

12.4.4 数据格式

CRC 计算的基本数据单元为字节。向 DR 寄存器写入的数据固定为 4 字节，该数据中哪些字节参与运算由 CR_DATASIZE 指定。下表中灰色格子参与运算。

表 12-2: 参与运算的数据

CR_DATASIZE	DR			
0	BYTE3	BYTE2	BYTE1	BYTE0
1	BYTE3	BYTE2	BYTE1	BYTE0
2	BYTE3	BYTE2	BYTE1	BYTE0
3	BYTE3	BYTE2	BYTE1	BYTE0

可以单独指定每一笔数据参与运算的字节，但应注意改变 CR_DATASIZE 必须在 SR_DONE 为 1 时，否则可能影响当前数据的计算结果。

运算顺序由 BYTE0,BYTE1,BYTE2,BYTE3 依次进行。计算每个字节时，默认按照从最高比特到最低比特的次序进行。如果配置了输入倒转模式，则按照倒转后从最高比特到最低比特的次序进行。下表为配置的示例，可根据内存中的数据格式灵活调整输入格式。

表 12-3: 运算顺序

DATASIZE	REV_IN	DR	倒转后输入	第一拍计算字节	第二拍计算字节	第三拍计算字节	第四拍计算字节
0	0	0x12345678	/	0x78	/	/	/
1	0	0x12345678	/	0x78	0x56	/	/
2	0	0x12345678	/	0x78	0x56	0x34	/
3	0	0x12345678	/	0x78	0x56	0x34	0x12
3	1	0x12345678	0x482C6A1E	0x1E	0x6A	0x2C	0x48
3	2	0x12345678	0x2C481E6A	0x6A	0x1E	0x48	0x2C
3	3	0x12345678	0x1E6A2C48	0x48	0x2C	0x6A	0x1E

12.4.5 计算速率

CRC 每个 HCLK 周期完成一个字节的计算。数据连续输入时，计算花费的时间约为字节数 ×HCLK 周期。

12.4.6 CRC 配置流程

1. 配置 CRC 格式，依需求设置 POL，INIT，CR_POLYSIZE，CR_REV_IN，CR_REV_OUT，CR_DATASIZE。
2. CR_RESET 置 1 初始化 CRC。
3. 由 CPU 或 DMA 向 DR 寄存器连续搬运所需数据。
4. 如果还剩余的数据字节数与 CR_DATASIZE 不匹配，则需首先查询 SR_DONE，为 1 时改变 CR_DATASIZE，并将剩余数据写入 DR 寄存器。
5. 读 DR 寄存器获取计算结果，并根据需求进行软件异或运算，得到最终 CRC 值。

12.4.7 CRC 寄存器

表 12-4: CRC 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00			**DR**	Data register
[31:0]	rw	32'hffffffff	DR	Data register bits. This register is used to write new data to the CRC calculator. It holds the previous CRC calculation result when it is read. If the data size is less than 32 bits, the least significant bits are used to write/read the correct value.
0x04			**SR**	Status register
[31:2]			RSVD	
[1]	r	1'h0	overflow	Overflow when new data arrive while last calculation not done yet
[0]	r	1'h0	done	Done flag. When DR written, done flag will be cleared automatically. The flag will assert after CRC operation of current DR finished.
0x08			**CR**	Control register
[31:8]			RSVD	
[7]	rw	1'h0	REV_OUT	Reverse output data This bit controls the reversal of the bit order of the output data. 0: Bit order not affected 1: Bit-reversed output format
[6:5]	rw	2'h0	REV_IN	Reverse input data These bits control the reversal of the bit order of the input data 00: Bit order not affected 01: Bit reversal done by byte 10: Bit reversal done by half-word 11: Bit reversal done by word
[4:3]	rw	2'h0	POLYSIZE	Polynomial size These bits control the size of the polynomial. 00: 32 bit polynomial 01: 16 bit polynomial 10: 8 bit polynomial 11: 7 bit polynomial

续表下页...

表 12-4: CRC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[2:1]	rw	2'h3	DATASIZE	Valid input data size These bits control the valid size of the input data. 00: lower 8-bit 01: lower 16-bit 10: lower 24-bit 11: all 32-bit
[0]	w	1'h0	RESET	This bit is set by software to reset the CRC calculation unit and set the data register to the value stored in the CRC_INIT register. This bit can only be set, it is automatically cleared by hardware
0x10			**INIT**	Initial CRC value
[31:0]	rw	32'hffffffff	INIT	Programmable initial CRC value
0x14			**POL**	CRC polynomial
[31:0]	rw	32'h04c11db7	POL	Programmable polynomial This register is used to write the coefficients of the polynomial to be used for CRC calculation. If the polynomial size is less than 32 bits, the least significant bits have to be used to program the correct value.

12.5 FACC

芯片有 1 个 FACC，位于 HPSYS。

12.5.1 简介

FACC 模块是 filter 计算模块，该模块通过 AHB 总线读入待处理数据，滤波后的数据通过 AHB 总线送出。

12.5.2 主要特性

- 支持 8/16bit 数据位宽
- 支持 FIR/IIR 滤波算法
- 支持 FIR 模式下普通、卷积、对称、反对称四三种算法
- 支持 FIR 模式最大阶数 32（16bit），64（8bit）
- 支持 IIR 模式最大阶数 16/16（16bit）、32/32（8bit）
- 支持数据并行处理
- 通过 AHB 总线输入/输出数据地址可配
- 支持数据分块处理
- 支持几组不同数据交叉处理

12.5.3 FIR 普通模式

FACC 模块支持的普通 FIR 算法公式如下：

$$y[n] = \sum_{k=0}^{N} b[k]x[n-k]$$

x 为输入的待处理数组，y 为输出的滤波后的数组，b 为每阶计算的参数。x 数组由 ahb 总线从源地址读回，y 数组由 ahb 总线送到目的地址。b 数组直接由软件配置到模块内部 fifo，fifo 位宽为 32bit。

x 数组的数据按 $x[0]$、$x[1]$、$x[2]$..... 的顺序从低位到高位的顺序排放。y、b 数组同理。

12.5.4 FIR 普通模式

FACC 模块支持的 FIR 卷积算法公式如下：

$$y_n = \begin{cases} \sum_{m=0}^{n} h_m x_{n-m}, & \text{if } 0 \le n < M, \\ \sum_{m=0}^{M} h_m x_{n-m}, & \text{if } M \le n \le L-1, \\ \sum_{m=n-L+1}^{M} h_m x_{n-m}, & \text{if } L-1 < n \le L-1+M, \end{cases}$$

公式中的 h 数组对应 FACC 模块的 b 数组。卷积模式下，输出数据 y 数组的个数大于输入数据 x 数组的个数。

12.5.5 FIR 对称模式

FACC 模块支持的 FIR 对称模式公式与普通 FIR 模式的公式相同，区别在于 b 数据的结构不同，该模式下 b 数据的数据按对称的方式分布。根据 b 数据的结构不同对称模式又分为两种：奇对称和偶对称。

假如 b 数组有 n 个数据，在偶对称模式下，b 数组对称后的新数组为：

$$b[0]b[1]b[2].....b[n-2]b[n-1]b[n-1]b[n-2].....b[1]b[0]$$

偶对称后的数组阶数为 $2n$。在奇对称的模式下，b 数组对称后的新数组为：

$$b[0]b[1]b[2].....b[n-2]b[n-1]b[n-2].....b[1]b[0]$$

奇对称后的数组阶数为 2n-1。

该模式下配置到 b 数组 fifo 的数据，不需要把对称数据全部写入，仅写入对称前的原始数据 $b[0]b[1].....b[n-1]$ 即可。阶数参数也按对称前的阶数配置。

12.5.6 FIR 反对称模式

FACC 模块支持的 FIR 反对称模式与对称模式的区别在于，对称模式是将对称后的计算数据累加，反对称模式是将对称后的计算数据累减。b 数组的对称结构同 FIR 对称模式，即分奇对称和偶对称。

12.5.7 IIR 模式

FACC 模块支持的 IIR 算法公式如下：

$$y[n] = \sum_{k=0}^{N} b[k]x[n-k] + \sum_{j=1}^{M} a[j]y[n-j]$$

相比 FIR 算法增加了 a 数据，在参数配置时需要对 b 数组和 a 数组分别进行配置。$a[0]$ 数据不使用，所以 $a[0]$ 数据不需要写入 a 数组的 fifo 内。

12.5.8 增益调整

滤波计算后的结果，可通过寄存器配置调整增益大小。

12.5.9 数据分块

FACC 模块支持对输入的数据分块处理，即将输入数据按一定规则进行分块，处理完一块数据后再启动下一块数据的处理。每块数据启动时都需要重新配置源地址、目的地址、数据块长度等参数信息。如果是 FIR 卷积模式，在启动最后一个数据块的时候，还需要配置 last_sel 标志位，以完成最后的卷积运算部分。

数据分块规则：由于 FACC 内部是 4 线并行处理，所以除最后一个数据块外，其他数据块的数据长度需是 4 的整数倍。数据长度是按待处理的数据个数定义，如待处理数据是 8bit 数据，那么 8bit 算 1 个数据长度，16bit 为 2 个数据长度。如待处理数据是 16bit 数据，那么 16bit 算 1 个数据长度，32bit 为 2 个数据长度。

12.5.10 数据缓存模式

FACC 模块支持数据缓存模式，该模式下可支持多组数据交叉处理。以两组数据为例，处理完第一组数据的一块数据后，可接着处理第二组数据的一块数据，然后又处理第一组数据的另一块数据，如此往复。更多组的数据原理相同。数据缓存模式下，每组数据需要一个外部缓存 buffer，将计算的中间结果缓存出去，第二次启动的时候再将缓存数据读回，所以需要预留数据缓存空间，配置数据缓存地址。

每组数据缓存空间的大小如下:

模式	空间大小 (byte)
FIR	68
FIR 对称	132
FIR 卷积	68
IIR	100

数据缓存模式需要配置 buf_sel 为 1，当 buf_sel=1 的时候，模块会先从缓存地址读入缓存数据，因此启动第一块数据的时候需将缓存空间数据清零。每块数据处理完成后，将需要缓存的数据送到缓存空间。

非数据缓存模式下，一组数据的中间不能插入另一组数据，需一次性计算完一组数据后方可启动其他组数据的计算。

12.5.11 非缓存模式下的配置流程

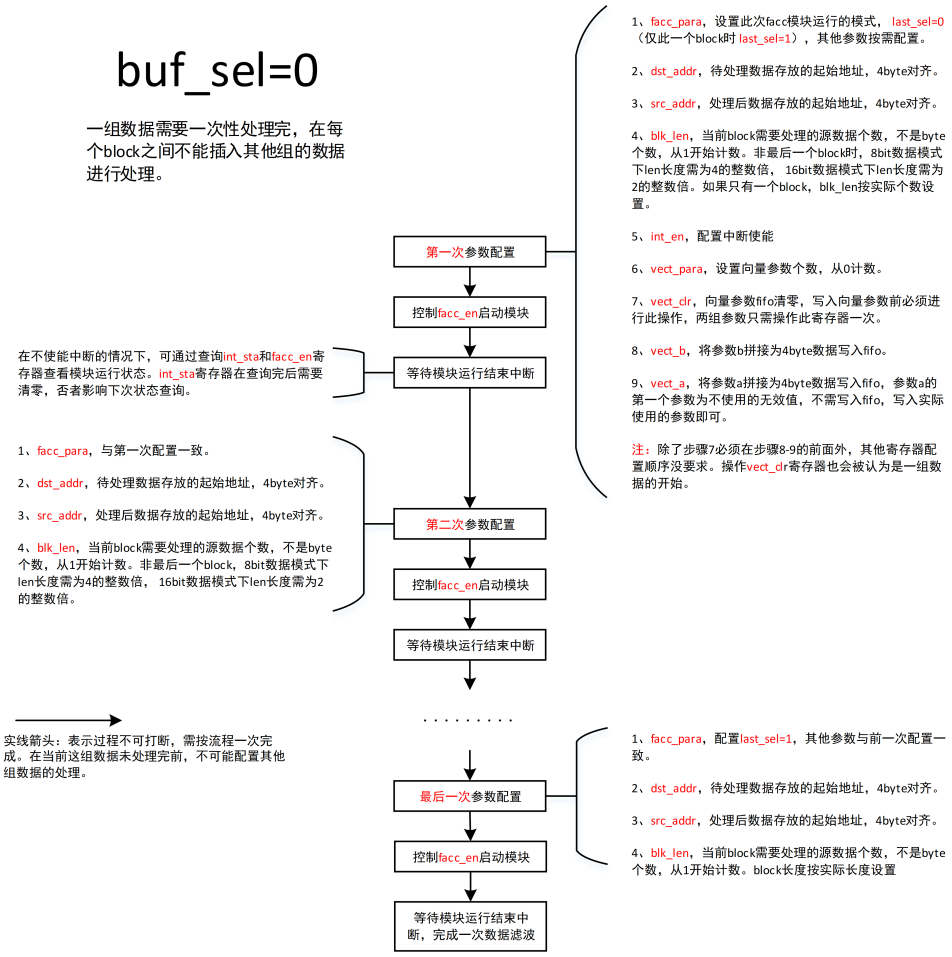

图 12-1: 非缓存模式下的配置流程图

12.5.12 缓存模式下的配置流程

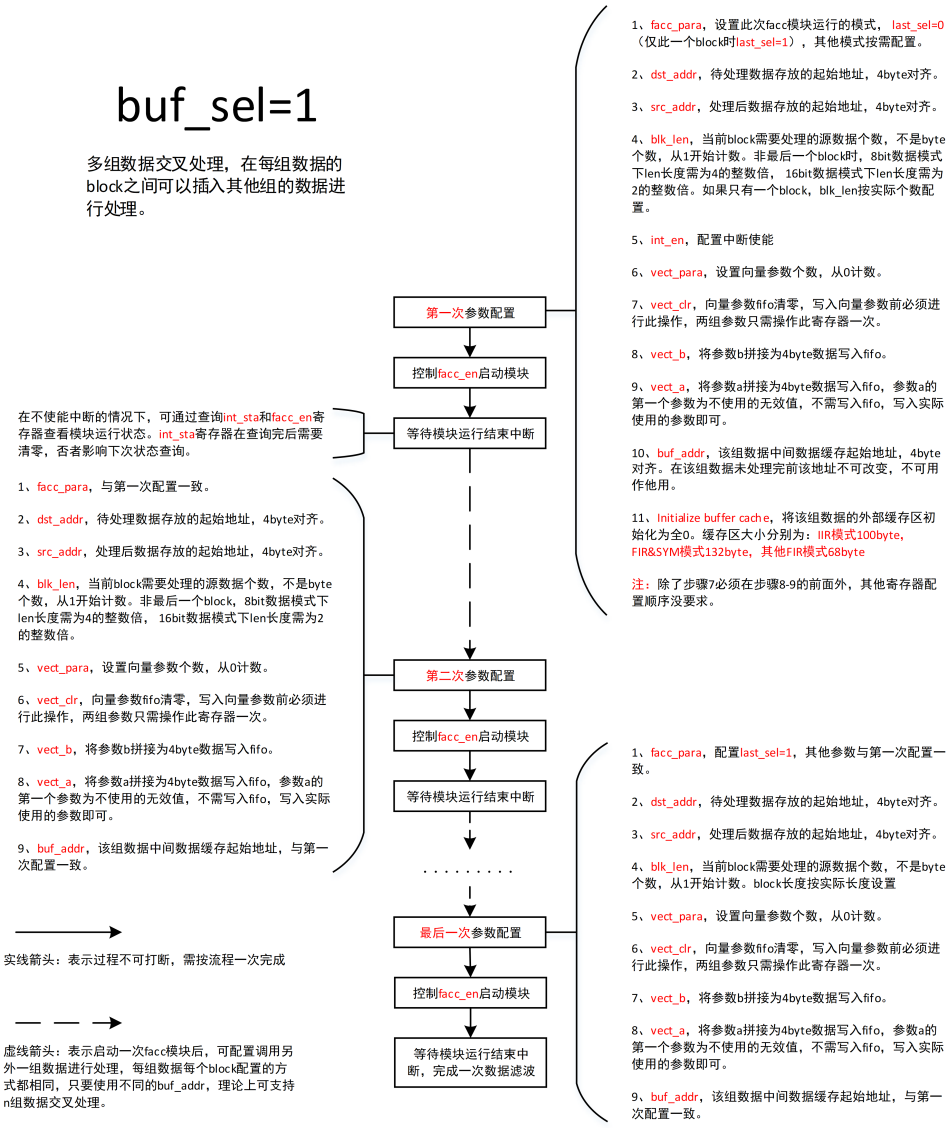

图 12-2: 缓存模式下的配置流程图

12.5.13 FACC 寄存器

表 12-5: FACC 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x000			**FACC_EN**	facc enable ctrl
[31:1]			RSVD	
[0]	rw1s	1'h0	facc_en	1:enable 0:stop
0x004			**FACC_PARA**	FACC parameter
[31:13]			RSVD	
[12]	rw	1'h0	anti_sel	when sym_sel=1,this bit is effective 0:disable 1:enable
[11]	rw	1'h0	buf_sel	0:only support one group data 1:store intermediate data to external buffer,support cross processing of multiple groups data
[10]	rw	1'h0	even_sel	when sym_sel=1, this bit is effective 0: odd 1: even
[9]	rw	1'h0	conv_sel	0: filter 1: convolution(only support fir mod)
[8]	rw	1'h0	fp_sel	0: 16bit 1: 8bit
[7]	rw	1'h0	sym_sel	0:normal 1:symmetric(only support fir mod)
[6]	rw	1'h0	mod_sel	0: fir 1: iir
[5]	rw	1'h0	first_sel	unused
[4]	rw	1'h0	last_sel	when conv_sel=1 ,it is necrssary 0:other data block 1:last data block
[3:0]	rw	4'h0	gain	facc gain
0x008			**SRC_ADDR**	source address
[31:0]	rw	32'h0	src_addr	source address
0x00C			**DST_ADDR**	destination address
[31:0]	rw	32'h0	dst_addr	destination address
0x010			**BLK_LEN**	source block length
[31:0]	rw	32'h0	blk_len	block data byte(8bit) or word(16bit) number,count from 1. if not the last data block,the block length must be a multiple of 4.
0x014			**BUF_ADDR**	buffer address
[31:0]	rw	32'h0	buf_addr	intermediate data buffer address
0x018			**DATA_SEQ**	the sequence of the first data
[31:0]	rw	32'h0	data_seq	unused
0x01C			**VECT_PARA**	vector number
[31:16]			RSVD	
[15:8]	rw	8'h0	m	IIR vector a step , count from 0
[7:0]	rw	8'h0	p	FIR/IIR vector b step , count from 0
0x020			**VECT_B**	vector b fifo
[31:0]	w	32'h0	vect_b	vector b
0x024			**VECT_A**	vector a fifo

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表 12-5: FACC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:0]	w	32'h0	vect_a	vector a
0x028			**VECT_CLR**	vector fifo clr
[31:1]			RSVD	
[0]	rw1s	1'h0	vect_clr	vector fifo clr
0x02C			**INT_EN**	interrupt enable
[31:1]			RSVD	
[0]	rw	1'h0	int_en	interrupt enable
0x030			**INT_STA**	interrupt state
[31:1]			RSVD	
[0]	rw1c	1'h0	int_sta	interrupt state
0x034			**DBG_DATA**	debug data
[31:0]	r	32'h0	debug_data	13:inbuf_empty 12:inmem_full 11:inmem_empty 10:iir_en 9:iir_on 8:iir_ok 7:fir_end 6:conv_act 5:fir_on 4:blk_on 3~0 :ahb_state

13 安全

13.1 AES

AES 位于 HPSYS。

13.1.1 简介

SF32LB56x 的 AES_ACC 模块主要针对安全领域的专用算法进行加解密的运算加速。对称加密算法包括 AES128、AES192、AES256 和 SM4。模式包括 ECB、CTR 和 CBC。散列算法包括 SHA1、SHA224、SHA256 和 SM3。启动后，AES_ACC 模块调用内部的 DMA 读入原始数据，根据算法将相应的结果通过内部 DMA 写入目标地址，或者存储在模块内部寄存器中。

13.1.2 AES 功能描述

13.1.2.1 对称加密算法

对称加密算法主要包括 AES 和 SM4，其中 AES 根据 Key 的长度不同又分为 AES128、AES192 和 AES256，SM4 则是国密的对称加密算法。强度上密码长度越长则强度越高，同时加解密花费的时间也会更长，SM4 算法花费的时间则是最长。

13.1.2.2 对称加密模式

对称加密模式主要包括 ECB、CTR 和 CBC。

ECB 模式：ECB 模式通过 KEY 直接对明文数据进行加解密，数据按 16byte 为一组，每次加解密都是对整个 16byte 进行操作。优点是每组数据之间相互独立，可以并行计算，支持数据按组的随机读写。缺点是不同组数据若明文相同，则密文也相同，容易被破解。

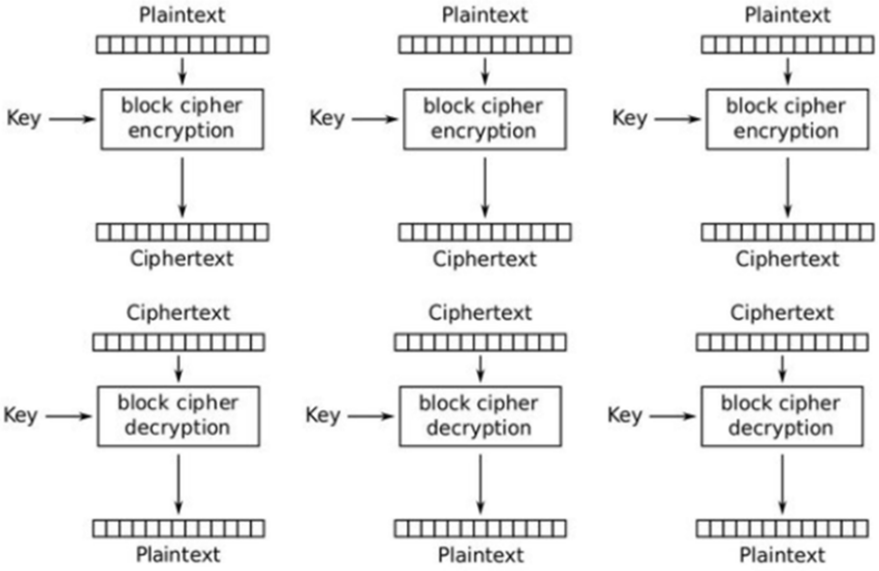

图 13-1: ECB 模式解密

CTR 模式：CTR 模式通过 KEY 对一个由 NONCE 和 COUNTER 组成的向量进行加密，然后用加密后的结果与明文数据进行异或，得到数据密文，实现加密操作。解密时用相同的向量加密后的结果与密文数据进行异或，得到明文数据，实现解密操作。实际使用中，NONCE 通常用常数表示，COUNTER 则会使用数据的地址，这样保证每组数据的向量不同，从而使加解密过程中使用的异或数据也不相同。在了解 CTR 使用的向量组成方式的情况下，该模式每组数据加解密互相独立，可以并行计算，这一点与 ECB 模式相同。同时该模式只有加密和异或运算，结构也相对简单。加解密时对向量的运算与数据无关，所以该模式常用于外部存储的数据进行加解密。

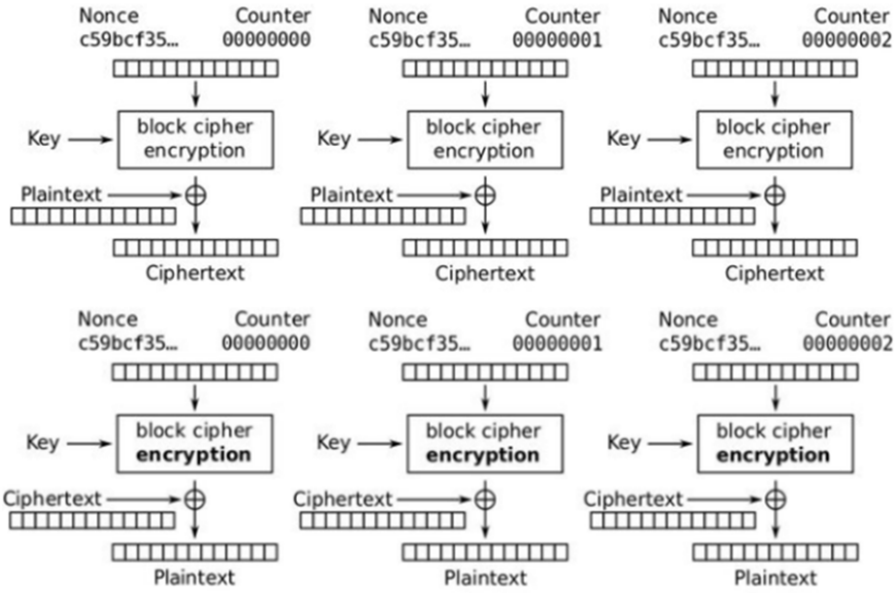

图 13-2: CTR 模式解密

CBC 模式：CBC 模式是将上一组数据的密文，作为初始化向量与当前组异或之后，用 KEY 进行加密生成密文。解密时用 KEY 将密文解密后与上一组的密文进行异或，生成明文。该模式既可以对数据进行加解密也可以将最

后一组密文数据作为数据的 MAC 值进行完整性校验，因为该模式加解密过程中，每组数据之间都相互关联，所以安全度更高，但无法做到并行计算，也无法对单独某组数据进行随机读写。

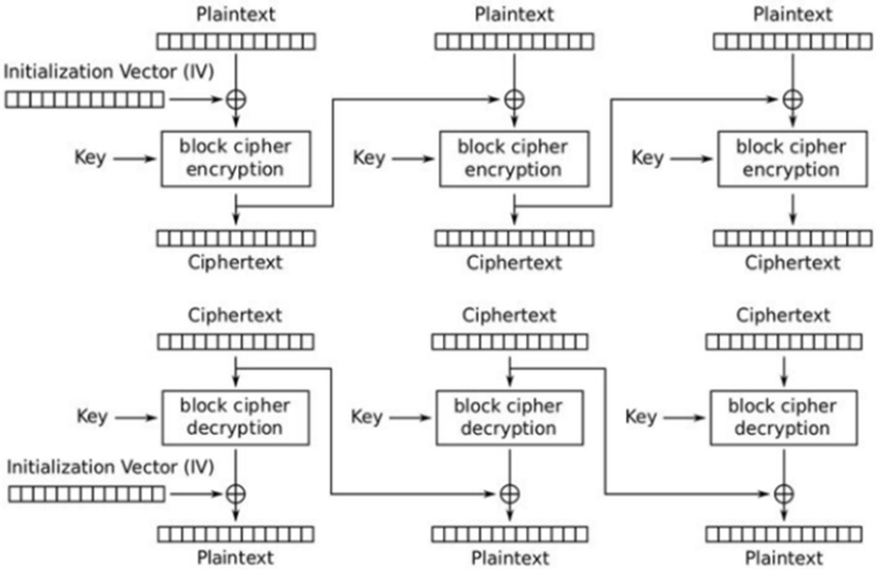

图 13-3: CBC 模式解密

13.1.2.3 对称加解密的多次调用

有时候需要对大量数据进行加解密的操作，但受限制与存储空间或者传输速率的影响，数据会被分为多批次进行处理，当需要多次调用对称加解密模块对一大段数据进行连续处理时就需要考虑到调用之间数据上下文的保存和维护。

ECB 模式：

ECB 模式对于每一组 16byte 数据进行单独的加解密操作的，对于单次加解密的数据，需要保证数据量为 16byte 的整数倍，多余的数据可以等到下一批数据准备好以后合并进行处理。

CTR 模式：

CTR 模式对于每一组 16byte 的数据均有对应的 NONCE 和 COUNTER 值，通常情况下，NONCE 为常数，COUNTER 为当前数据组的编号，数据组编号按每次加 1 递增。对于单次加解密的数据，上层软件调用时需要保证数据量为 16byte 的整数倍，同时根据数据量记录下 COUNTER 值，在下一次调用将累计的 COUNTER 值作为初始向量输入到对应的 IV 寄存器。多余的数据可以等到下一批数据准备好后合并进行处理。

CBC 模式：

CBC 模式的每组数据使用的初始向量均来自上一组数据的密文，对于单次加解密数据，上层软件调用时需要保证数据量为 16byte 的整数倍，同时需要记录下当前加解密操作最后一组数据的密文，在下一次操作时作为初始向量输入到对应的 IV 寄存器中。多余的数据则等到下一批数据准备好之后合并进行处理。

13.1.2.4 散列算法

散列算法包括 SHA1，SHA224，SHA256 和 SM3，不同算法的摘要长度不同。SHA1 摘要为 160bit，SHA224 为 224bit，SHA256 和 SM3 均为 256bit，碰撞性角度来说，摘要越长碰撞概率则会越低。

13.1.2.5 散列值计算的多次调用

有时候需要对大量数据进行散列值计算，但受限于存储空间或者传输速率的影响，数据会被分为多批次进行处理。当需要多次调用散列值计算模块对一大段数据进行处理时，需要注意以下几点。

第一，除最后一次以外，每一次处理的数据量必须为 4byte 的整数倍，单次处理多余的数据需保存，与下一批次的数据进行合并处理。

第二，对于所有散列算法，每一次计算前需要将上一次散列计算的中间结果 H0~H7 写入对应的寄存器，然后设置散列值计算模块使用外部 H0~H7 的初始值并且装载入模块。

第三，每次调用 HASH 时需要将上一次结束时的 HASH LEN RESULT 更新到当前 HASH LEN 寄存器，并且装载入模块。

第四，除最后一次调用以外，需要设置散列值计算模块不使用 padding。

13.1.3 AES 寄存器

表 13-1: AES 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00			**COMMAND**	
[31:5]			RSVD	
[4]	rw	1'h0	AUTO_GATE	auto clock gating
[3]	rw	1'h0	HASH_RESET	HASH_ACC soft reset, 1'h1: reset the HASH_ACC block
[2]	w1t	1'h0	HASH_START	write 1 to trigger the HASH_ACC block
[1]	rw	1'h0	AES_ACC_RESET	AES_ACC soft reset, 1'h1: reset the AES_ACC block
[0]	w1t	1'h0	START	write 1 to trigger the AES_ACC block
0x04			**STATUS**	
[31:3]			RSVD	
[2]	r	1'h0	HASH_BUSY	HASH_ACC block is busy
[1]	r	1'h0	FLASH_KEY_VALID	flash key valid indicator
[0]	r	1'h0	BUSY	AES_ACC block is busy
0x08			**IRQ**	
[31:22]			RSVD	
[21]	rw1c	1'h0	HASH_PAD_ERR_RAW_STAT	HASH_ACC padding error raw status
[20]	rw1c	1'h0	HASH_BUS_ERR_RAW_STAT	HASH_ACC bus error raw status
[19]	rw1c	1'h0	HASH_DONE_RAW_STAT	HASH_ACC done raw status
[18]	rw1c	1'h0	SETUP_ERR_RAW_STAT	AES_ACC setup error raw status
[17]	rw1c	1'h0	BUS_ERR_RAW_STAT	AES_ACC bus error raw status
[16]	rw1c	1'h0	DONE_RAW_STAT	AES_ACC done raw status
[15:6]			RSVD	
[5]	rw1c	1'h0	HASH_PAD_ERR_STAT	HASH_ACC padding error status
[4]	rw1c	1'h0	HASH_BUS_ERR_STAT	HASH_ACC bus error status
[3]	rw1c	1'h0	HASH_DONE_STAT	HASH_ACC done status
[2]	rw1c	1'h0	SETUP_ERR_STAT	AES_ACC setup error status
[1]	rw1c	1'h0	BUS_ERR_STAT	AES_ACC bus error status
[0]	rw1c	1'h0	DONE_STAT	AES_ACC done status
0x0C			**SETTING**	
[31:6]			RSVD	
[5]	rw	1'h0	HASH_PAD_ERR_MASK	HASH_ACC padding error interrupt mask, 0: mask the interrupt

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表 13-1: AES 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[4]	rw	1'h0	HASH_BUS_ERR_MASK	HASH_ACC bus error interrpt mask, 0: mask the interrupt
[3]	rw	1'h0	HASH_DONE_MASK	HASH_ACC done interrupt mask, 0: mask the interrupt
[2]	rw	1'h0	SETUP_ERR_IRQ_MASK	AES_ACC setup error interrupt mask, 0: mask the interrupt
[1]	rw	1'h0	BUS_ERR_IRQ_MASK	AES_ACC bus error interrupt mask, 0: mask the interrupt
[0]	rw	1'h0	DONE_IRQ_MASK	AES_ACC done interrupt mask, 0: mask the interrupt
0x10			**AES_SETTING**	
[31:9]			RSVD	
[8]	rw	1'h0	AES_BYPASS	1'h0: normal operation 1'h1: bypass
[7]	rw	1'h0	AES_OP_MODE	1'h0: decryption 1'h1: encryption
[6]	rw	1'h0	ALGO_STANDARD	1'h0: AES 1'h1: SM4
[5]	rw	1'h0	KEY_SEL	1'h0: select key from AES_ACC key registers 1'h1: use internal root key
[4:3]	rw	2'h0	AES_LENGTH	AES Length: 2'h0: 128-bit 2'h1: 192-bit 2'h2: 256-bit 2'h3: Reserved
[2:0]	rw	3'h0	AES_MODE	AES Mode: 3'h0: ECB 3'h1: CTR 3'h2: CBC Others: Reserved
0x14			**DMA_IN**	
[31:0]	rw	32'h0	ADDR	AES_ACC input data address
0x18			**DMA_OUT**	
[31:0]	rw	32'h0	ADDR	AES_ACC output data address
0x1C			**DMA_DATA**	
[31:28]			RSVD	
[27:0]	rw	28'h0	SIZE	AES_ACC data block size, AES_ACC only support block aligned transaction. Each block contains 16 bytes.
0x20			**IV_W0**	
[31:0]	rw	32'h0	DATA	Initial Vector Word0
0x24			**IV_W1**	
[31:0]	rw	32'h0	DATA	Initial Vector Word1
0x28			**IV_W2**	
[31:0]	rw	32'h0	DATA	Initial Vector Word2
0x2C			**IV_W3**	
[31:0]	rw	32'h0	DATA	Initial Vector Word3
0x30			**EXT_KEY_W0**	
[31:0]	rw	32'h0	DATA	External Key Word0
0x34			**EXT_KEY_W1**	
[31:0]	rw	32'h0	DATA	External Key Word1
0x38			**EXT_KEY_W2**	
[31:0]	rw	32'h0	DATA	External Key Word2
0x3c			**EXT_KEY_W3**	

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表 13-1: AES 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:0]	rw	32'h0	DATA	External Key Word3
0x40			**EXT_KEY_W4**	
[31:0]	rw	32'h0	DATA	External Key Word4
0x44			**EXT_KEY_W5**	
[31:0]	rw	32'h0	DATA	External Key Word5
0x48			**EXT_KEY_W6**	
[31:0]	rw	32'h0	DATA	External Key Word6
0x4C			**EXT_KEY_W7**	
[31:0]	rw	32'h0	DATA	External Key Word7
0x50			**HASH_SETTING**	
[31:9]			RSVD	
[8]	w1t	1'h0	HASH_LEN_LOAD	write 1 to load hash length
[7]	w1t	1'h0	HASH_IV_LOAD	write 1 to load hash iv
[6]	rw	1'h0	RESULT_ENDIAN	hash result endian setting: 1'h0: little endian 1'h1: big endian
[5]	rw	1'h0	DFT_IV_SEL	HASH default iv select. 1'h0: default iv according to hash mode 1'h1: default iv from HASH_IV_H* registers
[4]	rw	1'h0	BYTE_SWAP	HASH byte swap option. Set 1 to swap byte order when read data from memory.
[3]	rw	1'h0	DO_PADDING	HASH padding enable. Set 1 to do padding after data transfer.
[2:0]	rw	3'h0	HASH_MODE	HASH Mode: 3'h0: SHA-1 3'h1: SHA-224 3'h2: SHA-256 3'h3: SM3 Others: Reserved
0x54			**HASH_DMA_IN**	
[31:0]	rw	32'h0	ADDR	input data address
0x58			**HASH_DMA_DATA**	
[31:0]	rw	32'h0	SIZE	HASH input data byte size.
0x5C			**HASH_IV_H0**	
[31:0]	rw	32'h0	DATA	HASH IV H0
0x60			**HASH_IV_H1**	
[31:0]	rw	32'h0	DATA	HASH IV H1
0x64			**HASH_IV_H2**	
[31:0]	rw	32'h0	DATA	HASH IV H2
0x68			**HASH_IV_H3**	
[31:0]	rw	32'h0	DATA	HASH IV H3
0x6C			**HASH_IV_H4**	
[31:0]	rw	32'h0	DATA	HASH IV H4
0x70			**HASH_IV_H5**	
[31:0]	rw	32'h0	DATA	HASH IV H5
0x74			**HASH_IV_H6**	
[31:0]	rw	32'h0	DATA	HASH IV H6
0x78			**HASH_IV_H7**	

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表 13-1: AES 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:0]	rw	32'h0	DATA	HASH IV H7
0x7C			**HASH_RESULT_H0**	
[31:0]	r	32'h0	DATA	HASH result H0
0x80			**HASH_RESULT_H1**	
[31:0]	r	32'h0	DATA	HASH result H1
0x84			**HASH_RESULT_H2**	
[31:0]	r	32'h0	DATA	HASH result H2
0x88			**HASH_RESULT_H3**	
[31:0]	r	32'h0	DATA	HASH result H3
0x8C			**HASH_RESULT_H4**	
[31:0]	r	32'h0	DATA	HASH result H4
0x90			**HASH_RESULT_H5**	
[31:0]	r	32'h0	DATA	HASH result H5
0x94			**HASH_RESULT_H6**	
[31:0]	r	32'h0	DATA	HASH result H6
0x98			**HASH_RESULT_H7**	
[31:0]	r	32'h0	DATA	HASH result H7
0x9C			**HASH_LEN_L**	
[31:0]	rw	32'h0	DATA	HASH load length l
0xA0			**HASH_LEN_H**	
[31:29]			RSVD	
[28:0]	rw	29'h0	DATA	HASH load length h
0xA4			**HASH_RESULT_LEN_L**	
[31:0]	r	32'h0	DATA	HASH result length l
0xA8			**HASH_RESULT_LEN_H**	
[31:29]			RSVD	
[28:0]	r	29'h0	DATA	HASH result length h

13.2 TRNG

TRNG 位于 HPSYS。

13.2.1 简介

TRNG 全称真随机数发生器（True Random Number Generator），该模块利用由数字逻辑组成的震荡电路来生成随机熵源，经过一系列校验生成了随机数种子，在通过伪随机数发生器由种子产生随机数提供给系统使用。

13.2.2 模块架构

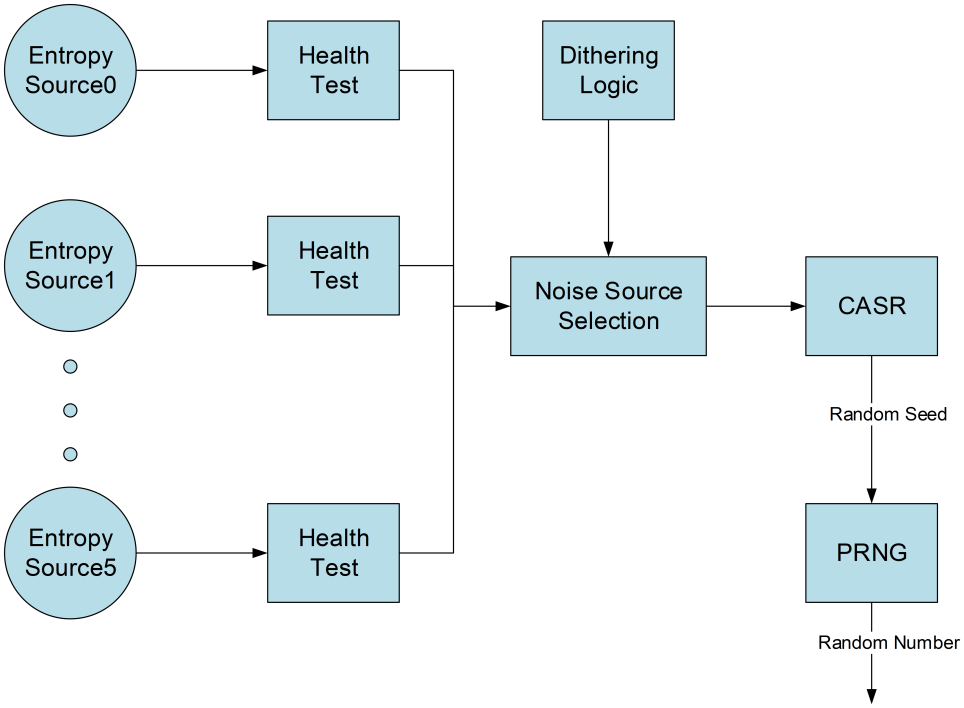

图 13-4: TRNG 结构图

真随机数发生器主要由 3 部分组成：熵源，随机种子发生器，随机数发生器。

13.2.3 功能描述

13.2.3.1 熵源

熵源由六条反相器链组成，每次产生新的随机种子的时候，都会启动所有反相器链，通过一定的校验算法生成随机数种子。随机数种子生成时间较长，同时消耗功耗也会较大，通常建议两种情况下重新生成新的种子，一种是原种子生命周期耗尽，需要定期生成新的种子覆盖，另一种是软件在特殊需求下手动生成新的种子。

熵源会在每次生成种子的时候启动，VN 校验器门限用来筛选熵源，门限越高则对于熵源筛选更宽松，生成种子速度更快，随机性会有所下降。

用户可以直接触发 gen_seed_start，启动熵源模块来生成新的随机种子。

13.2.3.2 随机种子发生器

随机种子发生器从熵源收集数据，通过 CASR(Cellular Automata Shift Register) 模块，生成随机种子，提供给下一级的 PRNG 使用。用户也可以通过寄存器直接获得随机种子。当用户配置 use_ext_seed 为 1 之后，下一级的 PRNG 模块，将不适用随机种子发生器产生的种子，转而使用外部种子来生成随机数。

13.2.3.3 随机数发生器

随机数发生器是基于现有随机种子的伪随机数发生器，相对时间较短且固定。需要注意的是，伪随机数发生器有概率进入自锁状态，原因是内部一些数据序列导致了线性反馈寄存器的死锁，当检测到 prng_lockup 的状态时，建议重新生成一组随机种子来生成新的随机数。

用户可以触发 gen_rand_num_start 来启动随机数发生器，若当前随机种子没有生成，则随机数发生器会先生成随机种子，然后在生成随机数。

13.2.3.4 其他功能模块

TRNG 模块额外提供了反相器链的震荡周期测量，由此可以简介推断芯片所在的工艺角。具体过程首先要确定使用的反相器链编号，因为不同的反相器链长度不同，对应的震荡周期也不同，然后设置震荡的周期数，这个周期数对应的系统 pclk 对应的频率。开启测量后，会有两个计数器分别统计 pclk 的时钟周期和反相器链的时钟周期，当 pclk 的时钟周期数达到设置的阈值时就会停止。此时可以根据 pclk 的时钟频率 Fpclk，周期数 Npclk，还有反相器链的周期数 Ninv 推算出反相器链的频率 Finv=Fpclk*Npclk/Ninv。由此可以推断该芯片所对应的工艺角。

13.2.4 TRNG 寄存器

表 13-2: TRNG 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00			**CTRL**	
[31:5]			RSVD	
[4]	rw	1'h0	gen_rand_num_suspend	Set 1 to suspend random number generation and update. Set 0 to recover the process.
[3]	rw	1'h0	gen_rand_num_stop	Set 1 to stop random number generation and update. This will reset the random number generation engine. After release the stop bit, user should write 1 to gen_rand_num_start to trigger the random number engine.
[2]	rw	1'h0	gen_seed_stop	Set 1 to stop random seed generation. This will reset the random seed generation engine. After release the stop bit, user should write 1 to gen_seed_start to trigger the random seed engine.
[1]	w1t	1'h0	gen_rand_num_start	write 1 to trigger the random number generation engine
[0]	w1t	1'h0	gen_seed_start	write 1 to trigger the random seed generation engine
0x04			**STAT**	
[31:4]			RSVD	
[3]	r	1'h0	rand_num_valid	random number valid flag
[2]	r	1'h0	rand_num_gen_busy	random number engine busy flag
[1]	r	1'h0	seed_valid	random seed valid flag
[0]	r	1'h0	seed_gen_busy	random seed engine busy flag
0x08			**CFG**	
[31:16]			RSVD	
[15:8]	rw	8'ha	reject_threshold	random seed internal VN corrector check threshold
[7:2]			RSVD	
[1]	rw	1'h0	use_ext_seed	set 1 to use external seed to generate random number
[0]	rw	1'h0	auto_clock_enable	auto clock gating enable
0x0c			**IRQ**	
[31:19]			RSVD	

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表 13-2: TRNG 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[18]	rw	1'h1	prng_lockup_msk	prng lockup interrupt mask
[17]	rw	1'h1	rand_num_avail_msk	random number available interrupt mask
[16]	rw	1'h1	seed_gen_done_msk	random seed generation done interrupt mask
[15:3]			RSVD	
[2]	rw1c	1'h0	prng_lockup	prng lockup raw interrupt
[1]	rw1c	1'h0	rand_num_avail	random number available raw interrupt
[0]	rw1c	1'h0	seed_gen_done	random seed generation done raw interrupt
0x10			**rand_seed0**	
[31:0]	rw	32'h0	val	random seed value0. If using external random seed, write value to this register will update the random seed in use.
0x14			**rand_seed1**	
[31:0]	rw	32'h0	val	random seed value1. If using external random seed, write value to this register will update the random seed in use.
0x18			**rand_seed2**	
[31:0]	rw	32'h0	val	random seed value2. If using external random seed, write value to this register will update the random seed in use.
0x1c			**rand_seed3**	
[31:0]	rw	32'h0	val	random seed value3. If using external random seed, write value to this register will update the random seed in use.
0x20			**rand_seed4**	
[31:0]	rw	32'h0	val	random seed value4. If using external random seed, write value to this register will update the random seed in use.
0x24			**rand_seed5**	
[31:0]	rw	32'h0	val	random seed value5. If using external random seed, write value to this register will update the random seed in use.
0x28			**rand_seed6**	
[31:0]	rw	32'h0	val	random seed value6. If using external random seed, write value to this register will update the random seed in use.
0x2c			**rand_seed7**	
[31:0]	rw	32'h0	val	random seed value7. If using external random seed, write value to this register will update the random seed in use.
0x30			**rand_num0**	
[31:0]	r	32'h0	val	random number value0
0x34			**rand_num1**	
[31:0]	r	32'h0	val	random number value1
0x38			**rand_num2**	
[31:0]	r	32'h0	val	random number value2
0x3c			**rand_num3**	
[31:0]	r	32'h0	val	random number value3
0x40			**rand_num4**	
[31:0]	r	32'h0	val	random number value4
0x44			**rand_num5**	
[31:0]	r	32'h0	val	random number value5
0x48			**rand_num6**	
[31:0]	r	32'h0	val	random number value6
0x4c			**rand_num7**	
[31:0]	r	32'h0	val	random number value7
0x50			**cal_cfg**	

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表 13-2: TRNG 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:16]	rw	16'hff	length	calibration length
[15:6]			RSVD	
[5]	r	1'h0	done	calibration done
[4]	rw	1'h0	enable	calibration enable
[3:1]	rw	3'h0	osc_clk_sel	osc clock select
[0]	rw	1'h0	osc_clk_force_on	osc force enable
0x54			**cal_result**	
[31:16]	r	16'h0	osc_cnt	osc clock calibration counter result
[15:0]	r	16'h0	pclk_cnt	pclk calibration counter result

13.3 efusec

efusec 位于 HPSYS。

13.3.1 简介

efusec 即 efuse control, 通过写操作可控制 efuse 相应位的熔断，熔断后的 bit 信息读回为 1，通过读操作可读出所存储的信息值。

13.3.2 主要特性

- 可控制 4 块 256 bit 的 efuse 单元
- 可读\写 1024 bit 信息
- 每次可控制一个 efuse 单元的读\写操作
- 读\写操作为单 bit 串行
- 读\写完成可产生中断信号
- 可实现读写屏蔽功能
- 部分存储信息直接通过模块接口输出
- efuse 的默认值为全 0

13.3.3 写操作

efusec 的写操作就是对 efuse 的一个编程操作，写数据为 1 的 bit，通过熔断的方式将该 bit 设置为开路，使得读回的数据值为 1。写入的信息通过寄存器 PGM_DATA0~7 配置，四个单元共用 8 个 PGM_DATA* 寄存器。写操作的控制流程如下：

- 配置 BANKSEL 寄存器选择要写的 efuse 单元
- 配置 MODE 寄存器选择写操作
- 配置 IE 寄存器使能中断状态
- 配置 PGM_DATA* 寄存器写入编程数据
- 配置 TIMER 寄存器设置关键时长
- 配置 EN 寄存器启动写操作
- 等待中断到来或查询 SR 寄存器获得写完成状态

熔断的 bit 无法恢复到 0 状态，未熔断的 bit 可再次通过写操作进行熔断。

13.3.4 读操作

eFusec 的读操作就是对 efuse 的存储信息进行读取，读出的存储信息可通过 BANK*_DATA* 寄存器查询，每个单元都有独立的寄存器进行数据查询。读操作的控制流程如下：

- 配置 BANKSEL 寄存器选择要读的 efuse 单元
- 配置 MODE 寄存器选择读操作
- 配置 IE 寄存器使能中断状态
- 配置 TIMER 寄存器设置关键时长
- 配置 EN 寄存器启动写操作
- 等待中断到来或查询 SR 寄存器获得读完成状态
- 读取 BANK*_DATA* 寄存器获得读取值
- 部分读取值直接通过接口信号送出

13.3.4.1 读写时间控制

efuse 的读写时序有一定要求，特别是熔断时间，当 efusec 模块的工作时钟变化时，需调整时钟的计数值以满足 efuse 的读写时序要求。需要进行时序控制的时间点有以下三个：

- TCKHP：单 bit 熔断时间，10us
- THPCK：启动写使能的保持时间，>20ns
- THRCK：启动读使能的保持时间，>500ns

通过 TIME 寄存器可配置这三个时间基于工作时钟的计数值。寄存器复位值为 48MHz 工作时钟下的计数值。

13.3.4.2 读写屏蔽功能

为了防止恶意的读写操作，在配置好数据后不再进行数据更新的情况下，可通过控制 bank0 的固定 bit 屏蔽 bank1~3 的 efuse 模块的读\写功能，屏蔽后无法对相应 efuse 进行写操作，也无法再更新读出的数值。

- bank0[255:254]=2’b11, 屏蔽 bank3 写功能；
- bank0[253:252]=2’b11, 屏蔽 bank3 读功能；
- bank0[251:250]=2’b11, 屏蔽 bank2 写功能；
- bank0[249:248]=2’b11, 屏蔽 bank2 读功能；
- bank0[247:246]=2’b11, 屏蔽 bank1 写功能；
- bank0[245:244]=2’b11, 屏蔽 bank1 读功能；

13.3.4.3 模块接口输出信号

efuse 的部分数值会通过模块接口信号输出，他们分别是：

表 13-3: efuse 接口信号

序号	信号名
1	idsel
2	swddis
3	pkgid[1:0]
4	uid[127:0]
5	rootkey[255:0]

13.3.5 efusec 寄存器

表 13-4: efusec 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00			**CR**	Control Register
[31:5]			RSVD	
[4]	rw	1'h0	IE	Interrupt enable
[3:2]	rw	2'h0	BANKSEL	Bank select
[1]	rw	1'h0	MODE	0 - READ, 1 - PGM
[0]	w1s	1'h0	EN	Write 1 to enable PGM/READ. Self clear
0x04			**TIMR**	Timer Register
[31:21]			RSVD	
[20:10]	rw	11'h78	TCKHP	SCLK high period for PGM. Recommended value ~10us
[9:7]	rw	3'h0	THPCK	SCLK to CSB hold time into PGM mode. Recommended value > 20ns
[6:0]	rw	7'h6	THRCK	SCLK to CSB hold time into READ mode. Recmmended value > 500ns
0x08			**SR**	Status Register
[31:1]			RSVD	
[0]	rw1c	1'h0	DONE	Indicates PGM/READ done. Write 1 to clear
0x0C			**RSVDR**	Reserved Register
0x0C			RSVDR	
[31:0]			RSVD	
0x10			**PGM_DATA0**	Program Data0
[31:0]	rw	32'h0	DATA	
0x14			**PGM_DATA1**	Program Data1
[31:0]	rw	32'h0	DATA	
0x18			**PGM_DATA2**	Program Data2
[31:0]	rw	32'h0	DATA	
0x1C			**PGM_DATA3**	Program Data3
[31:0]	rw	32'h0	DATA	
0x20			**PGM_DATA4**	Program Data4
[31:0]	rw	32'h0	DATA	
0x24			**PGM_DATA5**	Program Data5
[31:0]	rw	32'h0	DATA	
0x28			**PGM_DATA6**	Program Data6
[31:0]	rw	32'h0	DATA	
0x2C			**PGM_DATA7**	Program Data7
[31:0]	rw	32'h0	DATA	
0x30			**BANK0_DATA0**	Bank0 Data0
[31:0]	r	32'h0	DATA	
0x34			**BANK0_DATA1**	Bank0 Data1

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表 13-4: efusec 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:0]	r	32'h0	DATA	
0x38			**BANK0_DATA2**	Bank0 Data2
[31:0]	r	32'h0	DATA	
0x3C			**BANK0_DATA3**	Bank0 Data3
[31:0]	r	32'h0	DATA	
0x40			**BANK0_DATA4**	Bank0 Data4
[31:0]	r	32'h0	DATA	
0x44			**BANK0_DATA5**	Bank0 Data5
[31:0]	r	32'h0	DATA	
0x48			**BANK0_DATA6**	Bank0 Data6
[31:0]	r	32'h0	DATA	
0x4C			**BANK0_DATA7**	Bank0 Data7
[31:0]	r	32'h0	DATA	
0x50			**BANK1_DATA0**	Bank1 Data0
[31:0]	r	32'h0	DATA	
0x54			**BANK1_DATA1**	Bank1 Data1
[31:0]	r	32'h0	DATA	
0x58			**BANK1_DATA2**	Bank1 Data2
[31:0]	r	32'h0	DATA	
0x5C			**BANK1_DATA3**	Bank1 Data3
[31:0]	r	32'h0	DATA	
0x60			**BANK1_DATA4**	Bank1 Data4
[31:0]	r	32'h0	DATA	
0x64			**BANK1_DATA5**	Bank1 Data5
[31:0]	r	32'h0	DATA	
0x68			**BANK1_DATA6**	Bank1 Data6
[31:0]	r	32'h0	DATA	
0x6C			**BANK1_DATA7**	Bank1 Data7
[31:0]	r	32'h0	DATA	
0x70			**BANK2_DATA0**	Bank2 Data0
[31:0]	r	32'h0	DATA	
0x74			**BANK2_DATA1**	Bank2 Data1
[31:0]	r	32'h0	DATA	
0x78			**BANK2_DATA2**	Bank2 Data2
[31:0]	r	32'h0	DATA	
0x7C			**BANK2_DATA3**	Bank2 Data3
[31:0]	r	32'h0	DATA	
0x80			**BANK2_DATA4**	Bank2 Data4
[31:0]	r	32'h0	DATA	
0x84			**BANK2_DATA5**	Bank2 Data5
[31:0]	r	32'h0	DATA	
0x88			**BANK2_DATA6**	Bank2 Data6
[31:0]	r	32'h0	DATA	
0x8C			**BANK2_DATA7**	Bank2 Data7
[31:0]	r	32'h0	DATA	
0x90			**BANK3_DATA0**	Bank3 Data0
[31:0]	r	32'h0	DATA	
0x94			**BANK3_DATA1**	Bank3 Data1

续表下页...

表 13-4: efusec 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:0]	r	32'h0	DATA	
0x98			**BANK3_DATA2**	Bank3 Data2
[31:0]	r	32'h0	DATA	
0x9C			**BANK3_DATA3**	Bank3 Data3
[31:0]	r	32'h0	DATA	
0xA0			**BANK3_DATA4**	Bank3 Data4
[31:0]	r	32'h0	DATA	
0xA4			**BANK3_DATA5**	Bank3 Data5
[31:0]	r	32'h0	DATA	
0xA8			**BANK3_DATA6**	Bank3 Data6
[31:0]	r	32'h0	DATA	
0xAC			**BANK3_DATA7**	Bank3 Data7
[31:0]	r	32'h0	DATA	
0xB0			**ANACR**	Bank3 Data7
[31:24]	r	8'h0	RESERVE1	
[23:16]	rw	8'h0	RESERVE0	
[15:11]			RSVD	
[10:8]	rw	3'h0	LDO_DC_TR	
[7:5]			RSVD	
[4]	rw	1'h0	LDO_MODE	
[3:1]	rw	3'h4	LDO_VREF_SEL	
[0]	rw	1'h0	LDO_EN	
0xB4			**DB_SEL**	debug signal select
[31:0]	rw	32'h0	db_sel	debug signal select

14 存储接口

14.1 SDMMC1

芯片共有 2 个 SDMMC，均位于 HPSYS。应注意两个 SDMMC 的使用方法不同，调用的驱动也不一样。其中 SDMMC1 内置 DMA 并支持 DDR 与 8 线模式；SDMMC2 不支持 DDR 与 8 线模式，可向 DMAC1 发送请求。

14.1.1 简介

SDMMC 支持 SD 协议 3.0 以及 eMMC 标准 4.51，可作为 HOST 控制器与 SD/SDIO/eMMC 设备交互。SDMMC 内置链式 DMA 控制器以及 1K 字节 FIFO，可自主进行数据读写，支持分块数据搬运。SDMMC 支持 SDR 单线、4 线和 8 线模式，并支持 DDR 4 线和 8 线模式。

14.1.2 主要特性

- 兼容 SD Host Controller Standard Specification Version 3.0
- 兼容 SD 3.0 Physical Layer Specification Version 3.01
- 兼容 SDIO Specification Version 3.0
- 兼容 JEDEC JESD84-B451 eMMC 4.51 Specification
- 支持 SDSC/SDHC/SDXC/SDHS 卡
- 支持支持 UHS-1：SDR12/SDR25/SDR50/SDR104/DDR50
- 支持 SDR 单线、4 线、8 线模式
- 支持 DDR 4 线、8 线模式
- 内置 1K 字节 FIFO，最大支持单 block 512 字节
- 可配置时钟
- 内置链式 DMA

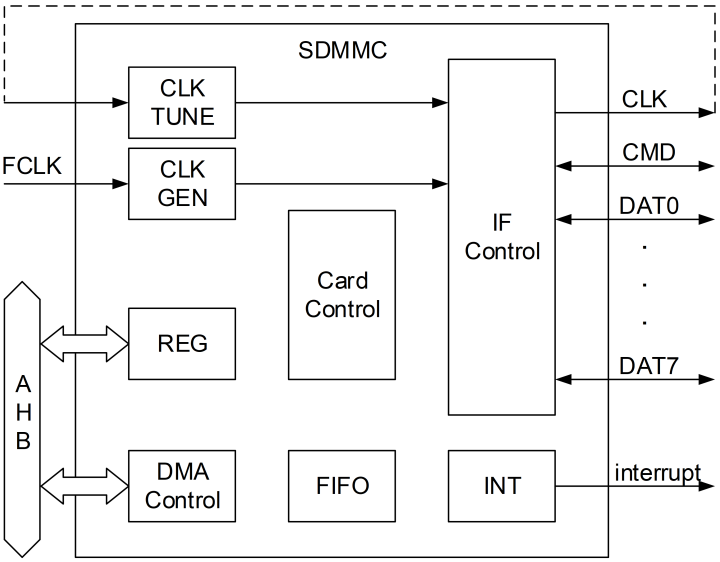

图 14-1: SDMMC 结构图

14.1.3 功能描述

14.1.3.1 SD/eMMC 接口

控制器支持的 SD/eMMC 接口共包括一根 CLK 线，一根 CMD 线和 8 根 DAT 线 (DAT0~DAT7)。CLK 线用于输出时钟。CMD 线依照协议打包传输 CMD 命令以及应答 RSP。DAT 线依照协议传输数据流。CMD 线仅支持单边沿 (SDR) 传输，即 CMD 仅在 CLK 的上升沿有效。DAT 线既支持单边沿 (SDR) 传输，即 DAT 仅在 CLK 的上升沿有效；也支持双边沿 (DDR) 传输，即 DAT 在 CLK 的上升沿和下降沿同时有效。

14.1.3.2 时钟设置

SDMMC 有独立的功能时钟 FCLK,能够在系统时钟或 DLL 时钟中进行选择,选择寄存器为 RCC 模块的 CSR_SEL_SDMMC。需要注意 SDMMC 工作时，系统时钟频率 HCLK 不能低于 FCLK，同时 CR3_INTCLKEN 需要置 1。

输出到 SD/eMMC 接口的 CLK 是由 FCLK 分频产生，分频比 CLKDIV 共 10bit，其中低 8 位由 CR3_CLKDIVL 指定，高 2 位由 CR3_CLKDIVU 指定。当 CLKDIV 等于 0 时，CLK 频率等于 FCLK 频率，否则 CLK 频率 =FCLK 频率/(2*CLKDIV)。例如当 FCLK 为 192M 时，要输出 400KHz 的 CLK，就需要将 CLKCR_DIV 配置成 240。当进行 DDR 传输时，CLKDIV 应当配置为偶数。

CLK 输出由 CR3_CLKEN 控制，设置为 1 以后时钟会持续输出，设置为 0 关闭输出。当时钟频率发生调整时，应当关闭 CLK 输出，设置完毕后再开启。

14.1.3.3 发送命令

命令是由控制器通过 CMD 线发送，由 SD/eMMC/SDIO 设备接收的固定格式的包，用于配置 SD/eMMC/SDIO 设备的状态，并控制数据的传输。命令的包长度固定为 48bit。

表 14-1: 命令包格式

Bit position	47	46	[45:0]	[39:8]	[7:1]	0
Width(bits)	1	1	6	32	7	1
Value	0	1	x	x	x	1
Description	Start bit	Transimission bit	Command index	Argument	CRC7	End bit

每条命令通过 6bit 的命令编号区分不同功能，并附带 32bit 的参数。设备通过 7bit CRC 判断接收到的命令是否正确，并在需要回复时发送响应。

根据 6bit 的命令编号 (command index)，命令通常被命名为 CMDn，其中 n 就是命令编号，由 CR1_CMDIDX 寄存器配置。

命令的 32bit 参数 (argument) 由 ARG1 寄存器配置。

某些命令如 CMD0，CMD4 等不需要接收响应；某些命令如 CMD8,CMD11 等需要接收 48bit 的响应；某些命令如 CMD2 需要接收 136bit 的响应。发送命令前，需要通过配置 CR1_RSPTYPE 寄存器选择命令期望的响应。

某些响应中包含了 command index 以及 CRC 校验值。如果要检查响应中的内容是否正确，可以根据需要配置 CR1_CHECKIDX 和 CR1_CHECKCRC。

某些命令如 CMD18，CMD24 等发送后需要进行数据读写，需要将 CR1_DATAPRESENT 置 1.

命令发送由写入 CR1_CMDIDX 的行为触发，因此推荐将命令的所有参数准备好以后一次性写入到 CR1 寄存器中，启动命令发送流程。

命令发送的状态可以通过 SR_CMDBUSY 查询。当 SR_CMDBUSY 为 1 时，说明命令发送流程 (包括接收响应) 仍在进行。

命令发送流程结束时，命令完成标志 ISR_CC 置 1 (当 ISER_CCEN 为 1 时)，且当 IER_CCIE 为 1 时可产生中断。接收响应的状态可以在 ISR 寄存器中查询，包括响应超时错误 ISR_CTOERR(64 个 CLK 内未检测到响应起始位)，响应 CRC 错误 ISR_CCRCERR，响应结束位错误 ISR_CEBERR，以及响应 index 错误 ISR_IDXERR。

接收到响应的 argument 保存在 RSP1~RSP4 中，其中 48bit 响应的 argument 保存在 RSP1 中。

如果响应带有 busy 信号 (如 R1b)，当 busy 信号结束后，传输完成标志 ISR_TC 会置 1(当 ISER_TCEN 为 1 时)，且当 IER_TCIE 为 1 时可产生中断。

命令发送的建议软件流程：

1. 一次性配置 index，argument 以及期望响应类型，启动命令发送
2. 等待命令完成中断，以及传输完成中断 (如果响应带 busy 信号)。
3. 检查返回的响应并获取 argument

14.1.3.4 数据传输

数据传输包括从设备读取数据和向设备写入数据，由控制器发送特定命令 (如 CMD17，CMD24 等) 启动，数据传输预设长度后结束，或由控制器发送特定命令 (如 CMD12) 结束。

SD 和 SDIO 协议定义的数据传输可采用单线或 4 线模式。eMMC 协议定义的数据传输可采用单线，4 线或 8 线模式。控制器支持单线，4 线或 8 线传输，通过 CR2_DATWIDTH 和 CR2_EXTWIDTH 寄存器配置。单线模式下，

数据通过 DAT0 传输，DAT0 也同时用于表示数据传输的 busy 状态。4 线模式下，数据通过 DAT0~DAT3 传输，DAT0 也同时用于表示数据传输的 busy 状态。8 线模式下，数据通过 DAT0~DAT7 传输，DAT0 也同时用于表示数据传输的 busy 状态。

控制器支持 4 线或 8 线 DDR 传输。将 CR4_UHSMODE 寄存器配置成 4 时数据为 DDR 传输，否则为 SDR 传输。

表 14-2: 数据传输模式配置

传输模式	线宽	CR2_DATWIDTH	CR2_EXTWIDTH	CR4_UHSMODE
SDR	单线	0	0	0
	4 线	1	0	0
	8 线	x	1	0
DDR	4 线	1	0	4
	8 线	x	1	4

数据采用分块传输的形式，每块的数据量大小根据设备类型有所不同。对于 SD 和 eMMC 设备，单块数据量通常为 512byte，但也有例外。某些设备允许通过命令 (如 CMD16) 改变单块数据量。控制器开始数据传输前，应当根据设备单块数据字节数配置 BSR_BSIZE 寄存器。控制器还需配置 CR1_MULTIBLK 和 BSR_BCNT 寄存器来确定单次数据传输的总块数。对于单块传输，CR1_MULTIBLK 应等于 0，此时 BSR_BCNT 不生效。对于多块传输，CR1_MULTIBLK 与 CR1_BCNTEN 应等于 1，并将 BSR_BCNT 配置成需要传输的总块数。

数据传输的方向由 CR1_DIR 配置，0 为读取，1 为写入。

数据传输配置完成后，当控制器发送读写命令 (命令配置 CR1_DATAPRESENT 为 1) 之后，会自动启动数据传输。

数据传输需经过控制器内部的 FIFO 缓存。待发送的数据由 CPU 或控制器内置 DMA 向 FIFO 写入，随后控制器再将 FIFO 中的数据写入到设备。从设备读取的数据也暂存在 FIFO 中，再由 CPU 或内置 DMA 取出。FIFO 的容量为 1024 字节，CPU 访问入口为 BUF 寄存器。

多块传输时，设备接收到传输结束命令 (如 CMD12) 才会停止传输。控制器支持所有数据块传输完成后自动发送传输结束命令，使能方式为将 CR1_AUTOCMD 置 1。

通过 SR_DATBUSY 可以查询数据传输是否完成。

数据传输有两种结束方式：

1. 传输正常结束。当指定块数的数据传输全部完成并且没有出错时，传输完成标志 ISR_TC 置 1(当 ISER_TCEN 为 1 时)，且当 IER_TCIE 为 1 时可产生中断。
2. 传输出错，包括数据超时 (ISR_DTOERR)，数据 CRC 错误 (ISR_DCRCERR) 以及数据结束位错误 (DEBERR)3 类。每种错误均可产生相应中断。其中数据超时的时间由 CR3_DTOCNT 配置，计算公式为：超时时间 =FCLK 周期 *4096*2^{CR3_DTOCNT}，其中 CR3_DTOCNT 小于 15。例如当 FCLK 为 48MHz，CR3_DTOCNT 为 13 时，超时时间约为 699ms。当出现传输出错时，可能无法产生正常结束中断 ISR_TC，因此必须同时监测正常结束中断与错误中断。

数据传输的建议软件流程：

1. 配置传输方向，传输线宽，超时时间，自动命令模式，单块数据量和总块数
2. 配置内置 DMA(SDMA 或 ADMA)

3. 发送读命令 (如 CMD17) 或写命令 (如 CMD24)
4. 等待命令中断，处理设备响应 (如 R1)
5. 等待数据传输结束中断或出错中断

14.1.3.5 中断产生

SDMMC 能够产生中断，用于通知 CPU 特定事件发生。这些事件包括命令发送完成，数据完成，以及各种错误等。发生的事件可通过 SR 寄存器查询。需注意只有 ISER 使能的事件才能够被记录，而记录的事件能否产生中断是通过 IER 寄存器配置。因此使能中断时，需要同时将对应事件的 ISER 和 IER 置 1。

14.1.3.6 FIFO 管理

SDMMC 内置 1KB 大小的 FIFO 用于缓存读写数据。FIFO 与内置的 DMA 配合完成数据搬运。在向设备写入数据时，控制器仅当 FIFO 中保存的数据量达到或超过单块数据量后才会启动一块数据写操作，否则会等待 CPU 或 DMA 往 FIFO 中搬入数据。等待期间接口 CLK 不会暂停输出。写多块数据过程中，每一块数据写入均遵循上述机制。

在从设备读取数据时，控制器仅当 FIFO 的剩余空间大于等于单块数据量后才会启动一块数据读操作，否则会等待 CPU 或 DMA 从 FIFO 中搬走数据。等待期间接口 CLK 暂停输出，以防止设备输出数据。读多块数据过程中，每一块数据读取均遵循上述机制。

14.1.3.7 DMA 传输

数据传输时，FIFO 的内容可以由 CPU 直接通过 FIFO 入口搬运，也可以通过内置 DMA 自动搬运。

内置 DMA 分为 SDMA 和 ADMA 两个模式。SDMA 配置简洁，能够完成基本的 DMA 功能。ADMA 支持链式传输，功能更丰富，使用前需要创建链式描述表。

DMA 功能通过 CR1_DMAEN 寄存器使能。DMA 模式通过 CR2_DMAMODE 选择，0 为 SDMA，2 为 ADMA。

SDMA 模式下，需配置数据搬运的起始地址 SAR，通常指向存储器 SRAM 或 PSRAM。数据传输启动后，SDMA 会自动将待写入数据从存储器搬运进 FIFO，或将读取到的数据从 FIFO 搬运到存储器。多块传输时，SDMA 会自动搬运多块连续地址的数据，并在存储器的特定地址边界自动暂停。

为方便文件系统管理，SDMA 模式搬运存储器数据时，在跨越特定地址边界处会暂停。存储器的地址边界由 BSR_SDMABDY 设定，从 4KB 到 512KB 可选。当存储器地址跨越特定地址边界时，SDMA 自动暂停，产生 SR_DMA 标志 (当 ISER_DMAEN 为 1 时)，并可产生中断 (当 IER_DMAIE 为 1 时)。暂停时，下一个待传输数据的存储器地址可以从 NSAR 寄存器读出 (此时 SAR 寄存器的值仍为之前配置的值)。CPU 检测到暂停后，需将后续待传输数据的存储器地址写入 SAR 寄存器，SDMA 会自动从新配置的存储器地址继续之前的传输。例如若将 BSR_SDMABDY 配置为 0(4KB 边界)，启动从 0x20019c00 开始搬运 2KB 数据，那么当 0x20019ffc 的 4 字节数据搬运完成后，SDMA 会自动暂停，此时 NSAR 寄存器的值为 0x2001a000。如果此时向 SAR 寄存器写入新地址 0x2001b000，SDMA 会自动从 0x2001b000 开始继续搬运剩余的 1KB 数据。

ADMA 模式使用前需要创建链式描述表。链式描述表的起始地址应当为 4 字节对齐，并写入 ASAR 寄存器。

链式描述表的每个表项占据 8 个字节空间，起始地址应当为 4 字节对齐。表项可分为传输表项和跳转表项两种类型，其中传输表项的下一个表项必须与该传输表项顺序存储，即下一个表项的首地址是该传输表项的首地址加 8 个字节；跳转表项指向的表项可以存储在任何 4 字节对齐的地址，与该跳转表项自身的存储位置无关。表

项格式如下。

表 14-3: 链式描述表表项格式

	bit field							
baseaddr	31~16	15~6	5	4	3	2	1	0
	LENGTH	reserved(0)	ACT2	ACT1	0	INT	END	VALID
baseaddr+4	63~32							
	ADDR							

表项字域含义如下：

VALID	为 1 表示当前表项有效，为 0 会产生错误标志 ISR_ADMAERR，并可产生中断。
END	为 1 表示当前表项为最终表项，没有下一个表项。最终表项执行完成会产生标志 ISR_TC，并可产生中断
ACT1/ACT2	用于标识表项类型。 ACT2 为 0 表示当前表项不需执行，直接进行下一个表项。 ACT2 为 1，ACT1 为 0 表示当前表项为传输表项，ADMA 需进行数据传输，ADDR 表示数据的起始地址。 ACT2 为 1，ACT1 为 1 表示当前表项为跳转表项，ADMA 不需进行数据传输，ADDR 表示下一个表项的存储地址。
LENGTH	当前表项为传输表项时，表示传输数据的字节数，其中 0 表示 65536 字节。传输字节数应当为单块数据字节数的整数倍。
ADDR	当前表项为传输表项时，表示数据的起始地址。当前表项为跳转表项时，表示下一个表项的存储地址。

ADMA 链式描述表的一个示例如下图。表项 ABCD 顺序存储在地址 A 开始的地址空间，表项 EF 顺序存储在地址 E 开始的地址空间。表项 ABCD 顺序执行，当执行到表项 D，跳转到表项 E 执行；表项 EF 顺序执行，当执行完表项 F 时，结束 ADMA 传输。

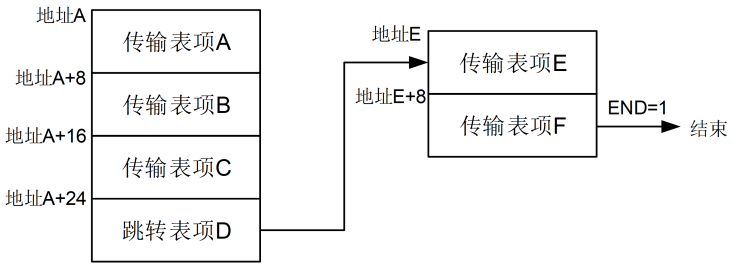

图 14-2: ADMA 链式描述表示例

14.1.3.8 eMMC 开漏模式

当 eMMC 设备处于某些状态 (如 inactive，idle，identification 状态，详见 eMMC 协议) 时，CMD 线需要配置成开漏模式，通过将 CR2_PPMODE 配置成 0 实现。

当访问 SD/SDIO 设备时，以及当 eMMC 进入其它状态时，需要将 CMD 线配置成推挽模式，即 CR2_PPMODE 配置成 1。

14.1.3.9 SDIO 中断

SDIO 设备可以通过拉低 DAT1 产生 SDIO 中断通知控制器。如果控制器需要响应 SDIO 中断，需要使能 ISER_CARDEN 和 IER_CARDIE。检测到中断后，SR_CARD 会置 1。

14.1.3.10 SD 卡片检测

SD 卡支持热拔插。卡片的插入与弹出检测通常有以下 3 种方式实现。

1. 通过专用 CD(card detect) 管脚检测。支持插入检测的 SD 卡槽通常提供一个专用的卡片检测管脚 (CD)，该管脚与电源间存在上拉电阻。芯片需要分配一个独立 IO 用于检测该管脚电平。当没有插入 SD 卡时，该管脚电平为高。当 SD 卡片插入卡槽时，该管脚与地导通，电平为低。通过判断该 IO 的 GPIO 输入电平，可以实现 SD 卡的插入与弹出检测。
2. 通过 DAT3 管脚检测。SD 卡上电时，卡片内部的 DAT3 到电源有 50K 欧姆的上拉电阻。芯片外部电路需要在 DAT3 管脚上放置到地的弱下拉电阻 (通常需大于 470K 欧姆)。芯片通过检测与 DAT3 相连接的 IO 电平，判断卡片是否插入。当没有插入 SD 卡时，该管脚电平为低。当 SD 卡片插入卡槽时，该管脚被上拉到高电平。通过判断该 IO 的 GPIO 输入电平，可以实现 SD 卡的插入与弹出检测。SD 卡启动数据传输时，应当停止该检测，将 DAT3 作为正常数据线使用。
3. 通过命令轮询检测。芯片每隔一段时间向 SD 卡发起命令交互，根据命令是否得到响应判断卡片是否存在。

14.1.3.11 采样时钟调节

SDMMC 与设备通信时，需要在 CLK 的边沿采样从设备输入的 CMD 与 DAT 信号。由于信号传输存在时延，可能需要调节采样时钟的边沿以保证采样正确。

SCR_SEL 选择控制器用于采样的 CLK 是使用外部回环时钟还是内部产生的时钟。外部回环时钟需要将 IO 输出的 CLK 在芯片外部通过另一个 IO 回环输入，能够更准确的补偿 IO 延时，代价是多占用一个 IO。

SCR_DLY 寄存器可以调节采样时钟的边沿，共有 64 档，配置值越大延时越大。当 CLK 频率大于 50M 时，往往需要调节采样时钟以保证接口功能正确。与 eMMC 设备交互时，控制器可以配置不同延时并发送 CMD21 以及调谐块，找到最佳采样点。

eMMC 调谐的建议软件流程：

1. 将设备设置为 HS200 模式 (CMD6)
2. 控制器配置 CLK 频率为目标频率，并设置目标线宽
3. SCR_DLY 配置成起始值（0 或其它经验值）
4. 控制器发送 CMD21 请求设备发送调谐块，并接收响应
5. 控制器接收设备发送的调谐块数据
6. 将调谐块数据与调谐块模板比对，记录数据正误
7. 将 SCR_DLY 增大 1(最大支持 63)
8. 重复步骤 4 7 若干次
9. 在扫描完成的数据正误记录里，选择连续接收正确的窗口中间位置的 SCR_DLY 作为最佳采样值
10. 将 SCR_DLY 配置为最佳采样值，开始进行后续数据传输

上述调谐过程应每隔一段时间，或工作状态发生改变时重新进行，以跟踪温度或环境的变化。

14.1.4 SDMMC 寄存器

表 14-4: SDMMC 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00			**SAR**	System Address/Argument2 Register
[31:0]	rw	32'h0	ADDR	This register contains the physical system memory address used for DMA transfers or the second argument for the Auto CMD23. (1) SDMA System Address This register contains the system memory address for a SDMA transfer. The SDMA transfer waits at the every boundary specified by BSR_SDMABDY. After SDMA has stopped, the next system address of the next contiguous data position cannot be read from this register but from NSAR. The Host Controller generates ISR_DMA Interrupt to request the Host Driver to update this register. The Host Driver sets the next system address of the next data position to this register. When the most upper byte of this register is written, the Host Controller restarts the SDMA transfer. (2) Argument 2 This register is used with the Auto CMD23 to set a 32-bit block count value to the argument of the CMD23 while executing Auto CMD23. If Auto CMD23 is used with ADMA, the full 32-bit block count value can be used. If Auto CMD23 is used without AMDA, the available block count value is limited by BSR_BCNT. 65535 blocks is the maximum value in this case.
0x04			**BSR**	Block Size Register
[31:16]	rw	16'h0	BCNT	Blocks Count For Current Transfer. This register is enabled when MULTIBLK is set to 1 and is valid only for multiple block transfers. Controller decrements the block count after each block transfer. Setting the block count to 0 results in no data blocks is transferred. This register should be accessed only when no transaction is executing (i.e., after transactions are stopped). During data transfer, read operations on this register may return an invalid value and write operations are ignored. When a suspend command is completed, the number of blocks yet to be transferred can be determined by reading this register. Before issuing a resume command, the Host Driver shall restore the previously saved block count. FFFFh 65535 blocks ... ... 0002h 2 blocks 0001h 1 block 0000h Stop Count
[15]			RSVD	

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表 14-4: SDMMC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[14:12]	r	3'h0	SDMABDY	Host SDMA Buffer Boundary. The large contiguous memory space may not be available in the virtual memory system. To perform long SDMA transfer, SDMA System Address register shall be updated at every system memory boundary during SDMA transfer. These bits specify the size of contiguous buffer in the system memory. The SDMA transfer shall wait at the every boundary specified by these fields and the Controller generates the ISR_DMA Interrupt to request the Host Driver to update the SDMA System Address register. At the end of transfer, the Controller may issue or may not issue ISR_DMA Interrupt. In particular, ISR_DMA Interrupt shall not be issued after ISR_TC Interrupt is issued. In case of this register is set to 0 (buffer size = 4K bytes), lower 12-bit of byte address points data in the contiguous buffer and the upper 20-bit points the location of the buffer in the system memory. The SDMA transfer stops when the Controller detects carry out of the address from bit 11 to 12. ADMA does not use this register. 000b 4K bytes (Detects A11 carry out) 001b 8K bytes (Detects A12 carry out) 010b 16K Bytes (Detects A13 carry out) 011b 32K Bytes (Detects A14 carry out) 100b 64K bytes (Detects A15 carry out) 101b 128K Bytes (Detects A16 carry out) 110b 256K Bytes (Detects A17 carry out) 111b 512K Bytes (Detects A18 carry out)
[11:0]	rw	12'h0	BSIZE	Transfer Block Size This register specifies the block size of data transfers such as CMD17, CMD18, CMD24, CMD25, and CMD53. Usually set to 512 for SD and eMMC access.
0x08			**ARG1**	Argument 1
[31:0]	rw	32'h0	ARG	Command Argument 1 The SD command argument is specified as bit39-8 of Command-Format in the Physical Layer Specification.
0x0C			**CR1**	Control and Command Register 1
[31:30]			RSVD	
[29:24]	rw	6'h0	CMDIDX	Command Index These bits shall be set to the command number (CMD0-63, ACMD0-63) that is specified in bits 45-40 of the Command-Format in the Physical Layer Specification and SDIO Card Specification.

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表 14-4: SDMMC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[23:22]	rw	2'h0	CMDTYPE	Command Type There are three types of special commands: Suspend, Resume and Abort. These bits shall be set to 00b for all other commands. (1) Suspend Command If the Suspend command succeeds, the Controller shall assume the SD Bus has been released and that it is possible to issue the next command, which uses the DAT line. The Controller shall de-assert Read Wait for read transactions and stop checking busy for write transactions. The interrupt cycle shall start, in 4-bit mode. If the Suspend command fails, the Controller shall maintain its current state, and the Host Driver shall restart the transfer by setting CR2_CONTREQ. (2) Resume Command The Host Driver re-starts the data transfer. The Controller shall check for busy before starting write transfers. (3) Abort Command If this command is set when executing a read transfer, the Controller shall stop reads to the buffer. If this command is set when executing a write transfer, the Controller shall stop driving the DAT line. After issuing the Abort command, the Host Driver should issue a software reset. 11b Abort CMD12, CMD52 for writing "I/O Abort" in CCCR 10b Resume CMD52 for writing "Function Select" in CCCR 01b Suspend CMD52 for writing "Bus Suspend" in CCCR 00b Normal Other commands
[21]	rw	1'h0	DATAPRESENT	Data Present Select This bit is set to 1 to indicate that data is present and shall be transferred using the DAT line. It is set to 0 for the following: (1) Commands using only CMD line (ex. CMD52). (2) Commands with no data transfer but using busy signal on DAT[0] line (R1b or R5b ex. CMD38) (3) Resume command
[20]	rw	1'h0	CHECKIDX	Command Index Check Enable If this bit is set to 1, the Controller shall check the Index field in the response to see if it has the same value as the command index. If it is not, it is reported as a Command Index Error. If this bit is set to 0, the Index field is not checked.
[19]	rw	1'h0	CHECKCRC	Command CRC Check Enable If this bit is set to 1, the Controller shall check the CRC field in the response. If an error is detected, it is reported as a Command CRC Error. If this bit is set to 0, the CRC field is not checked. The position of CRC field is determined according to the length of the response.
[18]			RSVD	
[17:16]	rw	2'h0	RSPTYPE	Response Type Select 00 No Response 01 Response Length 136 10 Response Length 48 11 Response Length 48 check Busy after
[15:12]			RSVD	
[11]	rw	1'h0	STREAMMODE	Stream Mode Enable The Host driver has to set this bit for MMC CMD11 / CMD20 Stream Read/Write Operations.
[10:6]			RSVD	

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表 14-4: SDMMC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[5]	rw	1'h0	MULTIBLK	Multi / Single Block Select This bit is set when issuing multiple-block transfer commands using DAT line. For any other commands, this bit shall be set to 0. If this bit is 0, it is not necessary to set BSR_BCNT
[4]	rw	1'h0	DIR	Data Transfer Direction Select This bit defines the direction of DAT line data transfers. The bit is set to 1 to read data from the SD card to the Controller and it is set to 0 for all other commands. 1 Read (Card to Host) 0 Write (Host to Card)
[3:2]	rw	2'h0	AUTOCMD	Auto CMD Enable This field determines use of auto command functions. 00b Auto Command Disabled 01b Auto CMD12 Enabled 10b Auto CMD23 Enabled 11b Reserved There are two methods to stop Multiple-block read and write operation. (1) Auto CMD12 Enable When this field is set to 01b, the Controller issues CMD12 automatically when last block transfer is completed. Auto CMD12 error is indicated to CR4. The Host Driver shall not set this bit if the command does not require CMD12. (2) Auto CMD23 Enable When this bit field is set to 10b, the Controller issues a CMD23 automatically before issuing a command specified. The following conditions are required to use the Auto CMD23. A memory card that supports CMD23 (SCR[33]=1) If DMA is used, it shall be ADMA. Only when CMD18 or CMD25 is issued (Note, the Controller does not check command index.) Auto CMD23 can be used with or without ADMA. The Controller issues a CMD23 first and then issues a command specified by CR1. If response errors of CMD23 are detected, the second command is not issued. A CMD23 error is indicated in CR4. 32-bit block count value for CMD23 is set to SAR.
[1]	rw	1'h0	BCNTEN	Block Count Enable This bit is used to enable the Block Count register, which is only relevant for multiple block transfers. When this bit is 0, the Block Count register is disabled, which is useful in executing an infinite transfer. If ADMA data transfer is more than 65535 blocks, this bit shall be set to 0. In this case, data transfer length is designated by Descriptor Table.
[0]	rw	1'h0	DMAEN	DMA Enable This bit enables DMA functionality. SDMA or ADMA mode can be selected by CR2_DMAMODE.
0x10			**RSP1**	Command Response 31 0

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表 14-4: SDMMC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:0]	r	32'h0	RSP	Command Response [31:0] The Response Field indicates bit positions of "Responses" defined in the Physical Layer Spec. Most responses with a length of 48 (R[47:0]) have 32 bits of the response data (R[39:8]) stored in RSP1. Responses of type R1b (Auto CMD12 responses) and R1 (Auto CMD23 response) have response data bits R[39:8] stored in RSP4. Responses with length 136 (R[135:0]) have 120 bits of the response data (R[127:8]) stored in RSP1~RSP4. To be able to read the response status efficiently, the Controller only stores part of the response data. This enables the Host Driver to read 32 bits of response data efficiently in one read cycle on a 32-bit bus system. Parts of the response, the Index field and the CRC, are checked by the Controller (as specified by CR1_CHECKIDX and the CR1_CHECKCRC) and generate an error interrupt if an error is detected. The bit range for the CRC check depends on the response length. If the response length is 48, the Controller shall check R[47:1], and if the response length is 136 the Controller shall check R[119:1]. Since the Controller may have a multiple block data DAT line transfer executing concurrently with a CMD_wo_DAT command, the Controller stores the Auto CMD12 response in RSP4. The CMD_wo_DAT response is stored in RSP1. This allows the Controller to avoid overwriting the Auto CMD12 response with the CMD_wo_DAT and vice versa. While executing Auto CMD23, the response of CMD23 is saved to RSP4 and the response of multiple-block read and write command is save to RSP1. The response error of CMD23 is indicated in CR4.
0x14			**RSP2**	Command Response 63 32
[31:0]	r	32'h0	RSP	Command Response [63:32]
0x18			**RSP3**	Command Response 95 64
[31:0]	r	32'h0	RSP	Command Response [95:64]
0x1C			**RSP4**	Command Response 127 96
[31:0]	r	32'h0	RSP	Command Response [127:96]
0x20			**BUF**	Buffer Data Port Register
[31:0]	rw	32'h0	DATA	Buffer Data The Controller buffer can be accessed through this 32-bit Data Port register.
0x24			**SR**	Present State Register
[31:25]			RSVD	
[24]	r	1'h0	CMDLVL	CMD Line Signal Level This status is used to check the CMD line level to recover from errors, and for debugging.
[23:20]	r	4'h0	DATLVL	DAT-DAT3 Line Signal Level This status is used to check the DAT line level to recover from errors, and for debugging. This is especially useful in detecting the busy signal level from DAT [0].
[19:12]			RSVD	
[11]	r	1'h0	BUFREN	Buffer Read Enable This status is used for non-DMA read transfers. The Controller may implement multiple buffers to transfer data efficiently. This read only flag indicates that valid data exists in the host side buffer. If this bit is 1, readable data exists in the buffer. A change of this bit from 1 to 0 occurs when all the block data is read from the buffer. A change of this bit from 0 to 1 occurs when block data is ready in the buffer and generates ISR_BUFRRDY.

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表 14-4: SDMMC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[10]	r	1'h0	BUFWEN	Buffer Write Enable This status is used for non-DMA write transfers. The Controller can implement multiple buffers to transfer data efficiently. This read only flag indicates if space is available for write data. If this bit is 1, data can be written to the buffer. A change of this bit from 1 to 0 occurs when all the block data is written to the buffer. A change of this bit from 0 to 1 occurs when top of block data can be written to the buffer and generates ISR_BUFWRDY. The Controller should neither set Buffer Write Enable nor generate ISR_BUFWRDY after the last block data is written to the Buffer Data Port Register.
[9]	r	1'h0	RACTIVE	Read Transfer Active This status is used for detecting completion of a read transfer. This bit is set to 1 for either of the following conditions: (1) After the end bit of the readcommand. (2) When read operation is restarted by writing 1 to CR2_CONTREQ. This bit is cleared to 0 for either of the following conditions: (1) When the last data block as specified by block length is transferred to the System. (2) In case of ADMA, end of read operation is designated by Descriptor Table. (3) When all valid data blocks in the Controller have been transferred to the System and no current block transfers are being sent as a result of CR2_BLKGAPSTOP being set to 1. A Transfer Complete interrupt is generated when this bit changes to 0.
[8]	r	1'h0	WACTIVE	Write Transfer Active This status indicates a write transfer is active. If this bit is 0, it means no valid write data exists in the Controller. This bit is set in either of the following cases: After the end bit of the write command. When write operation is restarted by writing 1 to CR2_CONTREQ. This bit is cleared in either of the following cases: After getting the CRC status of the last data block as specified by the transfer count (Single and Multiple) In case of ADMA, transfer count is designated by Descriptor Table. After getting the CRC status of any block where data transmission is about to be stopped by CR2_BLKGAPSTOP. During a write transaction, ISR_BLKGAP is generated when this bit is changed to 0, as the result of CR2_BLKGAPSTOP begin set. This status is useful for the Host Driver in determining non DAT line commands can be issued during write busy.
[7:3]			RSVD	

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表 14-4: SDMMC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[2]	r	1'h0	DATACTIVE	DAT Line Active This bit indicates whether one of the DAT line on SD Bus is in use. (a) In the case of read transactions This status indicates whether a read transfer is executing on the SD Bus. Changing this value from 1 to 0 generates ISR_BLKGAP, as the result of CR2_BLKGAPSTOP being set. This bit shall be set in either of the following cases: (1) After the end bit of the read command. (2) When writing 1 to CR2_CONTREQ to restart a read transfer. This bit shall be cleared in either of the following cases (1) When the end bit of the last data block is sent from the SD Bus to the Controller. In case of ADMA, the last block is designated by the last transfer of Descriptor Table. (2) When a read transfer is stopped at the block gap initiated by CR2_BLKGAPSTOP. The Controller shall stop read operation at the start of the interrupt cycle of the next block gap by driving Read Wait or stopping SD clock. If the Read Wait signal is already driven (due to data buffer cannot receive data), the Controller can continue to stop read operation by driving the Read Wait signal. It is necessary to support Read Wait in order to use suspend / resume function. (b) In the case of write transactions This status indicates that a write transfer is executing on the SD Bus. Changing this value from 1 to 0 generate ISR_TC. This bit shall be set in either of the following cases: (1) After the end bit of the write command. (2) When writing 1 to CR2_CONTREQ to continue a write transfer. This bit shall be cleared in either of the following cases: (1) When the SD card releases write busy of the last data block. If SD card does not drive busy signal for 8 SD Clocks, the Controller shall consider the card drive "Not Busy". In case of ADMA, the last block is designated by the last transfer of Descriptor Table. (2) When the SD card releases write busy prior to waiting for write transfer as a result of CR2_BLKGAPSTOP. (c) Command with busy This status indicates whether a command indicates busy (ex. erase command for memory) is executing on the SD Bus. This bit is set after the end bit of the command with busy and cleared when busy is de-asserted. Changing this bit from 1 to 0 generate ISR_TC.
[1]	r	1'h0	DATBUSY	Command Inhibit (DAT) This status bit is generated if either the DAT Line Active or the Read Transfer Active is set to 1. If this bit is 0, it indicates the Controller can issue the next SD Command. Commands with busy signal belong to Command Inhibit (DAT) (ex. R1b, R5b type). Changing from 1 to 0 generates ISR_TC interrupt. 1 Cannot issue command which uses the DAT line 0 Can issue command which uses the DAT line

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表 14-4: SDMMC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[0]	r	1'h0	CMDBUSY	Command Inhibit (CMD) If this bit is 0, it indicates the CMD line is not in use and the Controller can issue a SD Command using the CMD line. This bit is set immediately after CR1 is written. This bit is cleared when the command response is received. Auto CMD12 and Auto CMD23 consist of two responses. In this case, this bit is not cleared by the response of CMD12 or CMD23 but cleared by the response of a read/write command. Status issuing Auto CMD12 is not read from this bit. So if a command is issued during Auto CMD12 operation, Controller shall manage to issue two commands: CMD12 and a command set by CR1. Even if the DATBUSY is set to 1, commands using only the CMD line can be issued if this bit is 0. Changing from 1 to 0 generates ISR_CC Interrupt. If the Controller cannot issue the command because of a command conflict error or because of Command Not Issued By Auto CMD12 Error, this bit shall remain 1 and the Command Complete is not set. 1 Cannot issue command 0 Can issue command using only CMD line
0x28			**CR2**	Control Register 2
[31:20]			RSVD	
[19]	rw	1'h0	BLKGAPIE	Interrupt At Block Gap This bit is valid only in 4-bit mode of the SDIO card and selects a sample point in the interrupt cycle. Setting to 1 enables interrupt detection at the block gap for a multiple block transfer. Setting to 0 disables interrupt detection during a multiple block transfer. If the SD card cannot signal an interrupt during a multiple block transfer, this bit should be set to 0. The Host Driver shall set this bit according to the CCCR of the SDIO card.
[18]	rw	1'h0	RWAITEN	Read Wait Control The read wait function is optional for SDIO cards. If the card supports read wait, set this bit to enable use of the read wait protocol to stop read data using the DAT2 line. Otherwise, the Controller has to stop the SD Clock to hold read data, which restricts commands generation. The Host Driver shall set this bit according to the CCCR of the SDIO card. If the card does not support read wait, this bit shall never be set to 1 otherwise DAT line conflict may occur. If this bit is set to 0, Suspend/Resume cannot be supported.
[17]	rw	1'h0	CONTREQ	Continue Request
[16]	rw	1'h0	BLKGAPSTOP	Stop At Block Gap request This bit is used to stop executing read and write transaction at the next block gap for non-DMA, SDMA and ADMA transfers. The Host Driver shall leave this bit set to 1 until the Transfer Complete is set to 1. Clearing both Stop At Block Gap Request and Continue Request shall not cause the transaction to restart. The Controller shall stop read transfer by using Read Wait or stopping SD clock. In case of write transfers in which the Host Driver writes data to the Buffer Data Port register, the Host Driver shall set this bit after all block data is written. If this bit is set to 1, the Host Driver shall not write data to BUF. 1 Stop 0 Transfer
[15:13]			RSVD	

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表 14-4: SDMMC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[12]	rw	1'h1	PPMODE	CMD line output mode. Open drain mode should only be used when accessing eMMC device. 1 Push Pull Mode 0 Open Drain Mode
[11:6]			RSVD	
[5]	rw	1'h0	EXTWIDTH	Extended Data Transfer Width 1 8-bit Bus Width 0 Bus Width is Selected by DATAWIDTH
[4:3]	rw	2'h0	DMAMODE	DMA Select One of supported DMA modes can be selected. DMA mode is enabled by CR1_DMAEN. 00b SDMA 01b Reserved 10b ADMA 11b Reserved
[2]	rw	1'h0	HSMODE	Reserved for debug. Adjust output timing of CMD line and DAT lines.
[1]	rw	1'h0	DATWIDTH	Data Transfer Width This bit selects the data width of the Controller when EXTWIDTH is 0. The Host Driver shall set it to match the data width of the SD card. 1 4-bit mode 0 1-bit mode
[0]			RSVD	
0x2C			**CR3**	Control Register 3
[31:27]			RSVD	
[26]	rw	1'h0	RSTDAT	Software Reset For DAT Line Only part of data circuit is reset. DMA circuit is also reset. Will be cleared automatically. Because it takes some time to complete software reset, the SD Host Driver shall confirm that these bits are 0.
[25]	rw	1'h0	RSTCMD	Software Reset For CMD Line Only part of command circuit is reset. Will be cleared automatically. Because it takes some time to complete software reset, the SD Host Driver shall confirm that these bits are 0.
[24]	rw	1'h0	RST	This reset affects the entire Controller except for the card detection circuit. Register bits (except read-only bits) are cleared to 0. During its initialization, the Host Driver shall set this bit to 1 to reset the Controller. If this bit is set to 1, the host driver should issue reset command and reinitialize the SD card. Will be cleared automatically. Because it takes some time to complete software reset, the SD Host Driver shall confirm that these bits are 0.
[23:20]			RSVD	
[19:16]	rw	4'he	DTOCNT	Data Timeout Counter Value This value determines the interval by which DAT line timeouts are detected. Timeout period is defined as: 1111b Reserved 1110b 4096*214 FCLK periods .... 0001b 4096*21 FCLK periods 0000b 4096*2 FCLK periods

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表 14-4: SDMMC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[15:8]	rw	8'h0	CLKDIVL	CLK divider lower 8 bits 10-bit CLKDIV is CLKDIVU,CLKDIVL. If CLKDIV=0, CLK = FCLK. If CLKDIV!=0, CLK = FCLK/(2*CLKDIV). e.g. FCLK=192MHz, CLKDIV=240, then CLK frequency is 400KHz.
[7:6]	rw	2'h0	CLKDIVU	CLK divider upper 2 bits These bits expand clk divider to 10-bit.
[5:3]			RSVD	
[2]	rw	1'h0	CLKEN	SD Clock Enable 0: SD clock disabled 1: SD clock enabled
[1]			RSVD	
[0]	rw	1'h0	INTCLKEN	Internal Clock Enable 0: Internal clock disabled 1: Internal clock enabled
0x30			**ISR**	Interrupt State Register
[31:26]			RSVD	
[25]	rw1c	1'h0	ADMAERR	ADMA Error This bit is set when the Controller detects errors during ADMA based data transfer. The state of the ADMA at an error occurrence is saved in the AESR, In addition, the Controller generates this Interrupt when it detects invalid descriptor data (Valid=0). ADMA Error State in the ADMA Error Status indicates that an error occurs. The Host Driver may find that Valid bit is not set at the error descriptor.
[24]	rw1c	1'h0	ACERR	Auto CMD Error Auto CMD12 and Auto CMD23 use this error status. In case of Auto CMD12, this bit is set to 1, not only when the errors in Auto CMD12 occur but also when Auto CMD12 is not executed due to the previous command error.
[23]			RSVD	
[22]	rw1c	1'h0	DEBERR	Data End Bit Error Occurs either when detecting 0 at the end bit position of read data which uses the DAT line or at the end bit position of the CRC Status.
[21]	rw1c	1'h0	DCRCERR	Data CRC Error Occurs when detecting CRC error when transferring read data which uses the DAT line or when detecting the Write CRC status having a value of other than "010".
[20]	rw1c	1'h0	DTOERR	Data Timeout Error This bit is set when detecting one of following timeout conditions. Busy timeout for R1b,R5b type Busy timeout after Write CRC status Write CRC Status timeout Read Data timeout.
[19]	rw1c	1'h0	IDXERR	Command Index Error This bit is set if a Command Index error occurs in the command response.
[18]	rw1c	1'h0	CEBERR	Command End Bit Error This bit is set when detecting that the end bit of a command response is 0.

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表 14-4: SDMMC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[17]	rw1c	1'h0	CCRCERR	Command CRC Error Command CRC Error is generated in two cases. If a response is returned and the Command Timeout Error is set to 0 (indicating no timeout), this bit is set to 1 when detecting a CRC error in the command response. The Controller detects a CMD line conflict by monitoring the CMD line when a command is issued. If the Controller drives the CMD line to 1 level, but detects 0 level on the CMD line at the next SD clock edge, then the Controller shall abort the command (Stop driving CMD line) and set this bit to 1. The Command Timeout Error shall also be set to 1 to distinguish CMD line conflict
[16]	rw1c	1'h0	CTOERR	Command Timeout Error This bit is set only if no response is returned within 64 SD clock cycles from the end bit of the command. If the Controller detects a CMD line conflict, in which case Command CRC Error shall also be set, this bit shall be set without waiting for 64 SD clock cycles because the command will be aborted by the Controller.
[15]	r	1'h0	ERR	Error Interrupt If any error bit (bit16~bit31) of ISR are set, then this bit is set. Therefore the Host Driver can efficiently test for an error by checking this bit first. This bit is read only.
[14:9]			RSVD	
[8]	r	1'h0	CARD	Card Interrupt Writing this bit to 1 does not clear this bit. It is cleared by resetting the SD card interrupt factor. In 4-bit mode, the card interrupt signal is sampled during the interrupt cycle, so there are some sample delays between the interrupt signal from the SD card and the interrupt to the Host System. When this status has been set and the Host Driver needs to start this interrupt service, ISER_CARDEN may be set to 0 in order to clear the card interrupt statuses latched in the Controller and to stop driving the interrupt signal to the Host System. After completion of the card interrupt service (It should reset interrupt factors in the SD card and the interrupt signal may not be asserted), set ISER_CARDEN to 1 and start sampling the interrupt signal again.
[7:6]			RSVD	
[5]	rw1c	1'h0	BUFRRDY	Buffer Read Ready This status is set if the Buffer Read Enable changes from 0 to 1. Refer to SR_BUFREN register. 1 Ready to read buffer 0 Not ready to read buffer
[4]	rw1c	1'h0	BUFWRDY	Buffer Write Ready This status is set if the Buffer Write Enable changes from 0 to 1. Refer to SR_BUFWEN register. 1 Ready to write buffer 0 Not ready to write buffer
[3]	rw1c	1'h0	DMA	DMA Interrupt This status is set if the Controller detects the Host SDMA Buffer boundary during transfer. Refer to BSR_SDMABDY. In case of ADMA, by setting INT field in the descriptor table, Controller generates this interrupt. This interrupt shall not be generated after the Transfer Complete.

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表 14-4: SDMMC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[2]	rw1c	1'h0	BLKGAP	Block Gap Event If CR2_BLKGAPSTOP is set, this bit is set when both a read / write transaction is stopped at a block gap. If CR2_BLKGAPSTOP is not set to 1, this bit is not set to 1. (1) In the case of a Read Transaction This bit is set at the falling edge of the DAT Line Active Status (When the transaction is stopped at SD Bus timing. The Read Wait shall be supported in order to use this function. (2) Case of Write Transaction This bit is set at the falling edge of Write Transfer Active Status (After getting CRC status at SD Bus timing). 1 Transaction stopped at block 0 No Block Gap Event
[1]	rw1c	1'h0	TC	Transfer Complete This bit is set when a read / write transfer and a command with busy is completed. (1) In the case of a Read Transaction This bit is set at the falling edge of Read Transfer Active Status. This interrupt is generated in two cases. The first is when a data transfer is completed as specified by data length (After the last data has been read to the Host System). The second is when data has stopped at the block gap and completed the data transfer by setting CR2_BLKGAPSTOP (After valid data has been read to the Host System). (2) In the case of a Write Transaction This bit is set at the falling edge of the DAT Line Active Status. This interrupt is generated in two cases. The first is when the last data is written to the SD card as specified by data length and the busy signal released. The second is when data transfers are stopped at the block gap by setting CR2_BLKGAPSTOP and data transfers completed. (After valid data is written to the SD card and the busy signal released). (3) In the case of a command with busy This bit is set when busy is de-asserted. Refer to SR_DATACTIVE and SR_CMDBUSY. Transfer Complete has higher priority than Data Timeout Error. If both bits are set to 1, execution of a command can be considered to be completed.
[0]	rw1c	1'h0	CC	Command Complete This bit is set when get the end bit of the command response. Auto CMD12 and Auto CMD23 consist of two responses. Command Complete is not generated by the response of CMD12 or CMD23 but generated by the response of a read/write command. Command Timeout Error has higher priority than Command Complete. If both bits are set to 1, it can be considered that the response was not received correctly.
0x34			**ISER**	Interrupt Status Enable Register
[31:26]			RSVD	
[25]	rw	1'h0	ADMAERREN	ADMA Error Status Enable
[24]	rw	1'h0	ACERREN	Auto CMD Error Status Enable
[23]			RSVD	
[22]	rw	1'h0	DEBERREN	Data End Bit Error Status Enable
[21]	rw	1'h0	DCRCERREN	Data CRC Error Status Enable
[20]	rw	1'h0	DTOERREN	Data Timeout Error Status Enable
[19]	rw	1'h0	IDXERREN	Command Index Error Status Enable

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表 14-4: SDMMC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[18]	rw	1'h0	CEBERREN	Command End Bit Error Status Enable
[17]	rw	1'h0	CCRCERREN	Command CRC Error Status Enable
[16]	rw	1'h0	CTOERREN	Command Timeout Error Status Enable
[15:9]			RSVD	
[8]	rw	1'h0	CARDEN	Card Interrupt Status Enable If this bit is set to 0, the Controller shall clear interrupt request to the System. The Card Interrupt detection is stopped when this bit is cleared and restarted when this bit is set to 1. The Host Driver may clear the Card Interrupt Status Enable before servicing the Card Interrupt and may set this bit again after all interrupt requests from the card are cleared to prevent inadvertent interrupts.
[7:6]			RSVD	
[5]	rw	1'h0	BUFRRDYEN	Buffer Read Ready Status Enable
[4]	rw	1'h0	BUFWRDYEN	Buffer Write Ready Status Enable
[3]	rw	1'h0	DMAEN	DMA Interrupt Status Enable
[2]	rw	1'h0	BLKGAPEN	Block Gap Event Status Enable
[1]	rw	1'h0	TCEN	Transfer Complete Status Enable
[0]	rw	1'h0	CCEN	Command Complete Status Enable
0x38			**IER**	Interrupt Enable Register
[31:26]			RSVD	
[25]	rw	1'h0	ADMAERRIE	ADMA Error Interrupt Enable
[24]	rw	1'h0	ACERRIE	Auto CMD Error Interrupt Enable
[23]			RSVD	
[22]	rw	1'h0	DEBERRIE	Data End Bit Error Interrupt Enable
[21]	rw	1'h0	DCRCERRIE	Data CRC Error Interrupt Enable
[20]	rw	1'h0	DTOERRIE	Data Timeout Error Interrupt Enable
[19]	rw	1'h0	IDXERRIE	Command Index Error Interrupt Enable
[18]	rw	1'h0	CEBERRIE	Command End Bit Error Interrupt Enable
[17]	rw	1'h0	CCRCERRIE	Command CRC Error Interrupt Enable
[16]	rw	1'h0	CTOERRIE	Command Timeout Error Interrupt Enable
[15:9]			RSVD	
[8]	rw	1'h0	CARDIE	Card Interrupt Interrupt Enable If this bit is set to 0, the Controller shall clear interrupt request to the System. The Card Interrupt detection is stopped when this bit is cleared and restarted when this bit is set to 1. The Host Driver may clear the Card Interrupt Status Enable before servicing the Card Interrupt and may set this bit again after all interrupt requests from the card are cleared to prevent inadvertent interrupts.
[7:6]			RSVD	
[5]	rw	1'h0	BUFRRDYIE	Buffer Read Ready Interrupt Enable
[4]	rw	1'h0	BUFWRDYIE	Buffer Write Ready Interrupt Enable
[3]	rw	1'h0	DMAIE	DMA Interrupt Interrupt Enable
[2]	rw	1'h0	BLKGAPIE	Block Gap Event Interrupt Enable
[1]	rw	1'h0	TCIE	Transfer Complete Interrupt Enable
[0]	rw	1'h0	CCIE	Command Complete Interrupt Enable
0x3C			**CR4**	Control Register 4
[31:19]			RSVD	
[18:16]	rw	3'h0	UHSMODE	UHS Mode Select 100b DDR others SDR

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表 14-4: SDMMC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[15:8]			RSVD	
[7]	r	1'h0	CNIERR	Command Not Issued By Auto CMD12 Error Setting this bit to 1 means CMD_wo_DAT is not executed due to an Auto CMD12 Error in this register. This bit is set to 0 when Auto CMD Error is generated by Auto CMD23. 1 Not Issued 0 No Error
[6:5]			RSVD	
[4]	r	1'h0	ACIDXERR	Auto CMD Index Error This bit is set if the Command Index error occurs in response to a command
[3]	r	1'h0	ACEBERR	Auto CMD End Bit Error This bit is set when detecting that the end bit of command response is 0.
[2]	r	1'h0	ACCRCERR	Auto CMD CRC Error This bit is set when detecting a CRC error in the command response.
[1]	r	1'h0	ACTOERR	Auto CMD Timeout Error This bit is set if no response is returned within 64 SDCLK cycles from the end bit of command. If this bit is set to1, the other error status bits are meaningless.
[0]	r	1'h0	ACNE	Auto CMD12 Not Executed If memory multiple block data transfer is not started due to command error, this bit is not set because it is not necessary to issue Auto CMD12. Setting this bit to 1 means the Controller cannot issue Auto CMD12 to stop memory multiple block data transfer due to some error. If this bit is set to 1, other error status bits are meaningless. This bit is set to 0 when Auto CMD Error is generated by Auto CMD23. 1 Not Executed 0 Executed
0x54			**AESR**	ADMA Error Status Register
[31:3]			RSVD	
[2]	r	1'h0	LENERR	ADMA Length Mismatch Error This error occurs in the following 2 cases. (1) While CR1_BCNTEN being set, the total data length specified by the Descriptor table is different from that specified by the Block Count and Block Length. (2) Total data length cannot be divided by the block length.
[1:0]	r	2'h0	ERRSTATE	ADMA Error State This field indicates the state of ADMA when error is occurred during ADMA data transfer. This field never indicates "10" because ADMA never stops in this state. 00 ST_STOP (Stop DMA) Points next of the error descriptor 01 ST_FDS (Fetch Descriptor) Points the error descriptor 10 Never set this state (Not used) 11 ST_TFR (Transfer Data) Points the next of the error descriptor
0x58			**ASAR**	ADMA System Address Register

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表 14-4: SDMMC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:0]	rw	32'h0	ADDR	ADMA System Address This register holds byte address of executing command of the Descriptor table. At the start of ADMA, the Host Driver shall set start address of the Descriptor table. The ADMA increments this register address, which points to next line, when every fetching a Descriptor line. When the ADMA Error Interrupt is generated, this register shall hold valid Descriptor address depending on the ADMA state. The Host Driver shall program Descriptor Table on 32-bit boundary and set 32-bit boundary address to this register. Lower 2-bit of this register is ignored and assumes it to be 00b.
0x5C			**NSAR**	Next System Address Register
[31:0]	r	32'h0	ADDR	This register contains next physical system memory address used for SDMA transfer. When the Host Controller stops a SDMA transfer, this register shall point to the system address of the next contiguous data position. It can be accessed only if no transaction is executing (i.e., after a transaction has stopped). Read operations during transfers may return an invalid value. After SDMA has stopped, the next system address of the next contiguous data position can be read from this register.
0xEC			**ABSR**	AHB Burst Size Register
[31:7]			RSVD	
[6:0]	rw	7'h7	BSIZE	AHB Master Burst Size Register AHB Master performs Burst operations as per this register. 0:Disabled 1:Enabled Bit 00 INCR4 Bit 01 INCR8 Bit 02 INCR16 Bit 03 INCR Bit 04 WRAP4 Bit 05 WRAP8 Bit 06 WRAP16
0xF4			**SCR**	Sampling Clock Register
[31:8]			RSVD	
[7]	rw	1'h0	SEL	select sampling clock source (delay line input) 0: use internal clock 1: use loopback clock
[6]			RSVD	
[5:0]	rw	6'h0	DLY	Stages of delay line for sampling clock

14.2 SDMMC2

14.2.1 简介

SDMMC 支持 SD 协议 3.0 以及 eMMC 标准 4.51，可作为 HOST 控制器与 SD/SDIO/eMMC 设备交互，并与 DMAC 配合进行数据读写。SDMMC 支持 SDR 单线和 4 线模式，不支持 DDR，不支持 SPI 模式。

14.2.2 主要特性

- 兼容 SD Host Controller Standard Specification Version 3.0

- 兼容 SD 3.0 Physical Layer Specification Version 3.01
- 兼容 SDIO Specification Version 3.0
- 兼容 JEDEC JESD84-B451 eMMC 4.51 Specification
- 支持 SDSC/SDHC/SDXC/SDHS 卡
- 支持 SDR12/SDR25/SDR50
- 支持 SDR 单线、4 线模式
- 内置 2K 字节 FIFO，最大支持单 block 512 字节
- 可配置时钟
- 配合 DMAC 进行数据搬运

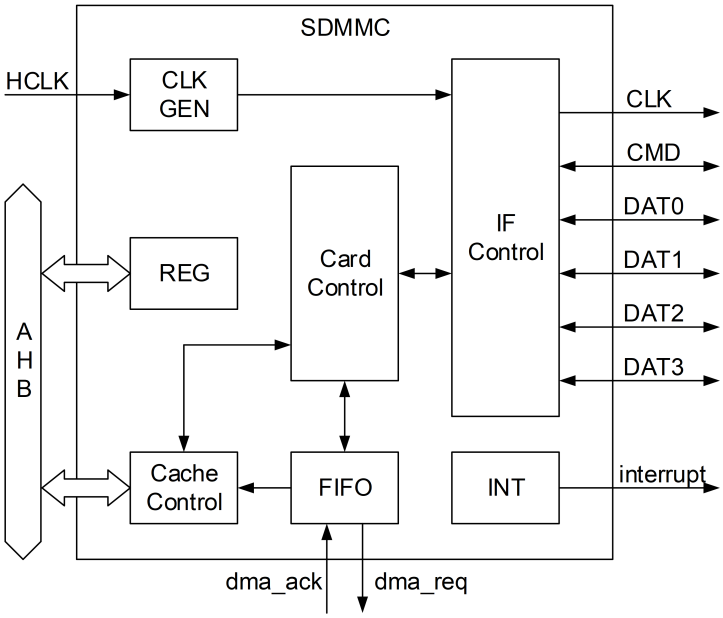

图 14-3: SDMMC 结构图

14.2.3 功能描述

14.2.3.1 SD/eMMC 接口

控制器支持的 SD/eMMC 接口共包括一根 CLK 线，一根 CMD 线和 4 根 DAT 线 (DAT0-DAT3)。单线模式下 DAT 线仅使用一根 (DAT0)。CLK 线用于输出时钟。CMD 线依照协议打包传输 CMD 命令以及应答 RSP。DAT 线依照协议传输数据流。本模块仅支持单边沿 (SDR) 传输，CMD 与 DAT 仅在 CLK 的上升沿有效。

14.2.3.2 时钟设置

控制器工作在系统时钟 HCLK 频率上。输出到 SD/eMMC 接口的 CLK 是由 HCLK 分频产生，分频比由 CLKCR_DIV 指定。分频公式为 CLK 频率 =HCLK 频率/(CLKCR_DIV+1)。例如当 HCLK 为 48M，要输出 400KHz 的 CLK，就需要将 CLKCR_DIV 配置成 119。CLKCR_DIV 最小支持设置为 1，即分频比至少为 2。

CLK 输出由 CLKCR_STOP_CLK 控制，设置为 0 以后时钟会持续输出，设置为 1 关闭输出。

14.2.3.3 发送命令

命令是由控制器通过 CMD 线发送，由 SD/eMMC/SDIO 设备接收的固定格式的包，用于配置 SD/eMMC/SDIO 设备的状态，并控制数据的传输。命令的包长度固定为 48bit。

命令包格式						
Bit position	47	46	[45:0]	[39:8]	[7:1]	0
Width(bits)	1	1	6	32	7	1
Value	0	1	x	x	x	1
Description	Start bit	Transimission bit	Command index	Argument	CRC7	End bit

每条命令通过 6bit 的命令编号区分不同功能，并附带 32bit 的参数。设备通过 7bit CRC 判断接收到的命令是否正确，并在需要回复时发送响应。

根据 6bit 的命令编号，命令通常被命名为 CMDn，其中 n 就是命令编号，由 CCR_CMD_INDEX 寄存器配置。

命令的 32bit 参数由 CAR 寄存器配置。

某些命令如 CMD0，CMD4 等不需要接收响应；某些命令如 CMD8,CMD11 等需要接收 48bit 的响应；某些命令如 CMD2 需要接收 136bit 的响应。发送命令前，需要通过配置 CCR_CMD_HAS_RSP 和 CCR_CMD_LONG_RSP 寄存器选择命令期望的响应。

响应配置				
响应	CMD 示例	RSP 示例	CCR_CMD_HAS_RSP	CCR_CMD_LONG_RSP
无	CMD0，CMD4	无	0	0
48bit	CMD8，CMD11	R1,R7	1	0
136bit	CMD2，CMD9	R2	1	1

控制器每次发送命令前，需要将命令的各项配置完成，并置位 CCR_CMD_TX_EN，随后置位 CMD_START，控制器就会启动命令发送流程。

命令发送流程有两种结束方式：

1. 命令完成，SR_CMD_DONE 拉高，且当 IER_CMD_DONE_MASK 为 1 时可产生中断。当命令发送完成且不需要接收响应，或者在超时时间以内接收到响应，不论响应的 CRC 是否正确，均会完成命令。如果接收响应出现 CRC 错误，SR_CMD_RSP_CRC 会拉高，且当 IER_CMD_RSP_CRC_MASK 为 1 时可产生中断。

2. 命令超时，SR_CMD_TIMEOUT 拉高，且当 IER_CMD_TIMEOUT_MASK 为 1 时可产生中断。当命令发送完成且需要接收响应，但在 TOR 寄存器配置的超时时间以内没有接收到响应 (未收到响应的 start bit)，会产生超时。一旦发生命令超时，控制器在发送下一条命令前需要被复位 (通过 RCC 模块)，并恢复配置 (仅需重新配置 SDMMC 控制器，与设备交互的状态不需改变)。

通过 SR_CMD_BUSY 可以查询命令发送流程是否完成。当前一条命令发送流程未结束时，控制器不响应新的命令发送请求。调试过程中，如果发现 SR_CMD_BUSY 长时间不拉低，请检查 TOR 设置是否合理，并检查上一条命令超时以后是否进行了控制器复位和重配置操作。

某些命令在期望响应 (如 R1b) 时，还需要检查设备通过 DAT 线反馈的 busy 状态，可以通过查询 DSR 寄存器判断 busy 是否撤销。

控制器接收到响应的 command index 保存在 RIR 寄存器中，argument 保存在 RAR1 RAR4 中，其中 48bit 响应的 argument 保存在 RAR1 中。

命令发送的建议流程：1. 配置 index，argument 以及期望响应类型，启动命令发送
2. 等待命令完成中断或命令超时中断
3. 如果命令完成，检查返回的响应并获取 argument
4. 如果命令超时，复位控制器并重新配置 (主要包括时钟设置和超时时间等)。

14.2.3.4 数据传输

数据传输包括从设备读取数据和向设备写入数据，由控制器发送特定命令 (如 CMD17，CMD24 等) 启动，数据传输预设长度后结束，或由控制器发送特定命令 (如 CMD12) 结束。

SD 和 SDIO 协议定义的数据传输可采用单线或 4 线模式。eMMC 协议定义的数据传输可采用单线，4 线或 8 线模式。本控制器只支持单线或 4 线传输，通过 DCR_WIRE_MODE 寄存器配置。单线模式下，数据通过 DAT0 传输，DAT0 也同时用于表示数据传输的 busy 状态。4 线模式下，数据通过 DAT0~DAT3 传输，DAT0 也同时用于表示数据传输的 busy 状态。

数据采用分块传输的形式，每块的数据量根据设备类型有所不同。对于 SD 和 eMMC 设备，单块数据量通常为 512byte，但也有例外。某些设备允许通过命令 (如 CMD16) 改变单块数据量。控制器在开始数据传输前，应当根据单块数据量将 DCR_BLOCK_SIZE 寄存器配置成相应值 (单块数据字节数等于 DCR_BLOCK_SIZE 加 1)。控制器还需配置 DLR_DATA_LEN 寄存器来确定单次数据传输的总量 (总字节数等于 DLR_DATA_LEN 加 1)。对于单块传输，DLR_DATA_LEN 应等于 DCR_BLOCK_SIZE。对于多块传输，(DLR_DATA_LEN+1) 应当为 (DCR_BLOCK_SIZE+1) 的整数倍。

数据传输的方向由 DCR_R_WN 配置。DCR_TRAN_DATA_EN 寄存器是数据传输使能，在传输过程中应当保持为高。DCR_DATA_START 用于启动数据传输。

数据传输需经过控制器内部的 FIFO 缓存。待发送的数据由 CPU 或 DMA 向 FIFO 写入，随后控制器再将 FIFO 中的数据写入到设备。从设备读取的数据也暂存在 FIFO 中，再由 CPU 或 DMA 取出。FIFO 的寄存器地址空间共占据 512byte，访问其中任何一个 word 对齐的地址效果相同。如果 FIFO 发生了上溢出或下溢，会产生 SR_FIFO_OVERRUN 或 SR_FIFO_UNDERRUN 记录，并可产生中断。

数据传输有可能正常结束，也可能在规定时间内未收到数据或 CRC 而产生超时。不论发生哪种情况，SR_DATA_DONE 都会拉高，并可产生中断。如果读设备时读取 CRC 错误，或者写设备时，设备返回了 CRC 错误，都会产生 SR_DATA_CRC 记录。如果读设备时在 TOR 配置的超时时间内未检测到数据起始位，或写设备时在 TOR 配置的超时时间内未收到设备返回的 CRC 响应，都会产生 SR_DATA_TIMEOUT 记录。

通过 SR_DATA_BUSY 可以查询数据传输是否完成。当前一次数据传输未结束时，控制器不响应新的数据传输请求。

数据读取的建议流程：1. 配置单块数据量和总数据量，启动数据读取
2. 配置 DMAC 为读取 FIFO，并启动 DMAC
3. 发送读命令 (如 CMD17)
4. 等待命令中断，处理设备响应 (如 R1)
5. 等待数据传输完成中断
6. 如果是多块读取，发送传输结束命令 (如 CMD12)

7. 等待 DMA 完成中断

数据写入的建议流程：1. 发送写命令 (如 CMD24)
2. 等待命令中断，处理设备响应 (如 R1)
3. 配置单块数据量和总数据量，启动数据写入
4. 配置 DMAC 为写入 FIFO，并启动 DMAC
5. 等待数据传输完成中断
6. 如果是多块写入，发送传输结束命令 (如 CMD12)

14.2.3.5 中断产生

SDMMC 能够产生中断，用于通知 CPU 特定事件发生。这些事件包括命令发送完成，命令超时，数据完成，数据超时，以及各种错误等。能够产生中断的事件通过 IER 寄存器配置。发生的事件通过 SR 寄存器查询。

14.2.3.6 FIFO 管理

SDMMC 内置 2KB 大小的 FIFO 用于缓存读写数据。FIFO 能够根据内容的空满情况产生 DMA 请求，与 DMAC 配合完成数据搬运。在多块数据传输时，DMAC 搬运数据的带宽通常能够满足设备数据传输的带宽，因此能够持续进行数据传输。但如果 DMAC 搬运的另一端存储空间发生了堵塞，导致没有及时响应 FIFO 的请求，就可能使得 FIFO 产生 overflow 或 underflow，数据传输出错。为避免这种情况发生，可以设置 CLKCR_VOID_FIFO_ERROR 寄存器，使得当 FIFO 内容无法满足数据传输要求时，自动停止接口 CLK，并停止数据传输，直到 FIFO 内容满足要求为止，此时会在接口上观察到 CLK 的暂停。

14.2.3.7 eMMC 开漏模式

当 eMMC 设备处于某些状态 (如 inactive，idle，identification 状态，详见 eMMC 协议) 时，CMD 线需要配置成开漏模式，通过将 CDR_CMD_OD 配置成 1 实现。

当访问 SD/SDIO 设备时，以及当 eMMC 进入其它状态时，需要将 CMD 线配置成推挽模式，即 CDR_CMD_OD 配置成 0。

14.2.3.8 SDIO 中断

SDIO 设备可以通过拉低 DAT1 产生 SDIO 中断通知控制器。

如果控制器需要响应 SDIO 中断，单线模式下需要将 CEATA_ENABLE_SDIO_IRQ 寄存器配置为 1。4 线模式下需要额外将 CEATA_SDIO_4WIRES_IRQ 配置为 1。

14.2.3.9 卡片检测

SD 卡支持热拔插。卡片的插入与弹出检测通常有以下 3 种方式实现。

1. 通过专用 CD(card detect) 管脚检测。支持插入检测的 SD 卡槽通常提供一个专用的卡片检测管脚 (CD)，该管脚与电源间存在上拉电阻。芯片需要分配一个独立 IO 用于检测该管脚电平。当没有插入 SD 卡时，该管脚电平为高。当 SD 卡片插入卡槽时，该管脚与地导通，电平为低。通过判断该 IO 的 GPIO 输入电平，可以实现 SD 卡的插入与弹出检测。

2. 通过 DAT3 管脚检测。SD 卡上电时，卡片内部的 DAT3 到电源有 50K 欧姆的上拉电阻。芯片外部电路需要在

DAT3 管脚上放置到地的弱下拉电阻 (通常需大于 470K 欧姆)。芯片通过检测与 DAT3 相连接的 IO 电平，判断卡片是否插入。当没有插入 SD 卡时，该管脚电平为低。当 SD 卡片插入卡槽时，该管脚被上拉到高电平。通过判断该 IO 的 GPIO 输入电平，可以实现 SD 卡的插入与弹出检测。SD 卡启动数据传输时，应当停止该检测，将 DAT3 作为正常数据线使用。

3. 通过命令轮询检测。芯片每隔一段时间向 SD 卡发起命令交互，根据命令是否得到响应判断卡片是否存在。

SDMMC 仅支持通过 DAT3 进行卡片检测。SR_CARD_EXIST 根据 DAT3 的电平报告卡片是否存在，而卡片的插入和拔出事件通过 SR_CARD_INSERT 和 SR_CARD_REMOVE 报告，并可产生中断。

14.2.3.10 总线直接读取模式

SDMMC 允许将 SD 卡的数据空间映射到 AHB 总线上，使得其它主控模块能够通过 AHB 总线直接访问地址的方式读取 SD 卡的数据。在使用这个功能前，SDMMC 需要首先将 SD 卡配置进入数据传输模式。随后当总线上有对映射空间的读访问时，SDMMC 自动向 SD 卡发出命令并读取多块数据，将数据保存在内置缓存内 (与 FIFO 共享存储空间)，并通过总线返回数据。如果后续总线要读取的数据位于缓存内，SDMMC 不会发起新的读取命令，而是直接返回缓存内的结果。

14.2.3.11 采样时钟调节

SDMMC 与设备通信时，需要在 CLK 的上升沿采样从设备输入的 CMD 与 DAT 信号。由于信号传输存在时延，可能需要调节采样时钟的边沿以保证采样正确。CLKCR_CLK_TUNE_SEL 寄存器可以用来向后调节采样时钟的边沿，共有 4 档，可根据产品的实际情况调整。当 CLK 频率大于 50M 时，往往需要调节采样时钟以保证接口功能正确。

14.2.4 SDMMC 寄存器

表 14-5: SDMMC 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00			**SR**	command and data status register
[31:18]			RSVD	
[17]	rw	1'h0	cache_err	Detect cache error Read 1: cache error occur Read 0: no cache error Write 1: clear the bit Write 0: no any influence to the bit
[16]	rw	1'h0	sdio	Detect SDIO Card Interrupt Read 1: detect sdio card generating interrupt Read 0: no interrupt Write 1: clear the bit Write 0: no any influence to the bit
[15]	r	1'h0	card_exist	Card exist status Read 1: card exist Read 0: no card exist This bit will be valid after enable detect card.

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表 14-5: SDMMC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[14]	rw	1'h0	card_remove	Detect card removed Read 1: detect card removed. When detect card inserted bit is set, the bit will also be back to 0 Read 0: no meaning Write 1: clear the bit Write 0: no any influence to the bit
[13]	rw	1'h0	card_insert	Detect card inserted Read 1: detect card inserted. When detect card removed bit is set, the bit will also be back to 0 Read 0: no meaning Write 1: clear the bit Write 0: no any influence to the bit
[12]	rw	1'h0	cmd_sent	Command sent (perhaps no response back yet) Read 1: command sent. When command start bit is set, the bit will also be back to 0 Read 0: command transferring or others Write 1: clear the bit Write 0: no any influence to the bit
[11]			RSVD	
[10]	rw	1'h0	fifo_overrun	FIFO overrun Read 1: FIFO overrun error Read 0: no FIFO overrun error Write 1: clear the bit Write 0: no any influence to the bit
[9]	rw	1'h0	fifo_underrun	FIFO underrun Read 1: FIFO underrun error Read 0: no FIFO underrun error Write 1: clear the bit Write 0: no any influence to the bit
[8]	rw	1'h0	startbit_error	Wide bus start bits error Didn't detect all start bits in data bus Read 1: start bits error Read 0: no start bits error Write 1: clear the bit Write 0: no any influence to the bit
[7]	rw	1'h0	data_timeout	Data timeout Read 1: timeout Read 0: no timeout Write 1: clear the bit Write 0: no any influence to the bit
[6]	rw	1'h0	data_crc	Data CRC error Read 1: data CRC error Read 0: data CRC right Write 1: clear the bit Write 0: no any influence to the bit

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表 14-5: SDMMC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[5]	rw	1'h0	data_done	Data transfer done Read 1: transfer data done, and start a new transfer will take the bit into 0 Read 0: data transferring or idle Write 1: clear the bit Write 0: no any influence to the bit
[4]	r	1'h0	data_busy	Transfer Data busy 1: busy, and when busy, start transfer data bit is no usage and you should not modify the relative register. If want to do this, first disable transfer data enable bit, then the busy bit will be back to 0, and this transfer will also be cancelled. 0: data idle
[3]	rw	1'h0	cmd_timeout	Command timeout (response timeout) Read 1: timeout Read 0: no timeout Write 1: clear the bit Write 0: no any influence to the bit
[2]	rw	1'h0	cmd_rsp_crc	Command response CRC error status Read 1: response CRC error Read 0: response CRC right Write 1: clear the bit Write 0: no any influence to the bit
[1]	rw	1'h0	cmd_done	Command done Read 1: transfer command done, and start a new transfer will take the bit into 0 Read 0: command transferring or idle Write 1: clear the bit Write 0: no any influence to the bit
[0]	r	1'h0	cmd_busy	Command busy 1: busy, and when busy, start TX command bit is no usage and should not modify the relative register 0: command idle
0x04			**CCR**	command control register
[31:24]			RSVD	
[23:18]	rw	6'h0	cmd_index	Command index
[17]	rw	1'h0	cmd_long_rsp	1: Response will be 136-bit, long response 0: Response will be 48-bit, normal response
[16]	rw	1'h1	cmd_has_rsp	1: Response expected after command 0: No response expected after command
[15:10]			RSVD	
[9]	rw	1'h0	cmd_pend	Command pending enable When prepare to send stop command, this bit should be set. Controller will calculate a proper time point to send out the command to guarantee all the data have been transferred. And this is mainly used in stream mode. Recommend using set_block_count (SD/MMC basis command) to control transferring data for block mode. If send stop command for canceling this transfer (such as CRC error in multi-block), no need to set the bit.
[8]	rw	1'h0	cmd_tx_en	TX command enable 1: enable TX command 0: disable TX command
[7:1]			RSVD	

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表 14-5: SDMMC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[0]	rw	1'h0	cmd_start	Command start write 1 to start command TX, and when begin to TX command, the bit will return into 0.
0x08			**CAR**	command argument register
[31:0]	rw	32'h0	cmd_arg	Command argument
0x0C			**RIR**	response command index register
[31:6]			RSVD	
[5:0]	r	6'h0	rsp_index	Response command index
0x10			**RAR1**	response command argument1 register
[31:0]	rw	32'h0	rsp_arg1	Response command content If long response, it is rsp_arg[39:8]
0x14			**RAR2**	response command argument2 register
[31:0]	rw	32'h0	rsp_arg2	Long response, it is rsp_arg[71:40]
0x18			**RAR3**	response command argument3 register
[31:0]	rw	32'h0	rsp_arg3	Long response, it is rsp_arg[103:72]
0x1C			**RAR4**	response command argument4 register
[31:24]			RSVD	
[23:0]	rw	24'h0	rsp_arg4	Long response, it is rsp_arg[127:104]
0x20			**TOR**	timeout count register
[31:0]	rw	32'h1000	timeout_cnt	Used to determine how much time waiting response or data bus busy is timeout, and decreased under card clock. Set to 400000 for 1s timeout if interface clock is 400KHz.
0x24			**DCR**	data control register
[31:27]			RSVD	
[26:16]	rw	11'h1ff	block_size	Data block size is block_size+1 (max 2048 bytes) 0: 1 byte 0x1ff: 512 bytes
[15:13]			RSVD	
[12:11]	rw	2'h0	wire_mode	Wide data bus mode 00: 1 wire bus 01: 4 wires wide bus 1X: reserved
[10]	rw	1'h0	stream_mode	Data transfer mode 0: block 1: stream
[9]	rw	1'h0	r_wn	Write or read 0: write data into card 1: read data from card
[8]	rw	1'h0	tran_data_en	Transfer data enable 0: disable transfer data. After disable data transfer, stop command should be sent to card 1: enable data transfer
[7:1]			RSVD	
[0]	rw	1'h0	data_start	Start transfer data set 1 to let the controller begin to transfer data (in fact, go into wait write or wait read state). After begin to transfer, this bit will be back to 0.
0x28			**DLR**	data length register

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表 14-5: SDMMC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:16]	r	16'h0	block_tran_num	The number of blocks which have been transferred successfully 1 = 1 block transferred It is cleared when start transfer data bit is set.
[15:0]	rw	16'h1ff	data_len	Data length value. The number of data bytes is data_len+1. The number of data bytes should be a multiple of data block size. 0 is 1 byte. 0x1ff is 512 bytes. Max is 63.5KB.
0x2C			**IER**	command and data interrupt mask register
[31:18]			RSVD	
[17]	rw	1'h1	cache_err_mask	cache error mask for interrupt
[16]	rw	1'h0	sdio_mask	Detect SDIO interrupt(data[1]) mask for interrupt
[15]			RSVD	
[14]	rw	1'h0	card_remove_mask	Detect card remove mask for interrupt
[13]	rw	1'h0	card_insert_mask	Detect card insert mask for interrupt
[12]	rw	1'h0	cmd_sent_mask	Command sent mask for interrupt
[11]			RSVD	
[10]	rw	1'h1	fifo_overrun_mask	FIFO overrun bit mask for interrupt
[9]	rw	1'h1	fifo_underrun_mask	FIFO underrun bit mask for interrupt
[8]	rw	1'h0	startbit_error_mask	Wide bus start bits error bit mask for interrupt
[7]	rw	1'h1	data_timeout_mask	Data timeout bit mask for interrupt
[6]	rw	1'h1	data_crc_mask	Data CRC error bit mask for interrupt
[5]	rw	1'h1	data_done_mask	Data transfer done bit mask for interrupt
[4]			RSVD	
[3]	rw	1'h1	cmd_timeout_mask	Command timeout bit mask for interrupt
[2]	rw	1'h1	cmd_rsp_crc_mask	Command CRC error bit mask for interrupt
[1]	rw	1'h1	cmd_done_mask	Command done bit mask for interrupt
[0]			RSVD	
0x30			**CLKCR**	clock control register
[31:21]			RSVD	
[20:8]	rw	13'h80	div	Divide card clock counter. 0 is illegal. sd_clock = hclk/(div + 1) If hclk is 240M and div is 599, 400KHz SD clock will be generated.
[7:4]			RSVD	
[3:2]	rw	2'h0	clk_tune_sel	select clock delay for rx sample 0: no delay 1: delay level 1 (~1.5ns typical) 2: delay level 2 (~3ns typical) 3: delay level 3 (~5ns typical)
[1]	rw	1'h0	void_fifo_error	Void FIFO error 0: close the function 1: open the function If open it, when FIFO will be overrun or underrun soon, the SD_CLK and the clock enable of this module will be closed, and wait to host to read or write FIFO. Note: this function needs to be supported by card.
[0]	rw	1'h1	stop_clk	Disable SD card clock 1: stop SD card clock 0: SD card clock generated
0x3C			**CDR**	card interface control and card detect register

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表 14-5: SDMMC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:19]	rw	13'h0	otiming	define output timing
[18:6]	rw	13'h0	itiming	define input timing
[5]	rw	1'h0	cmd_od	Open Drain mode for cmd line (for eMMC identification mode) 0: cmd line is push-pull 1: cmd line is open-drain
[4]	rw	1'h1	cd_hvalid	Card detect high level valid 0: detect low level means card exist 1: detect high level means card exist (default)
[3]	rw	1'h1	en_cd	Enable card detect Only when the bit is valid, controller does card detect. If use sd_data[3] to do card detect, the bit should be cleared when transfer valid data.
[2]	rw	1'h0	otiming_sel	select output timing (according to otiming config)
[1]	rw	1'h0	itiming_sel	select input sample timing (according to itiming config)
[0]	rw	1'h1	sd_data3_cd	Use sd_data[3] to do card detect 0: use special pin to do card detect / write protect. (Currently not supported) 1: use sd_data[3] to do card detect (default)
0x40			**DBGR1**	card debug port1 register
[31]			RSVD	
[30:16]	r	15'h1	data_st	data state for debug only
[15:0]	r	16'h1	cmd_st	command state for debug only
0x44			**DBGR2**	card debug port2 register
[31:30]	rw	2'h0	dbg_sel	for debug only
[29:26]			RSVD	
[25:16]	r	10'h0	valid_data_cou	for debug only
[15:14]			RSVD	
[13:0]	r	14'h0	host_word_counter	for debug only
0x48			**CEATA**	CE-ATA/SDIO mode register
[31:4]			RSVD	
[3]	rw	1'h0	sdio_4wires_multi_irq	Select the sdio host 4 wires interrupt on multi-block support 0: host not support 4 wires interrupt on multi-block data transfers 1: host support 4 wires interrupt on multi-block data transfers
[2]	rw	1'h0	sdio_4wires_irq	Select the sdio host 4 wires interrupt support 0: host not support 4 wires interrupt on single-block data transfers 1: host support 4 wires interrupt on single-block data transfers
[1]	rw	1'h0	enable_sdio_irq	Select the sdio card mode, default is sd card 0: sd card mode , no sdio card interrupt 1: sdio card mode , enable sdio card interrupt
[0]	rw	1'h0	ata_mode	Select the card type, default is sd card 0: sd card mode 1: CE-ATA device mode
0x54			**DSR**	data status register
[31:8]			RSVD	
[7:0]	r	8'h0	sd_data_i_ll	The status of each sd data pad status
0x58			**CDCR**	clock duty cycle register
[31:1]			RSVD	
[0]	rw	1'h1	clk_config	1: the sd clock is 50% duty cycle 0: the high level of the sd clock is 1 hclk cycle

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表 14-5: SDMMC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
0x5C			**CASR**	cache status register
[31:4]			RSVD	
[3]	rw1s	1'h0	cache_flush	Set 1 to flush cache. Should set when cache not busy.
[2]	r	1'h0	cache_busy	Indicates cache is working
[1]	rw1c	1'h0	sd_busy	Read 1 indicates sd is ready for normal access. Ahb access will be hold during sd_busy asserted. After sd normal access done, write 1 to clear, and ahb access will continue
[0]	rw1s	1'h0	sd_req	Set 1 to request sd normal access. sd_req will be cleared automatically after sd_busy asserted
0x60			**CACR**	cache control register
[31]	rw	1'h1	cache_en	enable cache 1: ahb read will return cached data 0: ahb read always return dummy data with no error response
[30]	rw	1'h1	cache_to_en	enable ahb read timeout recover
[29]	rw	1'h0	cache_force_read	force cache read done 1: start new fetch for miss access only after cache read done 0: start new fetch for miss access even when cache is still filling (read will be breaked by cmd12)
[28]	rw	1'h1	cache_sdsc	select card version 1: card size <=2GB, address of cmd18 is in byte 0: card size >2GB, address of cmd18 is in block
[27]	rw	1'h0	cache_nocrc	1: return ahb data without crc check 0: return ahb data after block crc pass
[26]	rw	1'h0	cache_hresp	1: generate ahb error response when error occur 0: no ahb error response generated. Could check cache_err interrupt
[25:24]			RSVD	
[23:20]	rw	4'h8	cache_pref_block	cache prefetch depth is cache_pref_block blocks. Should be no less than cache_block
[19]			RSVD	
[18:16]	rw	3'h4	cache_block	cache depth is cache_block blocks
[15]	rw	1'h0	stop_long_rsp	Stop response is 136-bit, long response
[14]	rw	1'h1	stop_has_rsp	Stop command have a response
[13:8]	rw	6'h0c	stop_index	Command index for stop. CMD12 by default
[7]	rw	1'h0	read_long_rsp	Read response is 136-bit, long response
[6]	rw	1'h1	read_has_rsp	Read command have a response
[5:0]	rw	6'h12	read_index	Command index for cache read. CMD18 by default
0x64			**CACNT**	cache counter register
[31:16]	rw	16'hffff	cache_tor	timeout count register for ahb read
[15:8]	rw	8'h0	cache_ndc	data-cmd interval counter in hclk cycles
[7:0]	rw	8'h20	cache_ncc	cmd-cmd interval counter in hclk cycles
0x68			**CAOFF**	cache offset register
[31:0]	rw	32'h0	cache_offset	offset to map ahb address to sd address for ahb access
0x200			**FIFO**	FIFO entry
[31:0]	rw	32'h0	data	Entry to access internal FIFO. Access should be word-aligned, ranging from 0x200 to 0x3fc. Inside the range, write to any address will push the data into the FIFO, and read any address will pop a word from the FIFO.

14.3 MPI

芯片共有 4 个 MPI，其中 MPI1，MPI2 和 MPI3 位于 HPSYS，可向 DMAC1 发送请求；MPI5 位于 LPSYS，可向 DMAC2 发送请求。

MPI1 的输入输出连接至 IO(SA)，用于访问芯片内合封 (SiP) 的 8 线 pSRAM。

MPI2 的输入输出连接至 IO(SB)，用于访问芯片内合封 (SiP) 的另一片 8 线 pSRAM。

MPI3 的输入输出连接至 IO(PA)，用于访问芯片外接的 NOR/NAND Flash。

MPI5 的输入输出连接至 IO(SC)，用于访问芯片内合封 (SiP) 的 4 线 NOR Flash。

MPI (Memory Peripheral Interface) 控制器是一个专用的 memory 通信接口，支持多种片外存储颗粒，包括：

- SPI NOR Flash，支持 1 线/2 线/4 线，支持 DTR 模式
- SPI NAND Flash，支持 1 线/2 线/4 线
- pSRAM，支持 x8 和 x16 数据位宽，支持 Xccela 标准接口，兼容 Legacy 接口
- HyperRAM，支持 x8 和 x16 数据位宽，支持 HyperBus 标准接口

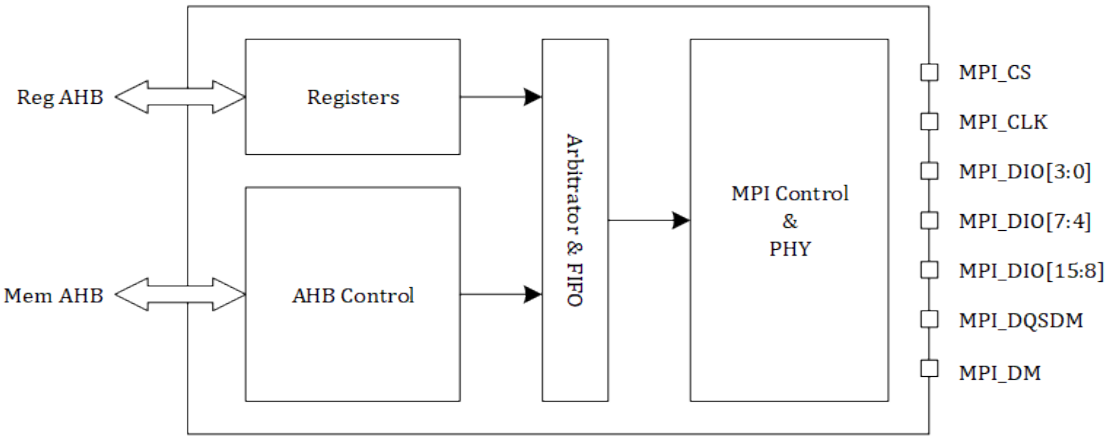

图 14-4: MPI 控制器框图

MPI 控制器支持两种操作模式：（1）寄存器模式和（2）地址映射模式。两种模式的切换由硬件自动完成，可动态穿插执行。且无论哪种模式，都支持高度可定制的接口时序，以兼容各种存储颗粒。

寄存器模式

- 通过寄存器操作，发送一个命令时序。也可以将该命令设置为状态查询命令反复发送，直到读回的数据满足某个预设状态
- 支持发送包含两个命令时序的序列，其中第二个命令可设置为状态查询命令反复发送，直到读回的数据满足某个预设状态
- 支持 DMA 通道，通过寄存器 FIFO 接口完成数据搬运

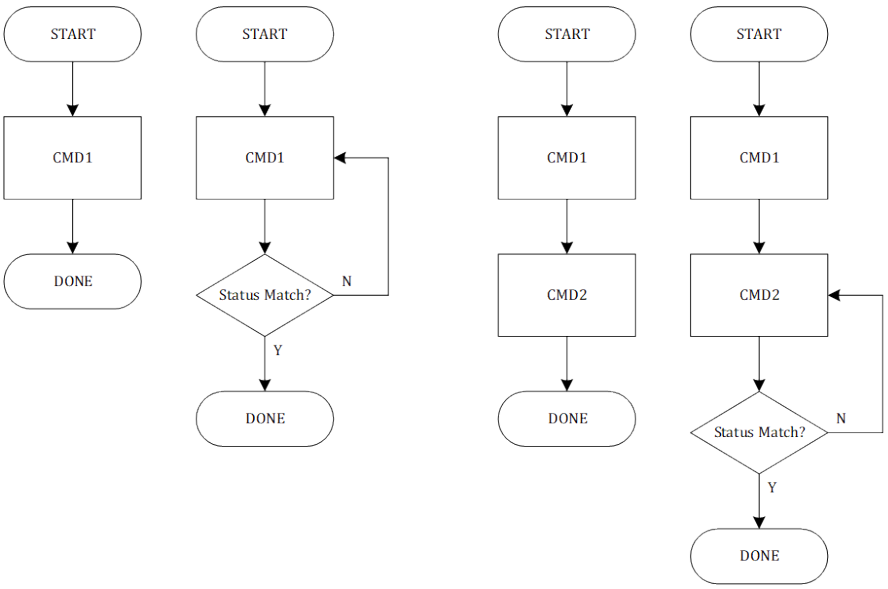

图 14-5: 寄存器模式单个和多个命令时序的序列

地址映射模式

- 外部 memory 映射为 AHB 地址空间，自动将 AHB 总线读写转换为预设的 Memory 接口时序，实现 XIP 功能
- 支持 Byte (8-bit)、Half-word (16-bit) 和 Word (32-bit) AHB 访问
- 高效转换 AHB Wrap 操作，不依赖于颗粒是否支持 Wrap
- 支持 XIP 实时（On-The-Fly）解密，模式为 AES128-CTR 或者 AES256-CTR
- 支持连续读写功能，如果当前一笔 AHB 的读写地址与前一笔连续，则直接开始数据传输，省略命令和地址部分。该功能可大幅提升大块数据搬运时的有效带宽
- 针对 pSRAM 和 HyperRAM 的内部动态刷新特性，自动处理颗粒最长 CS 拉低时间、最近 CS 访问间隔、最大 burst 数据长度等限制，无需软件处理

14.3.1 MPI 寄存器

表 14-6: MPI 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00			**CR**	Control Register
[31]	w1t	1'h0	ABORT	Write 1 to abort internal state machine. For debug purpose only
[30:26]			RSVD	
[25]	rw	1'h0	AHBDIS	Hold hreadyout low if AHB access
[24]	rw	1'h0	DFM	Dual Flash Mode Reserved-Do not modify
[23]	rw	1'b0	MX16	Mode X16 Reserved-Do not modify
[22]	rw	1'b0	PREFE	Prefetch enable. If enabled, MPI will prefetch at consequtive address following a read transaction. Recommend to use when reading large data in a burst manner. 0: prefetch disabled 1: prefetch enabled

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表 14-6: MPI 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[21]	rw	1'b0	OPIE	OPI interface enable 0: x8 mode disabled 1: x8 mode enabled
[20]	rw	1'b0	HWIFE	Hardware interface enable Reserved-Do not modify
[19]	rw	1'b0	SMM	Status match mode 0: AND mode 1: OR mode
[18]	rw	1'b0	SME2	Status match enable. If enabled, CMD2 will be issued repeatedly until the data match the value in SMR and SMKR 0: disabled 1: enabled
[17]	rw	1'b0	SME1	Status match enable. If enabled, CMD1 will be issued repeatedly until the data match the value in SMR and SMKR 0: disabled 1: enabled (either SME1 or SME2 can be enabled, and SME1 has high priority)
[16]	rw	1'b0	CMD2E	Enable CMD2 0: disabled 1: CMD2 is enabled and will be issued after CMD1 with an interval of TI2
[15:14]			RSVD	
[13]	rw	1'h0	RBXIE	Row boundary crossing interrupt enable
[12]	rw	1'h0	CSVIE	CS max violation interrupt enable
[11]	rw	1'h0	SMIE	Status match interrupt enable
[10]			RSVD	
[9]			RSVD	
[8]	rw	1'h0	TCIE	Transfer complete interrupt enable
[7]	rw	1'h0	CTRM	AES-CTR mode 0: AES-128 1: AES-256
[6]	rw	1'h0	CTRE	AES-CTR on-the-fly decryption enable 0: disabled 1: enabled, data read from memory will be decrypted on the fly by MPI controller
[5]	rw	1'h0	DMAE	DMA enable 0: disabled 1: enable DMA to read or write DR register
[4]	rw	1'h0	HOLD	The value of HOLD when HOLDE is set
[3]	rw	1'h0	HOLDE	Enable HOLD function on IO3. Use this only in SPI or Dual SPI mode
[2]	rw	1'h0	WP	The value of WP when WPE is set
[1]	rw	1'h0	WPE	Enable WP function on IO2. Use this only in SPI or Dual SPI mode
[0]	rw	1'h0	EN	Enable MPI
0x04			**DR**	Data Register
[31:0]	rw	32'h0	DATA	The entry of internal data FIFO
0x08			**DCR**	Device Control Register
[31]	rw	1'h0	FIXLAT	Indicate PSRAM is fixed latency or variable latency. It must be compatible to the configuration in PSRAM registers. Recommend always set to 1. 0: variable latency 1: fixed latency

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表 14-6: MPI 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[30:26]	rw	5'h0	TRCMIN	Write/Read cycle minimum time in internal MCLK cycles. Please see MCLK frequency in PSCLR description. For example, if PSRAM clock is 120MHz (i.e. internal MCLK is 240MHz) and TRCMIN = n, then tRC time = (n+1) * 1000/240 ns which must meet minimum tRC requirement for PSRAM
[25:22]	rw	4'h2	CSHMIN	Minimum CS high deselect time in MCLK cycles. For example, if PSRAM clock is 120MHz (i.e. internal MCLK is 240MHz) and CSHMIN = n, then CS High time = (n+1) * 1000/240 ns which must meet minimum tCPH requirement for PSRAM
[21:18]	rw	4'h0	CSLMIN	Minimum CS low active time in MCLK cycles. For example, if PSRAM clock is 120MHz (i.e. internal MCLK is 240MHz) and CSLMIN = n, then CS Low time = (n+1) * 1000/240 ns which must meet the minimum tCEM requirement for PSRAM
[17:6]	rw	12'h0	CSLMAX	Maximum CS low active time in MCLK cycles For example, if PSRAM clock is 120MHz (i.e. internal MCLK is 240MHz) and CSLMAX = n, then CS Low time = (n+1) * 1000/240 ns which must meet the maximum tCEM requirement for PSRAM
[5]	rw	1'h0	XLEGACY	Xccela legacy protocol. Set to 1 for AP 32Mb PSRAM only, othersize always set to 0.
[4]	rw	1'h0	HYPER	HyperBus protocol. Set to 1 for HyperRAM.
[3]	rw	1'h0	DQSE	DQS enable. Setting to 1 indicates device provides DQS signal for Rx data latching
[2:0]	rw	3'h0	RBSIZE	Row boundary size. 0: no row boundary 1: $2^{(1+3)}$ = 16 bytes 2: $2^{(2+3)}$ = 32 bytes ... n: $2^{(n+3)}$ bytes
0x0C			**PSCLR**	Prescaler Register
[31:8]			RSVD	
[7:0]	rw	8'h4	DIV	Prescaler divider. 0: MCLK = FCLK/1 1: MCLK = FCLK/1 2: MCLK = FCLK/2 n: MCLK = FCLK/n Note: FLASH clock = MCLK. E.g. FCLK=192M and DIV=2, then FLASH clock = MCLK = 192/2 = 96MHz PSRAM clock = MCLK/2. E.g. FCLK=240M and DIV=1, then PSRAM clock = MCLK/2 = 240/2 = 120MHz
0x10			**SR**	Status Register
[31]	r	1'h0	BUSY	For debug purpose only
[30:6]			RSVD	
[5]	r	1'h0	RBXF	Row boundary crossing flag
[4]	r	1'h0	CSVF	CS max violation flag
[3]	r	1'h0	SMF	Status match flag in Polling Mode
[2]			RSVD	

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表 14-6: MPI 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[1]			RSVD	
[0]	r	1'h0	TCF	Transfer complete flag
0x14			**SCR**	Status Clear Register
[31:6]			RSVD	
[5]	w1c	1'h0	RBXFC	Write 1 to clear RBXF
[4]	w1c	1'h0	CSVFC	Write 1 to clear CSVF
[3]	w1c	1'h0	SMFC	Write 1 to clear SMF
[2]			RSVD	
[1]			RSVD	
[0]	w1c	1'h0	TCFC	Write 1 to clear TCF
0x18			**CMDR1**	Command Register
[31:8]			RSVD	
[7:0]	rw	8'h0	CMD	Command. Write to this register will trigger the sequence specified in CCR1
0x1C			**AR1**	Address Register
[31:0]	rw	32'h0	ADDR	Address
0x20			**ABR1**	Alternate Byte Register
[31:0]	rw	32'h0	ABYTE	Alternate byte
0x24			**DLR1**	Data Length Register
[31:20]			RSVD	
[19:0]	rw	20'h0	DLEN	Data length 0: one byte 1: two bytes ... n: (n+1) bytes
0x28			**CCR1**	Communication Configuration Register
[31:22]			RSVD	
[21]	rw	1'b0	FMODE	Function Mode 0: read mode 1: write mode
[20:18]	rw	3'h0	DMODE	Data Mode 0: no data phase 1: single line 2: dual lines 3: quad lines 4/5/6: reserved 7: quad lines DDR
[17:13]	rw	5'h0	DCYC	Number of dummy cycles 0: no dummy cycle 1: one dummy cycle 2: two dummy cycles
[12:11]	rw	2'h0	ABSIZE	Alternate byte size 0: one byte 1: two bytes 2: three bytes 3: four bytes

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表 14-6: MPI 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[10:8]	rw	3'h0	ABMODE	Alternate byte mode 0: no alternate byte 1: single line 2: dual lines 3: quad lines 4/5/6: reserved 7: quad lines DDR
[7:6]	rw	2'h0	ADSIZE	Address size 0: one byte 1: two bytes 2: three bytes 3: four bytes
[5:3]	rw	3'h0	ADMODE	Address mode 0: no address phase 1: single line 2: dual line 3: quad line 4/5/6: reserved 7: quad line DDR
[2:0]	rw	3'h0	IMODE	Instruction mode 0: no instruction phase 1: single line 2: dual lines 3: quad lines 4/5/6 - reserved 7 - quad lines DDR
0x2C			**CMDR2**	Command Register
[31:8]			RSVD	
[7:0]	rw	8'h0	CMD	Command 2. If CMD2E is enabled, the CMD2 sequence will be issued after CMD1 as specified in CCR2 Note: CMD2 sequence cannot be issue individually
0x30			**AR2**	Address Register
[31:0]	rw	32'h0	ADDR	Address byte in CMD2 sequence
0x34			**ABR2**	Alternate Byte Register
[31:0]	rw	32'h0	ABYTE	Alternate byte in CMD2 sequence
0x38			**DLR2**	Data Length Register
[31:20]			RSVD	
[19:0]	rw	20'h0	DLEN	Data length in CMD2 sequence
0x3C			**CCR2**	Communication Configuration Register
[31:22]			RSVD	
[21]	rw	1'b0	FMODE	
[20:18]	rw	3'h0	DMODE	
[17:13]	rw	5'h0	DCYC	
[12:11]	rw	2'h0	ABSIZE	
[10:8]	rw	3'h0	ABMODE	
[7:6]	rw	2'h0	ADSIZE	
[5:3]	rw	3'h0	ADMODE	
[2:0]	rw	3'h0	IMODE	This register specifies the format of CMD2 sequence. Refer to CCR1 description
0x40			**HCMDR**	AHB Command Register

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表 14-6: MPI 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:16]			RSVD	
[15:8]	rw	8'h02	WCMD	AHB write command. During XIP, the AHB write transaction will be translated into this Write Command on memory interface
[7:0]	rw	8'h0b	RCMD	AHB read command. During XIP, the AHB read transaction will be translated into this Read Command on memory interface
0x44			**HRABR**	AHB Read Alternate Byte Register
[31:0]	rw	32'h0	ABYTE	
0x48			**HRCCR**	AHB Read Communication Configuration Register
[31:21]			RSVD	
[20:18]	rw	3'h0	DMODE	
[17:13]	rw	5'h0	DCYC	
[12:11]	rw	2'h0	ABSIZE	
[10:8]	rw	3'h0	ABMODE	
[7:6]	rw	2'h0	ADSIZE	
[5:3]	rw	3'h0	ADMODE	
[2:0]	rw	3'h0	IMODE	This register specifies the format of AHB read command sequence. Refer to CCR1 description
0x4C			**HWABR**	AHB Write Alternate Byte Register
[31:0]	rw	32'h0	ABYTE	
0x50			**HWCCR**	AHB Write Communication Configuration Register
[31:21]			RSVD	
[20:18]	rw	3'h0	DMODE	
[17:13]	rw	5'h0	DCYC	
[12:11]	rw	2'h0	ABSIZE	
[10:8]	rw	3'h0	ABMODE	
[7:6]	rw	2'h0	ADSIZE	
[5:3]	rw	3'h0	ADMODE	
[2:0]	rw	3'h0	IMODE	This register specifies the format of AHB write command sequence. Refer to CCR1 description
0x54			**FIFOCR**	FIFO Control Register
[31:15]			RSVD	
[14:10]	rw	5'h8	TXSLOTS	When DMA enabled, asserts DMA reqeust if TXFIFO vacant slots is greater than or equal to TXSLOTS. Note: this field should be set in accordance to the burst length in DMA. For example, if DMA employs BURST8 transction, then this filed is set to 8
[9]	r	1'h0	TXF	Tx FIFO full flag
[8]	w1c	1'h0	TXCLR	write 1 to clear Tx FIFO
[7:2]			RSVD	
[1]	r	1'h1	RXE	Rx FIFO empty
[0]	w1c	1'h0	RXCLR	write 1 to clear Rx FIFO
0x58			**MISCR**	Miscelaneous Register
[31:28]	rw	4'h0	DBGSEL	
[27]			RSVD	
[26]	rw	1'h0	DTRPRE	Enable pre-sampling for DTR Reserved-Do not modify
[25]	rw	1'h1	SCKINV	Invert output clock. This bit is used to align (coarse tune) the output clock to the center of output data.
[24]	rw	1'h0	RXCLKINV	Invert internal Rx clock to add half-cycle delay (coarse tune) when sampling data. It is usually used for FLASH device w/ higher frequency.

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表 14-6: MPI 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[23:16]	rw	8'h0	DQSDLY	Delay the input DQS signal to the appropriate sampling position. For device w/ DQS signal only. Note: effective 7-bit
[15:8]	rw	8'h0	SCKDLY	Add delay on output clock to fine tune the clock position. Note: effective 7-bit
[7:0]	rw	8'h0	RXCLKDLY	Add delay on internal Rx clock to fine tune the sampling position. Note: effective 5-bit
0x5C			**CTRSAR**	CTR Starting Address Register
[31:10]	rw	22'h0	SA	Starting address of the AES decryption area. Since the lowest 10 bits are zero, the address is always 1KB aligned. Together with CTREAR, the total area is [CTRSAR, CTREAR) For example, CTRSAR = 32'h0, CTREAR = 32'h200000, then the on-the-fly decryption area is 0x0 - 0x1FFFFF
[9:0]			RSVD	
0x60			**CTREAR**	CTR Ending Address Register
[31:10]	rw	22'h0	EA	Ending address of the AES decryption area
[9:0]			RSVD	
0x64			**NONCEA**	Nonce A Register
[31:0]	rw	32'h0	NONCEA	Used for on-the-fly decryption
0x68			**NONCEB**	Nonce B Register
[31:0]	rw	32'h0	NONCEB	Used for on-the-fly decryption
0x6C			**AASAR**	Address Aliasing Start Address Register
[31:10]	rw	22'h0	SA	Starting address of the address aliasing area. Always 1KB aligned.Together with AAEAR, the aliasing area is [AASAR, AAEAR). If the address falls into this area, an offset AAOAR is added and the aliased address will be used to access external memory
[9:0]			RSVD	
0x70			**AAEAR**	Address Aliasing Ending Address Register
[31:10]	rw	22'h0	EA	Ending address of the address aliasing area
[9:0]			RSVD	
0x74			**AAOAR**	Address Aliasing Offset Address Register
[31:10]	rw	22'h0	OA	The offset to be added to the original address
[9:0]			RSVD	
0x78			**CIR**	Command Interval Register
[31:16]	rw	16'h0	INTERVAL2	The interval between CMD1 and CMD2 (or between CMD2 itself) if CMD2E is enabled. The unit is in MCLK cycles
[15:0]	rw	16'h0	INTERVAL1	The interval between CMD1 itself. The unit is in MCLK cycles
0x7C			**SMR**	Status Match Register
[31:0]	rw	32'h0	STATUS	If status match is enabled, this register is compared with the data read from external memory. Together with SMKR, only the bits with mask=1 will be considered to compare in AND or OR mode as configured in SMM field.
0x80			**SMKR**	Status Mask Register
[31:0]	rw	32'h0	MASK	Status mask 0: the corresponding bit is not considered to compare 1: the corresponding bit is considered to compare
0x84			**TIMR**	Timer Register
[31:16]			RSVD	

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表 14-6: MPI 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[15:0]	rw	16'h0	TIMEOUT	After the transaction is complete, CS remains low for multiple cycles of MCLK as specified by this register. For example if TIMEOUT=n, CS remains active for n cycles, during which if a new transaction occurs and the address is consecutive, the memory access can be resumed w/o sending the command and address again.
0x88			**WDTR**	WDT Register
[31]	r	1'h0	TOF	Timeout flag. Self cleared when HREADYOUT becomes ready
[30:17]			RSVD	
[16]	rw	1'b0	EN	WDT enable. This watchdog is on AHB side such that bus access will not hang in exceptional cases
[15:0]	rw	16'hffff	TIMEOUT	Set timeout value in number of clk_wdt cycles
0x8C			**PRSAR**	Prefetch Starting Address Register
[31:10]	rw	22'h0	SA	Starting address of the prefetch area If prefetch is enabled and the read address falls into [PRSAR, PREAR), controller will prefetch the following data
[9:0]			RSVD	
0x90			**PREAR**	Prefetch Ending Address Register
[31:10]	rw	22'h0	EA	Ending address of the prefetch area
[9:0]			RSVD	
0x94			**CALCR**	Calibration Clock Register
[31]	rw	1'h0	EN	calibration enable
[30:9]			RSVD	
[8]	r	1'h0	DONE	calibration done flag
[7:0]	r	8'h0	DELAY	calibration delay result
0x98			**APM32CR**	APM32 Control Register
[31:8]			RSVD	
[7:4]	rw	4'h4	TCPHW	For special use by AP 32Mb PSRAM. Reserved-Do not modify
[3:0]	rw	4'h2	TCPHR	For special use by AP 32Mb PSRAM. Reserved-Do not modify
0x9C			**CR2**	Control Register 2
[31:8]			RSVD	
[7:0]	rw	8'h0	LOOP	Repeat CMD1->CMD2 sequence for n times. This filed is only valid when CMD2E=1 and SME2=0. For example if LOOP=0, then the sequence is CMD1 -> CMD2. If LOOP=2, then the sequence is (CMD1->CMD2) -> (CMD1->CMD2) -> (CMD1->CMD2)

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